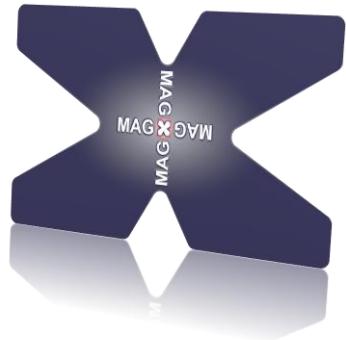


Electronics and DAQ for the GEM Detector

Pepe Gölker

MAGIX Collaboration Meeting 2017



Hardware

Electronics Periphery



HV Power Supply

- Need 7 channels per module or voltage divider
- Up to 4 kV
- Trip control
- Current monitoring ~50pA

Gas-Flow and -Quality Control

- Flowmeter
- Moisture and oxygen sensors

Current Control

- Measure leakage current with a pico amperemeter

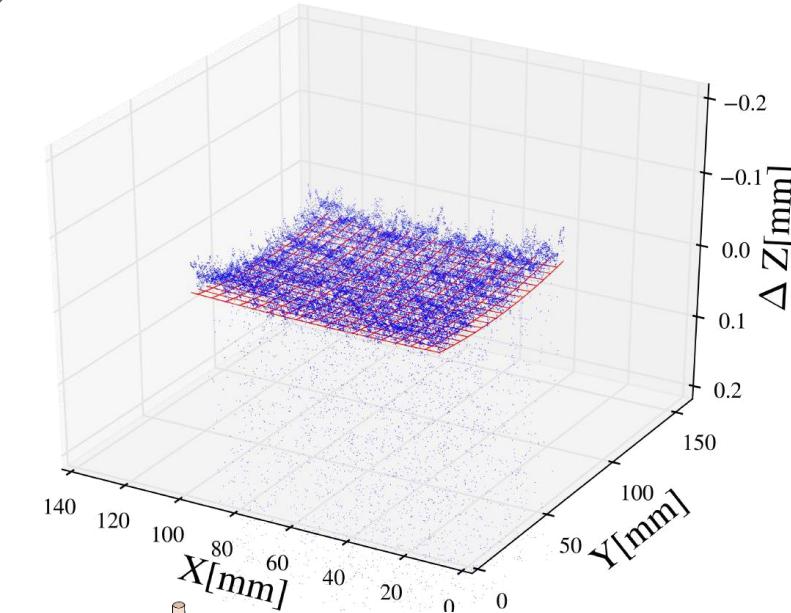
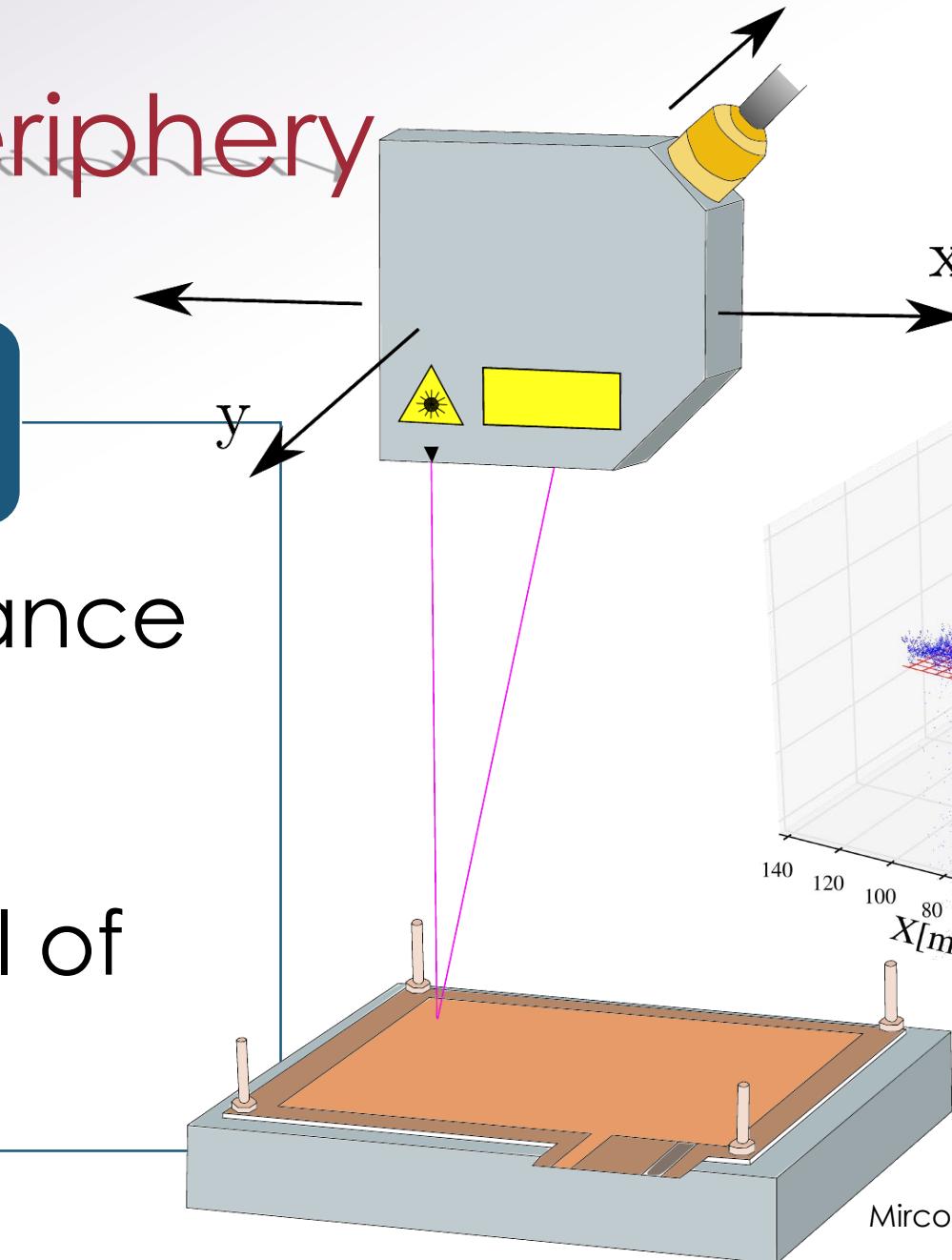


Mirco Christmann Diploma Thesis 2016

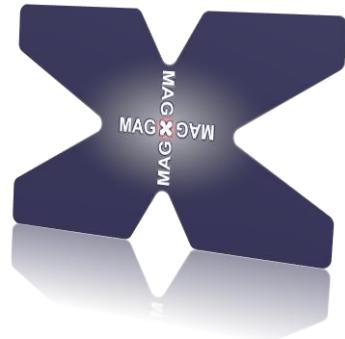
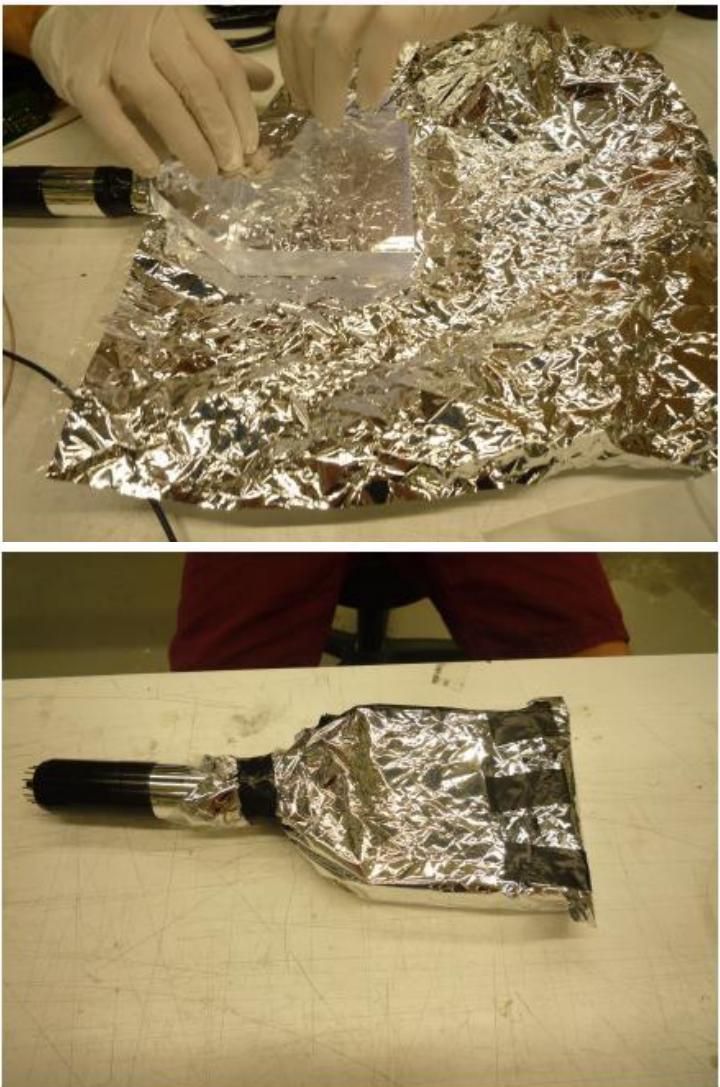
Electronics Periphery

Profile Laser

- Accurate distance measurement
- $\sim 1.8 \times 0.8 \text{ m}^2$
- Quality control of stretching



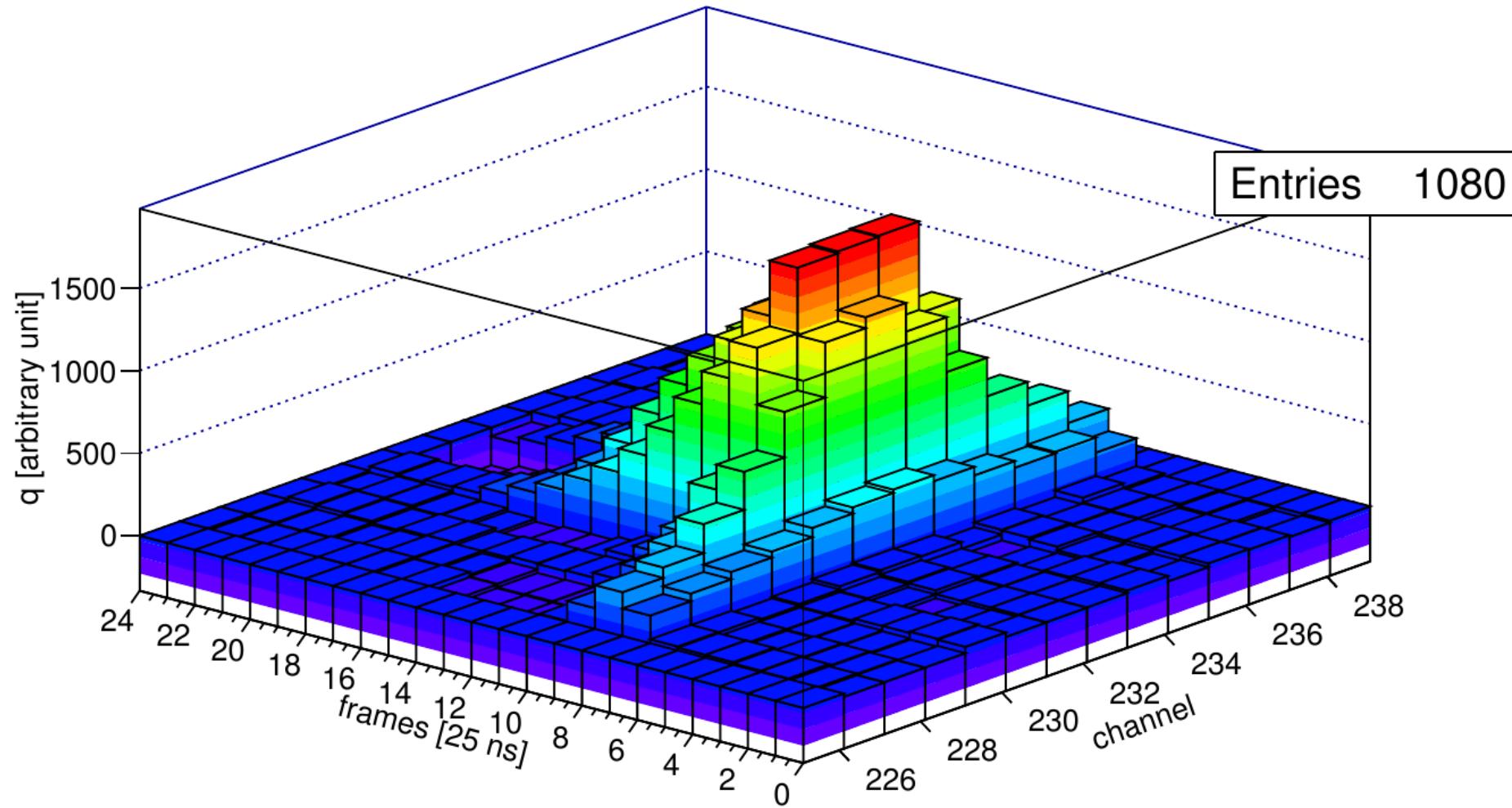
Trigger



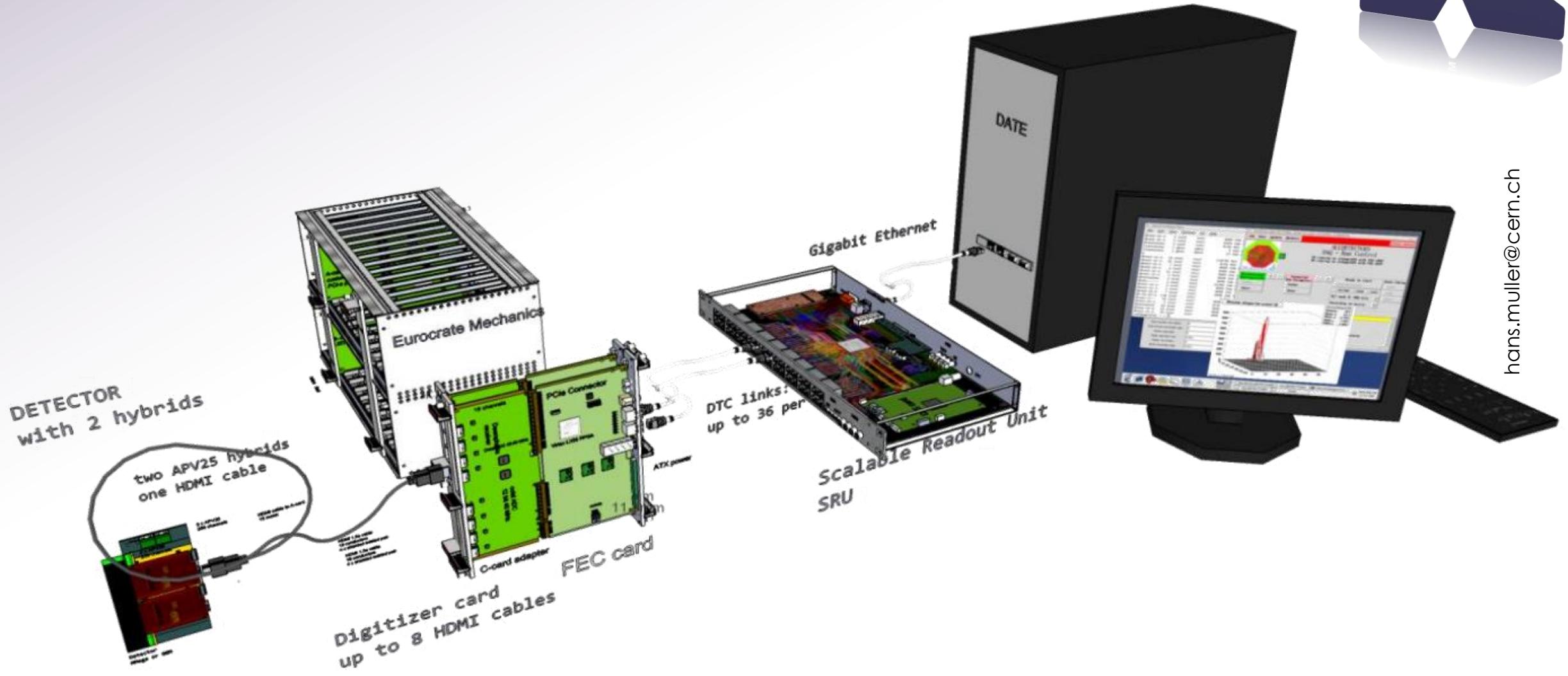
Signals



complete collected charge



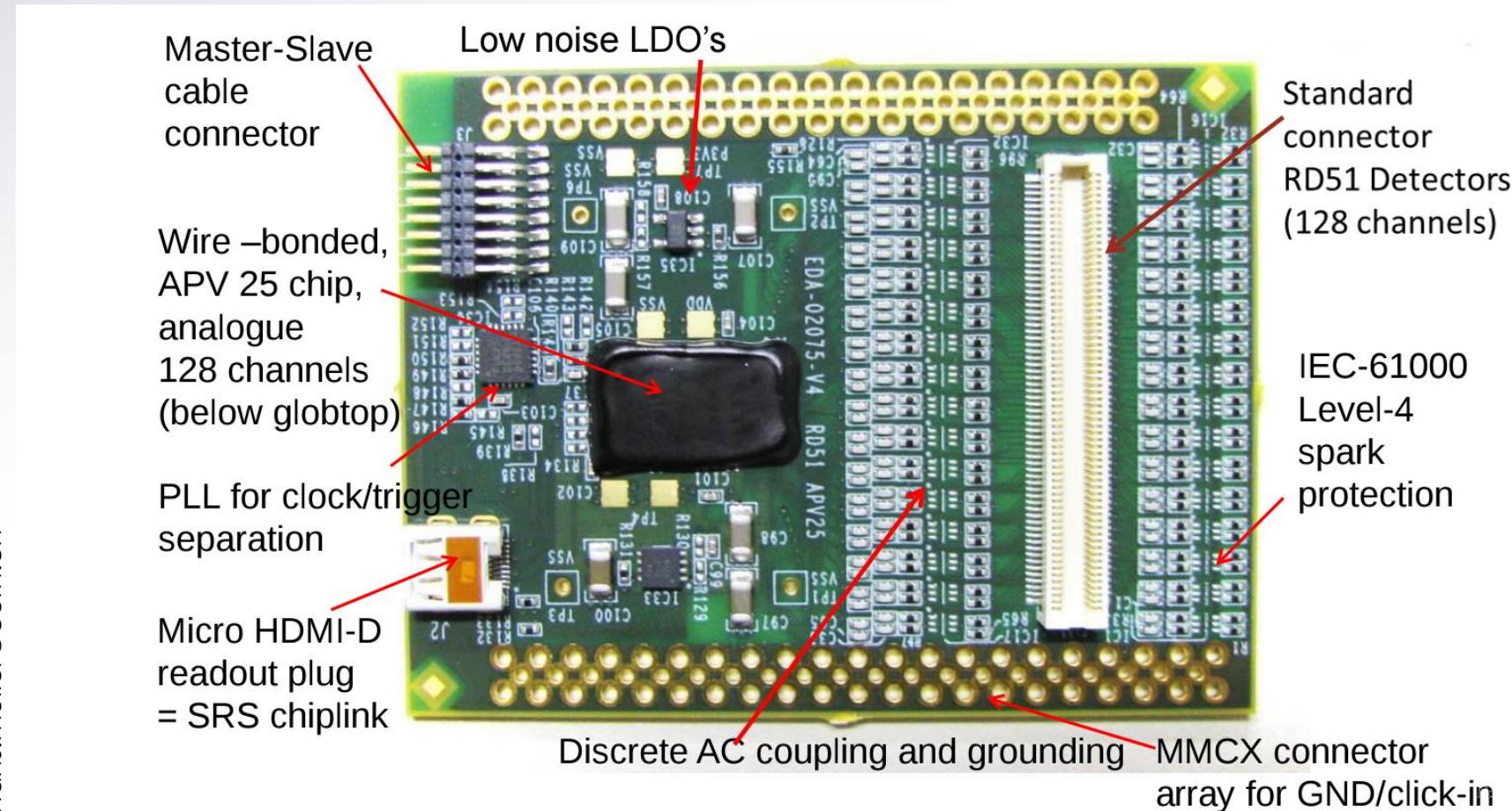
SRS – Scalable Readout System



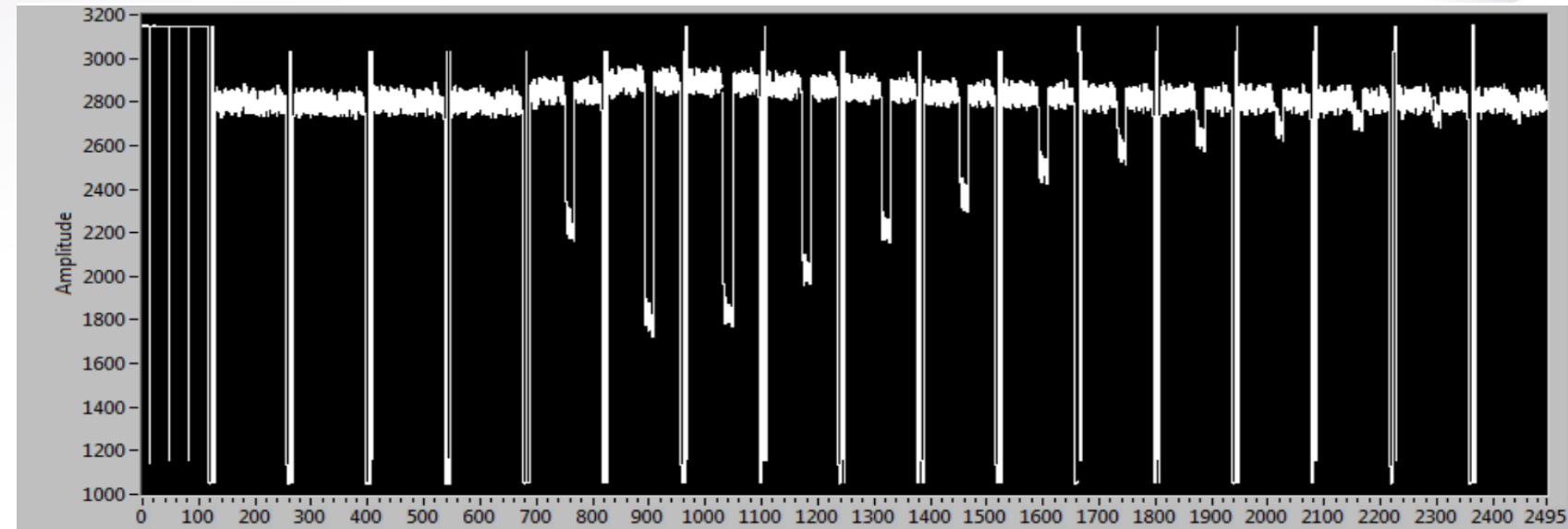
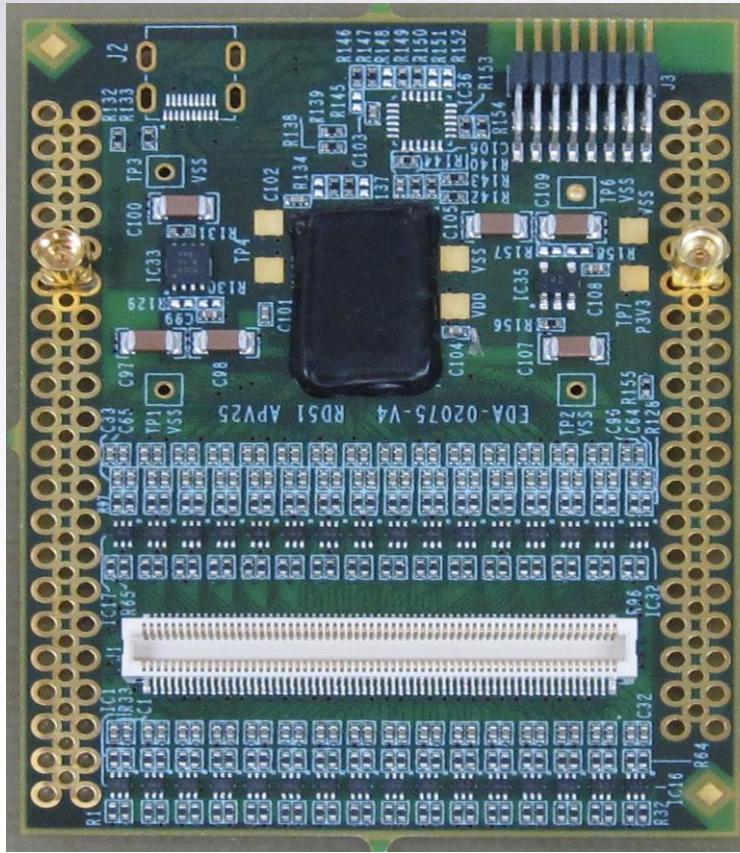
hans.muller@cern.ch



APV25 – Frontend Card



APV25 – Frontend Chip



128
Channels

40 MHz

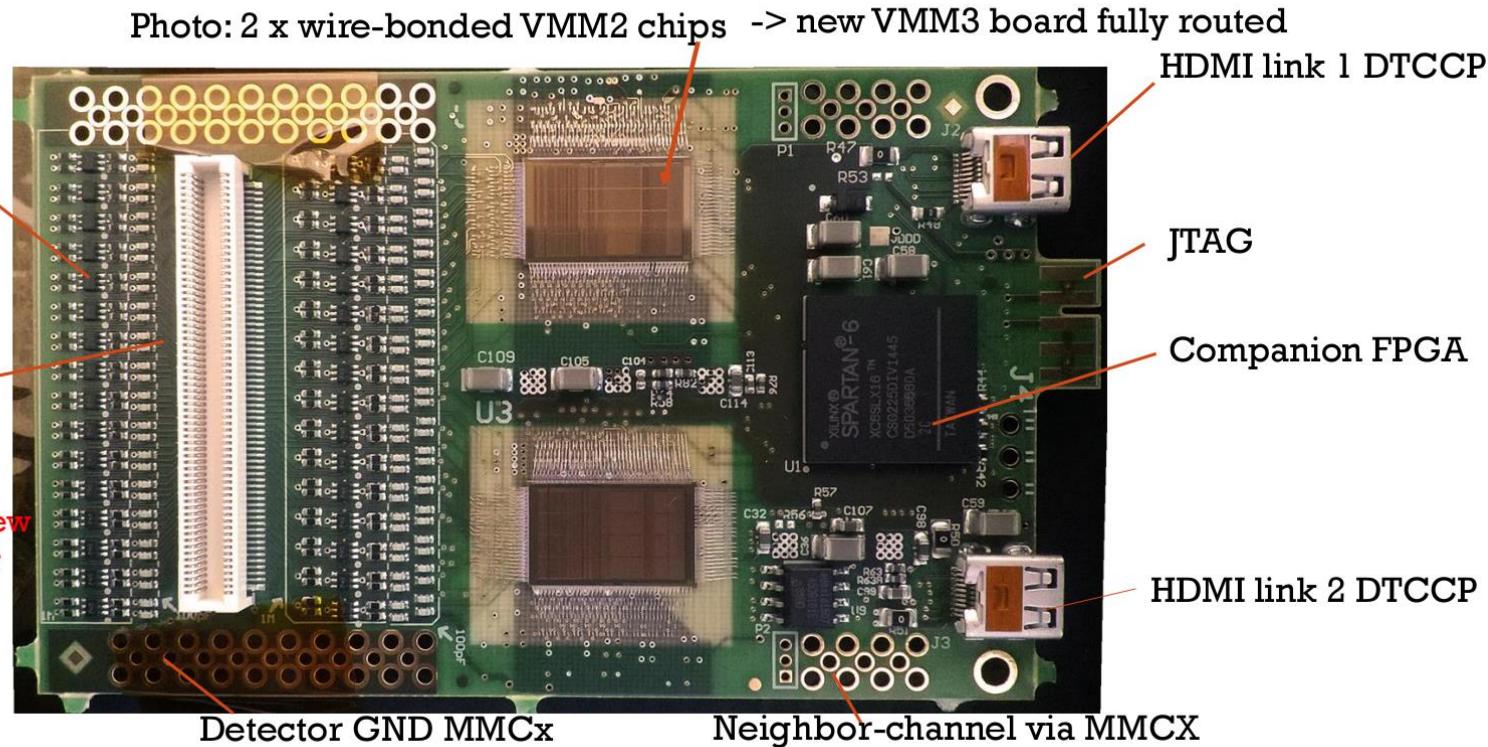
192 steps
data matrix

No trigger

APV25 – Problems



- Waveforms -> Nice for R&D
- Not capable of required rates
- Highest rate achieved ~7 kHz
- We need O(MHz)
-> new frontend chip VMM



Final Detector Requirements

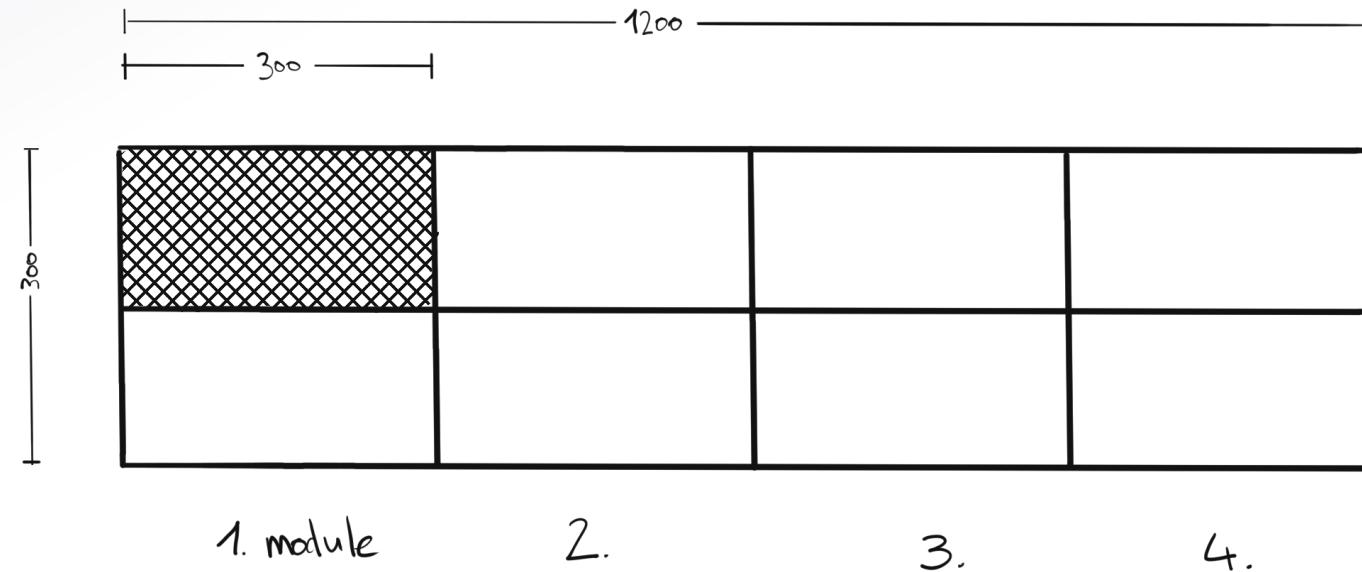


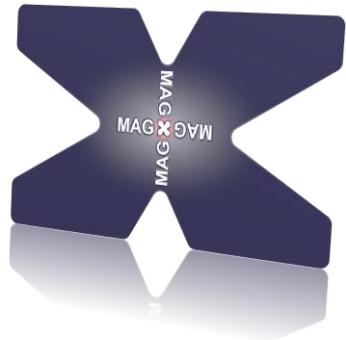
1 section

- 1500 channels
- 12 APVs/VMMs

1 module

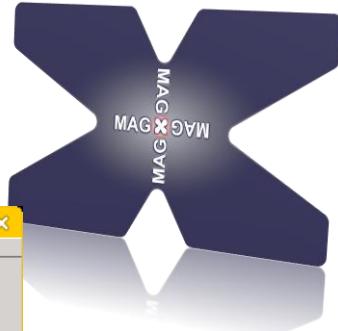
- 8 sections
- 10 k channels
- 96 APVs/VMMs





Software

SRS - Configuration



SRS SDC

- Scalable Detector Control
- Developed at NTUA

APV

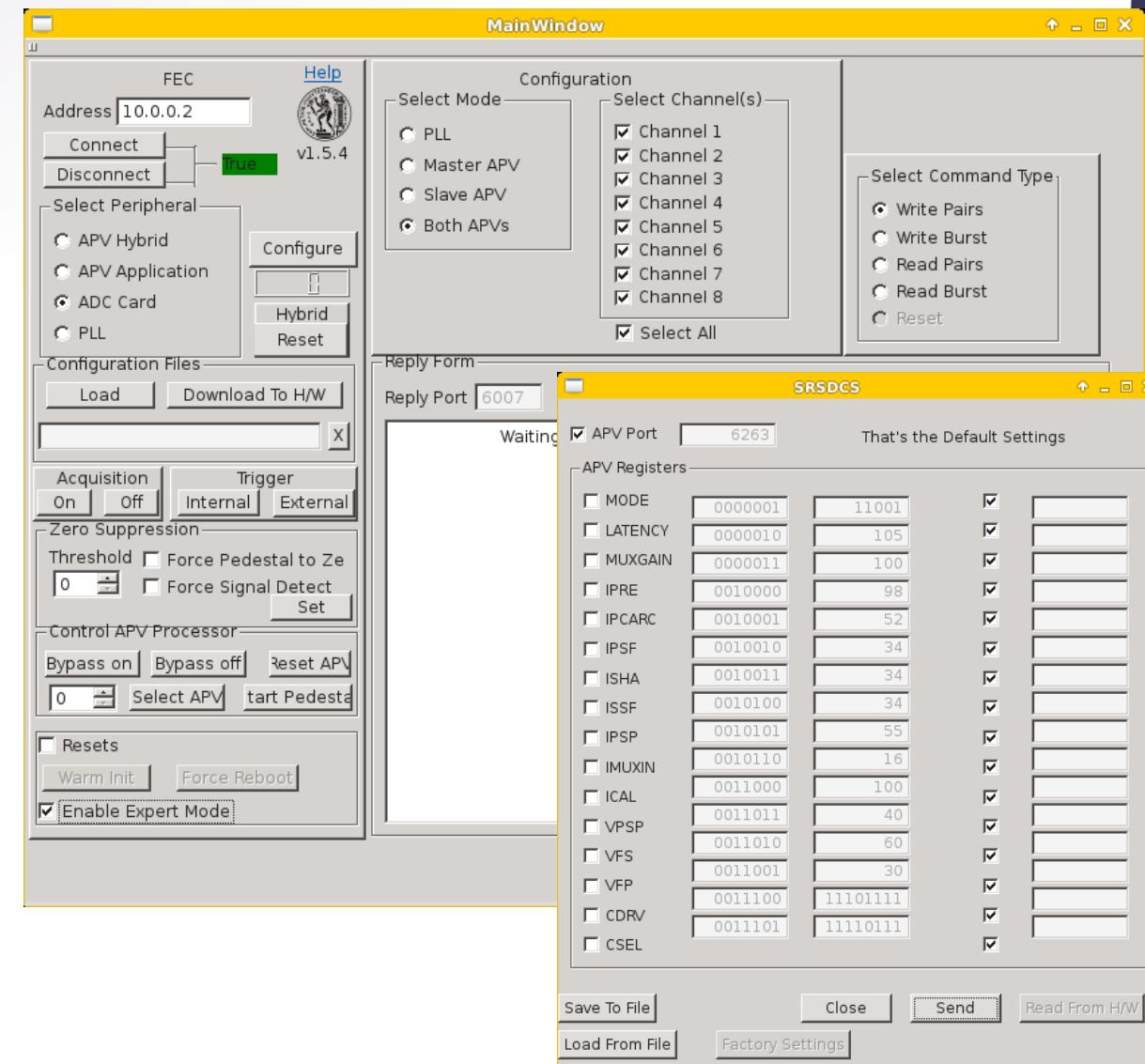
- Set baseline
- Set gain
- Set latency

FEC

- Set active APVs
- Set trigger mode

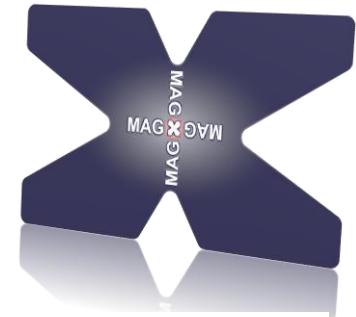
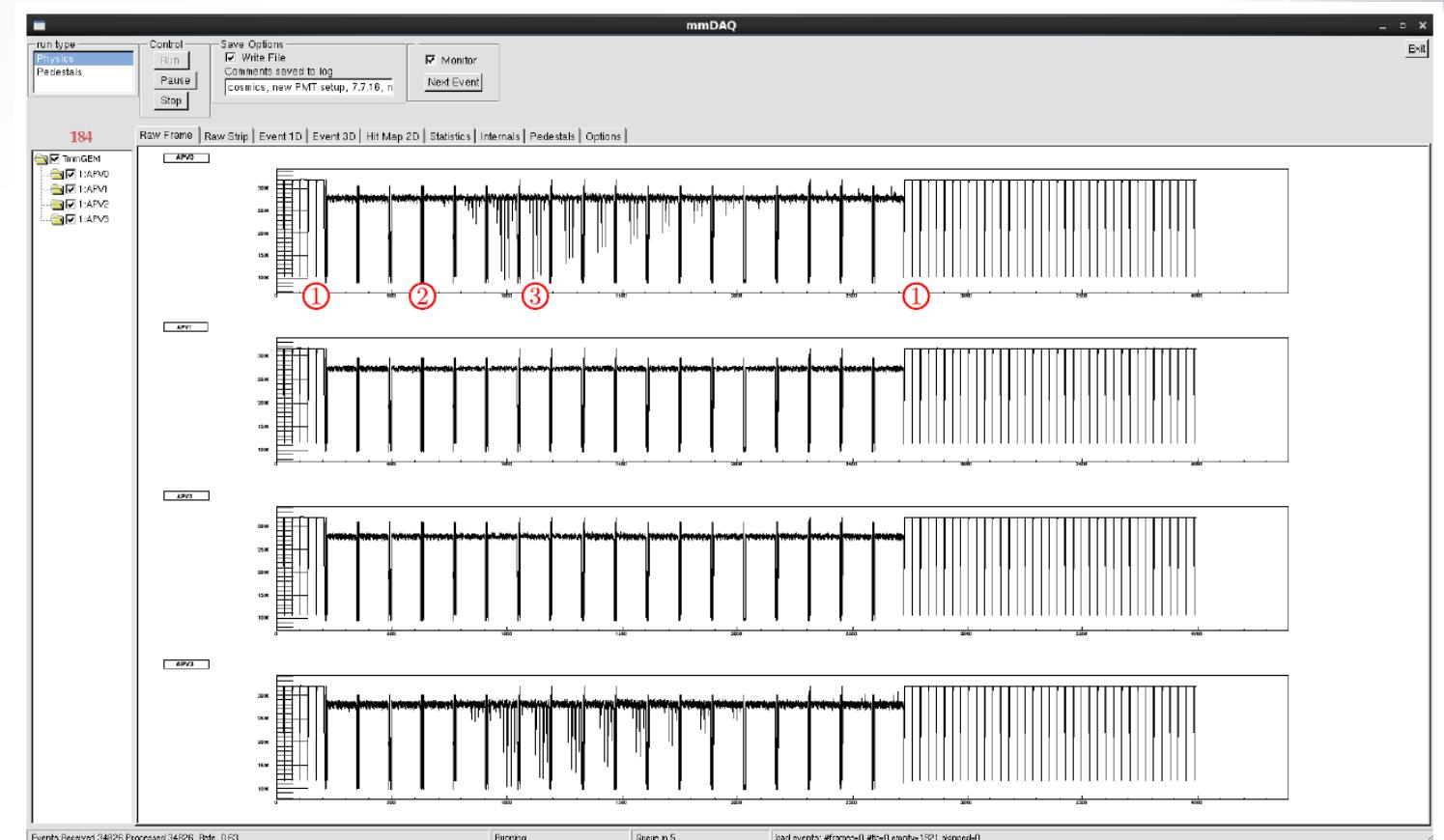
TODO

- Include to our slow control
-> Stefan L.



DAQ – mmdaq2

- Developed for Micromegas
- Based on root
- Load pedestals for APVs
- Monitor analog input
- Nice online statistics



Working Setup



- We have a fully working DAQ
- Now:
 - Write own slow control
 - Set up own DAQ
 - Get hands on VMMS



THANK YOU FOR YOUR ATTENTION!

<http://magix.kph.uni-mainz.de>



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Institute of
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Backup



APV - VMM

APV (ANALOGUE)

APV (250 nm CMOS)

- Pipeline depth: max. 192 clocks
- Trigger latency: max. 3 us
- Noise: < 500 e- intrinsic >750..1400 e- on detector
- dynamic range: 25 fC
- Detector capacity: 18... < 60pf
- ADC ext. 4096/1000 [counts/baseline]
- Gain: fixed CSA gain 100uA/mip, 5 output signal gains (in step of 20%)
- Timing jitter : $\frac{1}{2}(1/fc)$ [+ - 12ns]
- Shaping times: 50 ns adjustable to 80 ns
- max readout rate: 7 kHz

VMM (DIGITAL)

VMM (130nm CMOS)

- Pipeline depth: 64 digital frames (peak)
- Trigger latency: (self triggered) or L0 (12.8us)
- noise : < 400 e- on 10x10 detector reported
- dynamic range: expect $>>$ 25 fC
- Detector capacity: 30pF ... < 1nF
- ADC: embedded, 10 bit
- Gains: 8 CSA gains [0.5..16mV/fC]
- Timing jitter: 20 bit t-stamp, 1ns resolution
- Shaping times: 4 [25... 200ns]
- max readout rates: estimated 4 MHz/ch

