DEPFET Pixel Detector for Belle II

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Physik Department E18 - Technische Universität München

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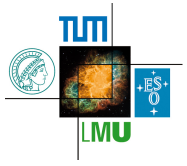


Belle II Experiment

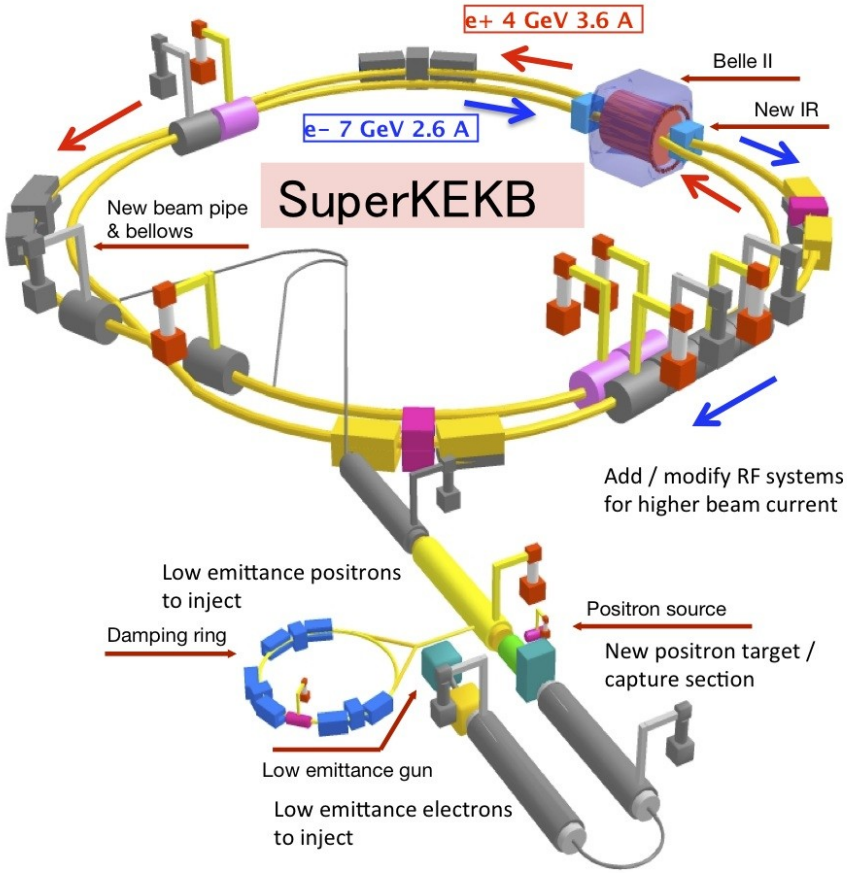
Pixel Detector

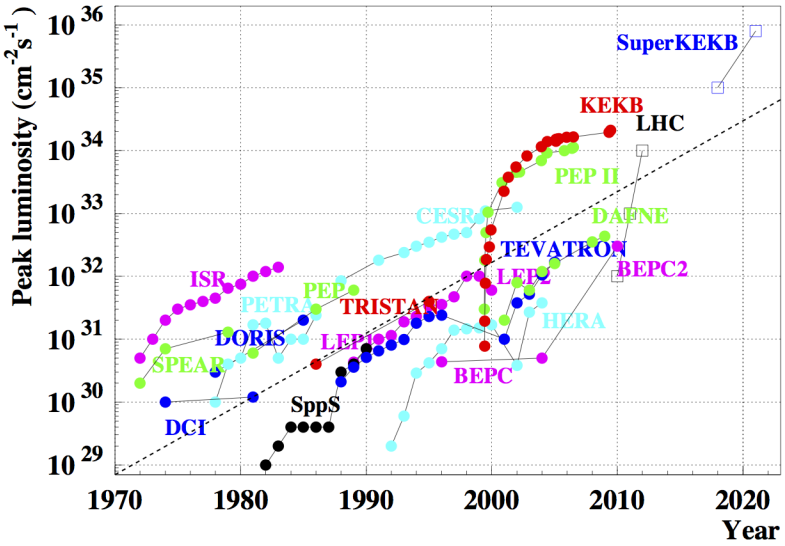
Gated Mode

Online Data Reduction

Conclusions

SuperKEKB



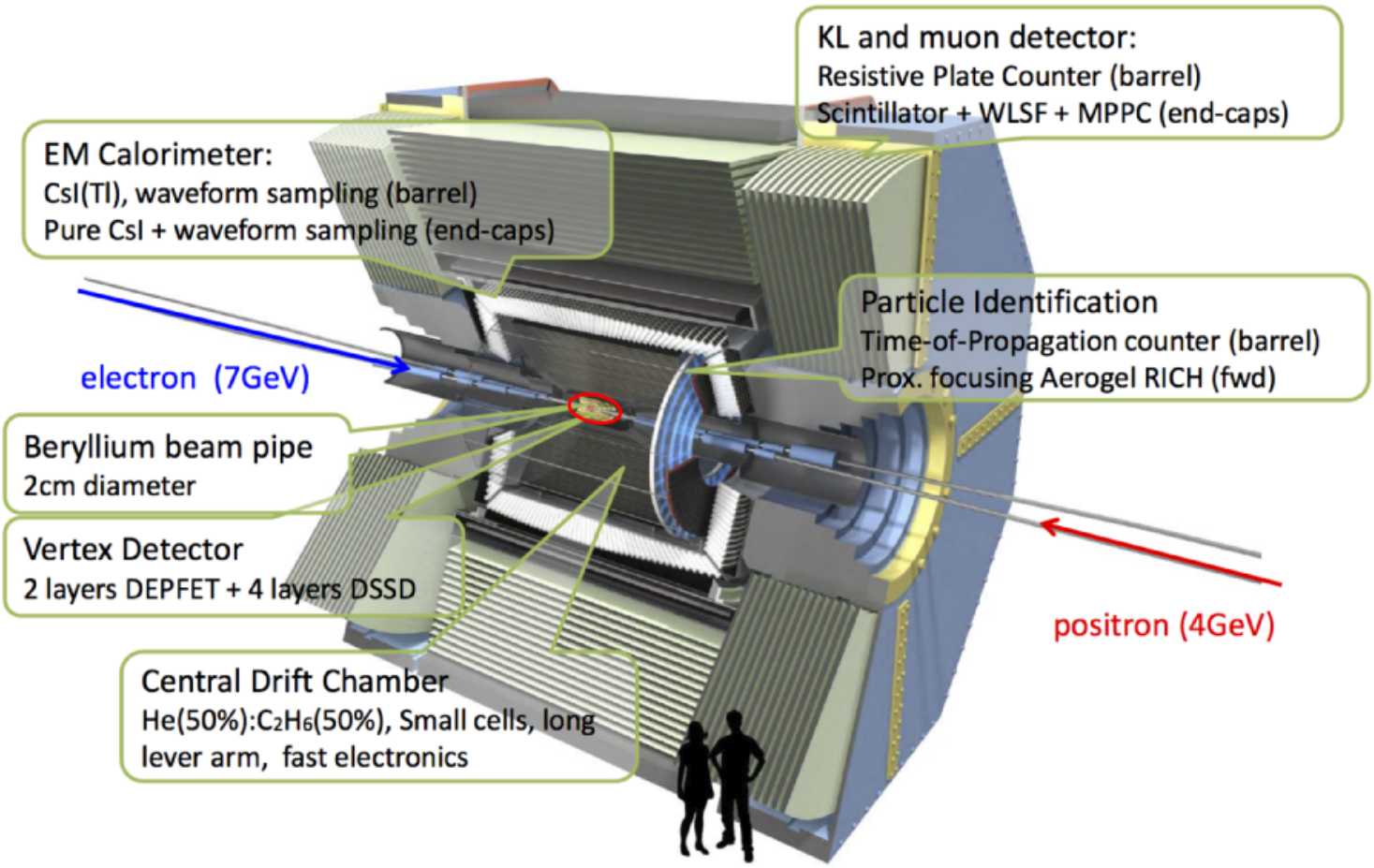


- Asymmetric e^+e^- collider operates at $\Upsilon(4S)$ resonance
- Nano beam scheme
  - $\Rightarrow$ smaller beam size (10 μmx60 nm)
- Luminosity $8 \cdot 10^{35} cm^{-2} s^{-1}$
  - $\Rightarrow$ 40 times higher than in KEKB

Belle II

Technische Universität München

Belle II Detector



Belle II Vertex Detector

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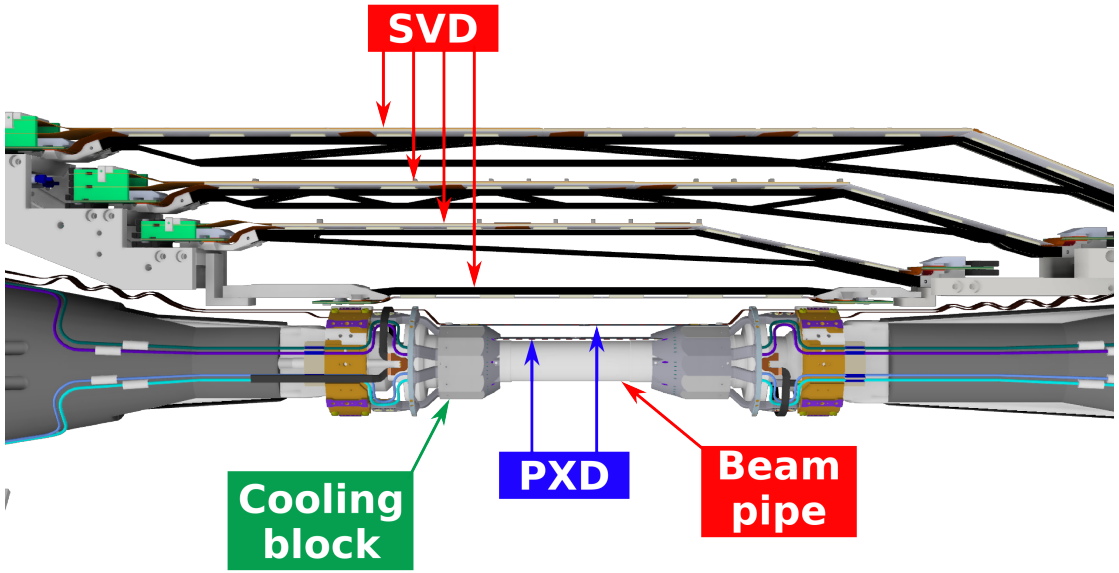
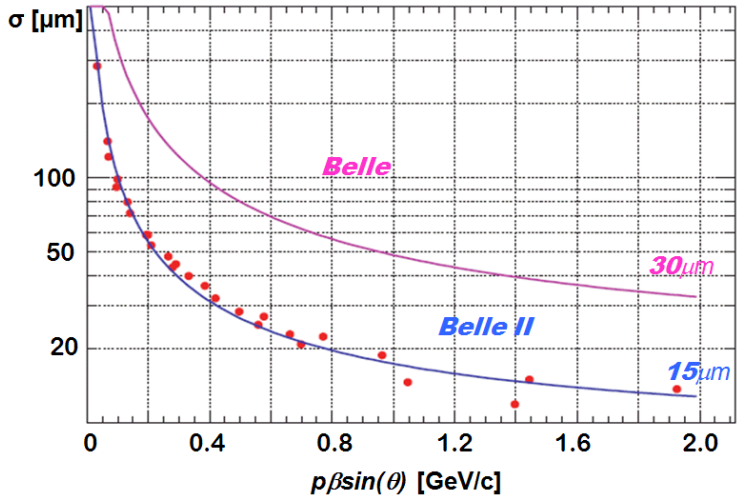
Requirements

- High resolution
- High sensitivity
- High signal-to-noise ratio
- Low material budget

Components

- DEPFET pixel detector (PXD)
  - ⇒ 40 modules (8 Mpx)
  - ⇒ 2 layers at R = 1.4, 2.2 cm
- Double-sided silicon strip detector (SVD)
  - ⇒ 45 ladders
  - ⇒ 4 layers at R = 3.8-14 cm





Depleted P-Channel Field Effect Transistor

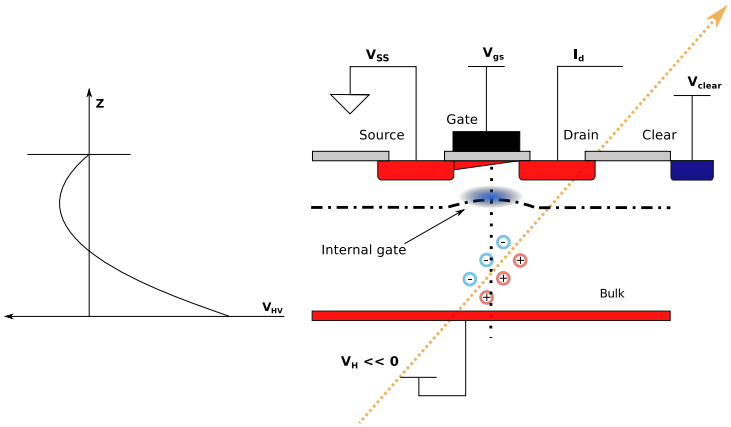


Figure : DEPFET Principle

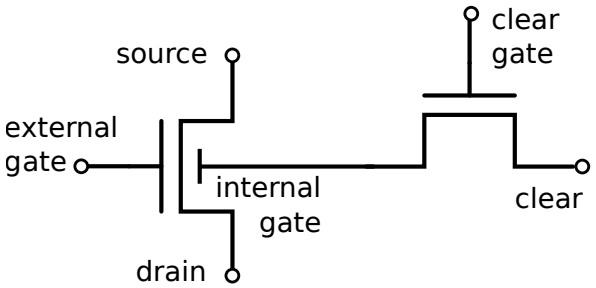


Figure : Equivalent circuit of the DEPFET pixel

- Detection and internal amplification
  - $\Rightarrow$ g_q = 500 pA/e^-
- Low intrinsic noise
- High signal-to-noise ratio
- Non-destructive readout
- High radiation tolerance
  - no charge transfer from internal gate
  - change in threshold voltage

From Pixel to Matrix

Rolling shutter read out

- 100 ns/row
- 4-fold read-out
  - ⇒ 4 rows read out in parallel
  - ⇒ 4 x drain lines (ADC channels)
- line steering chip required
- low power consumption
  - ⇒ only activated rows consume power

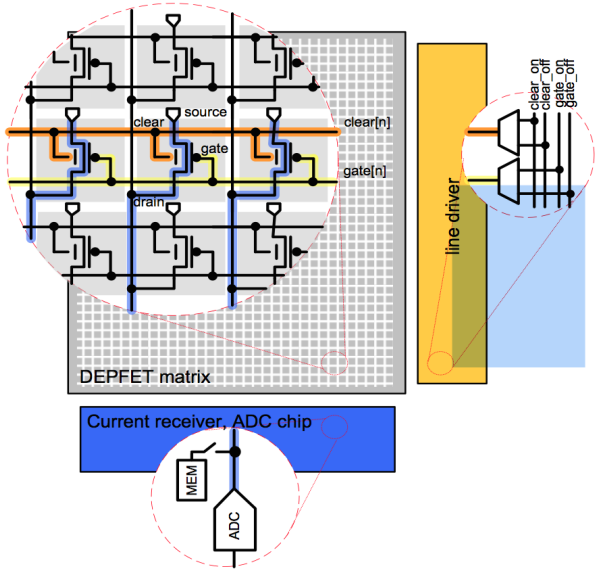


Figure : DEPFET matrix

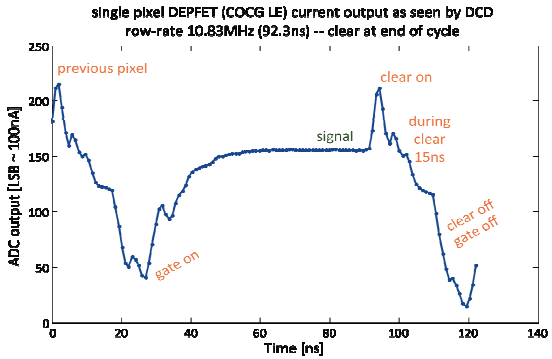
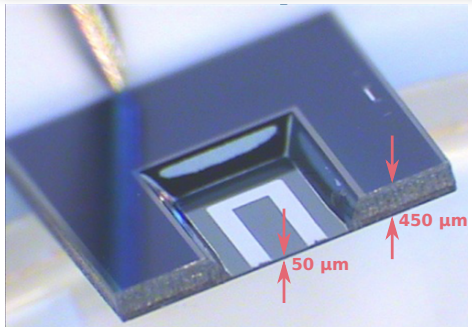
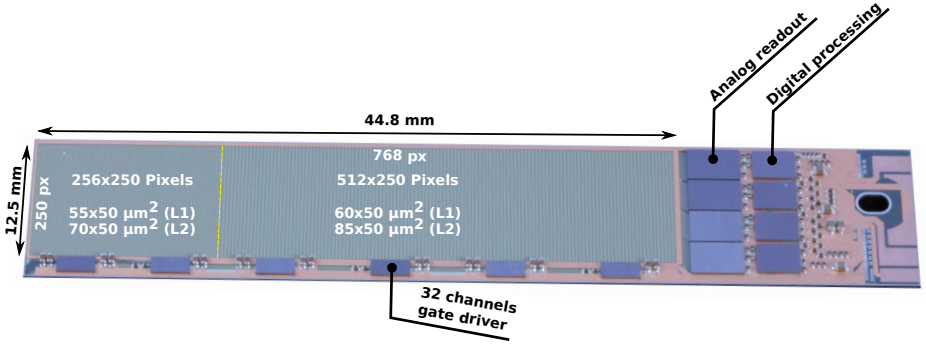


Figure : Drain current during DEPFET read-out cycle

DEPFET Module





Material budget	0.21 % X_0/layer
Spacial resolution	10 μm
Sensitive area	44.8x12.5 mm^2 61.4x12.5 mm^2
Integration time	20 μs/frame
Radiation tolerance	2 Mrad/year

- **Gate driver**
  - ⇒ fast voltage pulses up to 20 V
  - ⇒ 32 channels/ASIC
- **Drain Current Digitizer**
  - ⇒ 8 bit ADC
  - ⇒ 256 channels/ASIC
  - ⇒ pedestal current variation compensation
  - ⇒ data rate: 80 Gb/s
- **Digital Handling Processor**
  - ⇒ pedestal/common mode correction
  - ⇒ zero suppression
  - ⇒ read-out synchronization
  - ⇒ max. occupancy: 3 %
  - ⇒ max. data rate: 1.6 Gb/s

DEPFET Module

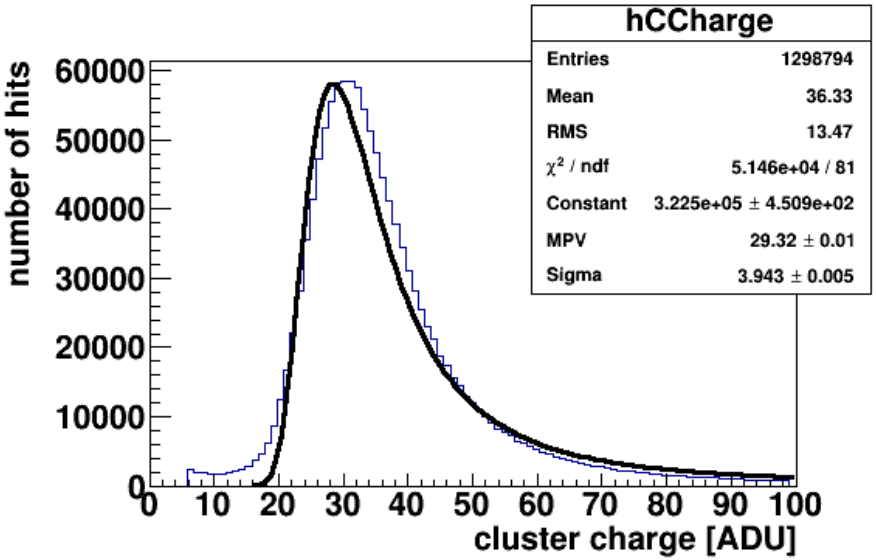


Figure : Cluster charge distribution

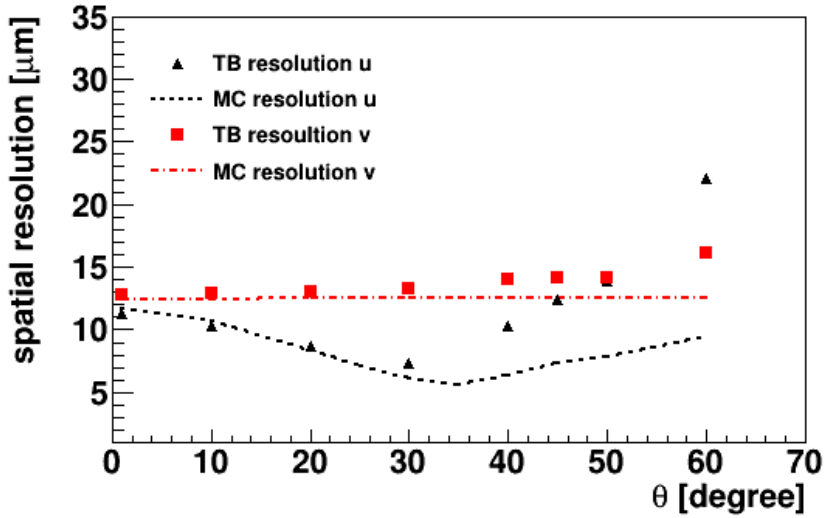
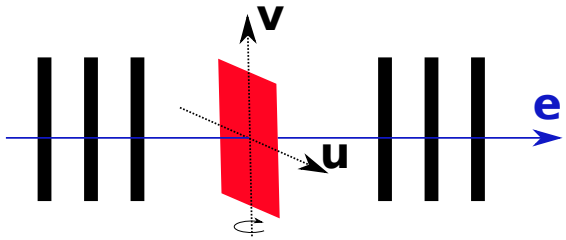


Figure : Resolution of the DEPFET sensor



Detector Modules

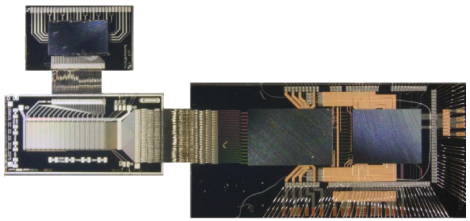


Figure : Hybrid5 module: 64x32 px (2012)

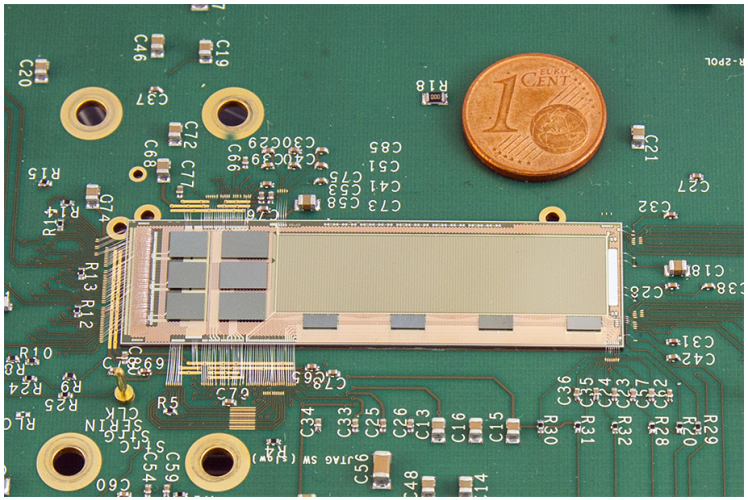


Figure : Hybrid6 module: 480x192 px (2013)

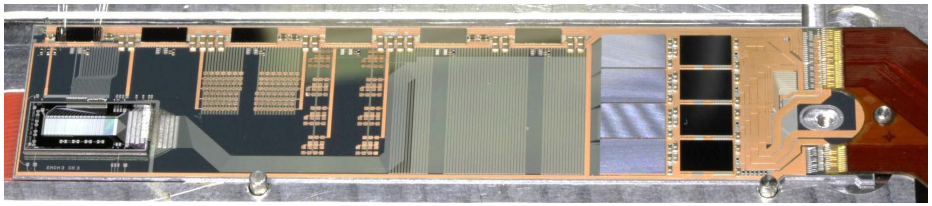


Figure : Electrical Multi Chip Module: electrical prototype (2013)

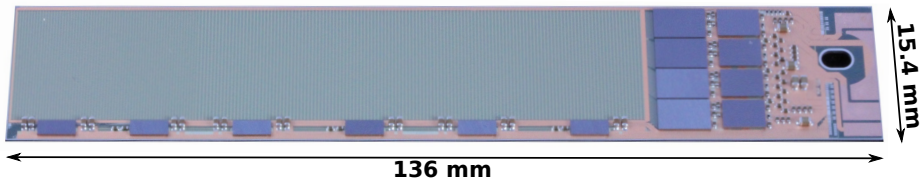
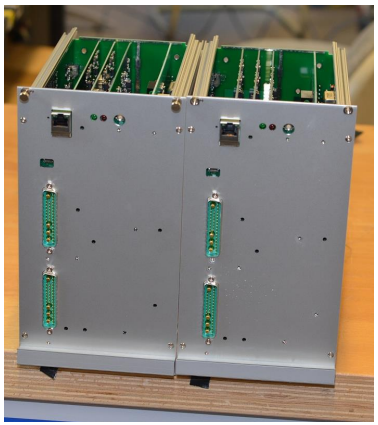


Figure : Belle II half ladder: 768x250 px (2015)

Power Supply and Cooling

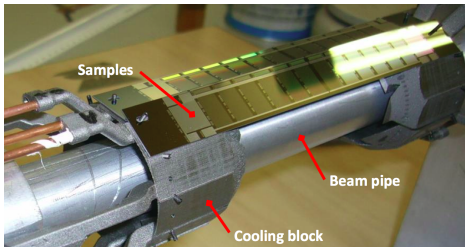
Power supply

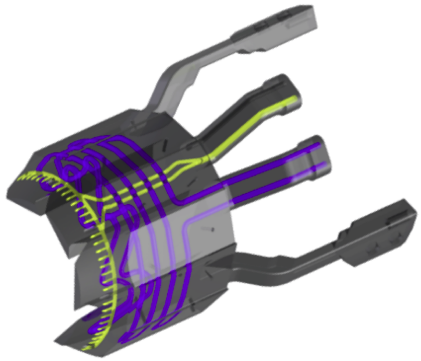
- 18 independent channels
- Transmission of voltages over 15 m cables with high precision
  - ⇒ voltage drop compensation using sense wires
  - ⇒ noise protection
- Sensor protection
  - ⇒ interlock in hardware



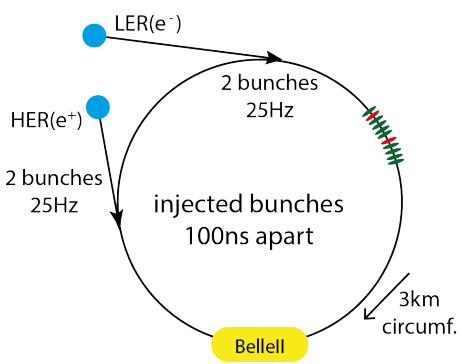
Cooling: IB-Belle

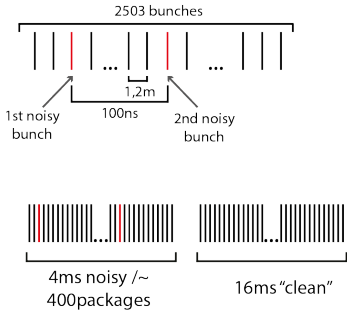
- Common project of ATLAS IBL and Belle II VXD
- Requirements: -20 ^{o}C (SVD)
- Dry CO_2 cooling
- Two independent systems for redundancy



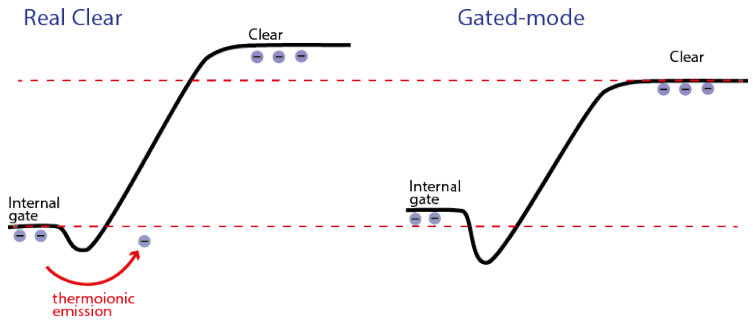


Gated Mode (Intrinsic Electronic Shutter)





- High injection noise increases occupancy
  - ⇒ dead time reduced through intrinsic electronic shutter
- Charge is saved in internal gate during bunch crossing
- No new charge is stored in internal gate
  - ⇒ charge from noisy bunches removed immediately



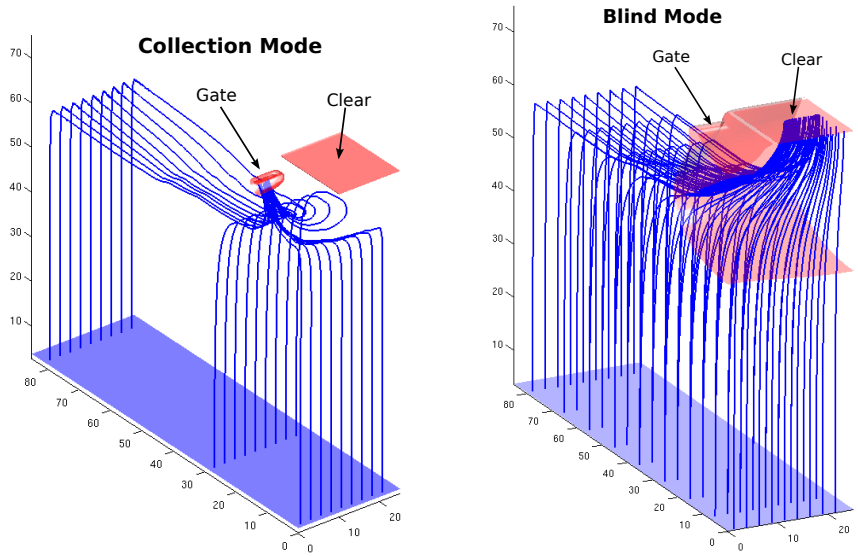
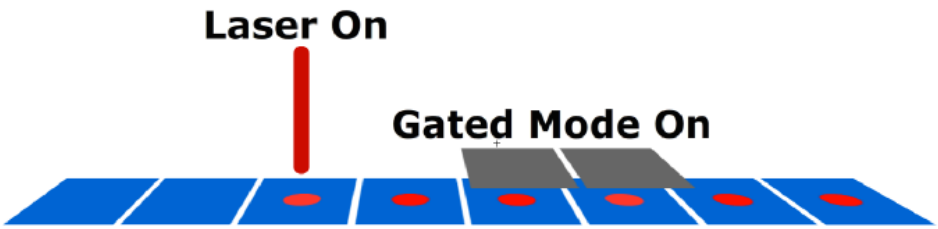
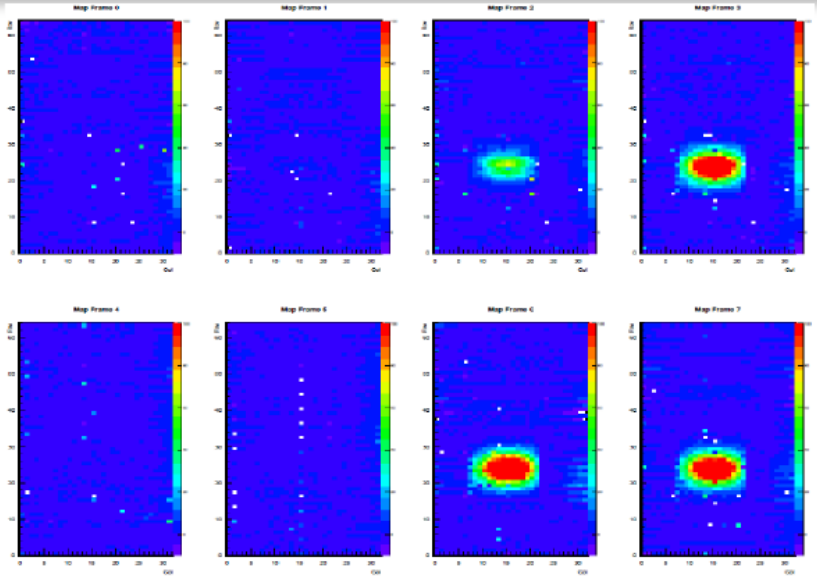


Figure : Simulation of electron trajectories in the detector

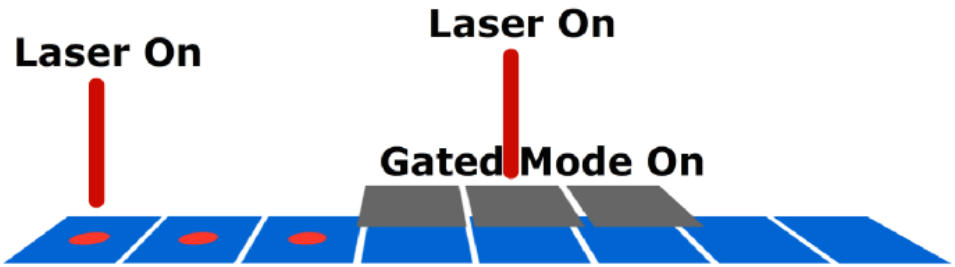
Gated Mode

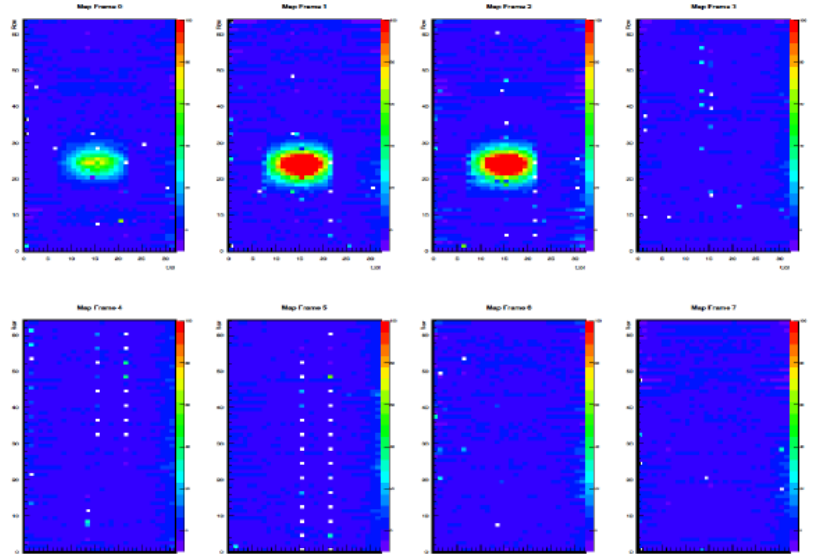
Signal Charge Restore:





Junk Charge Generation:





Read-Out Topology

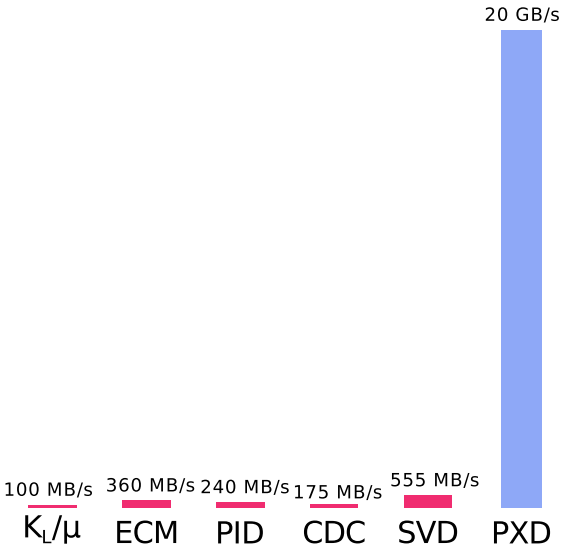
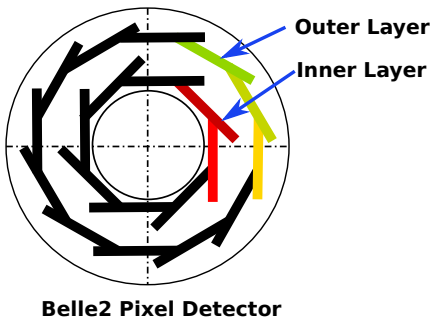


Figure : Data rates in Belle II



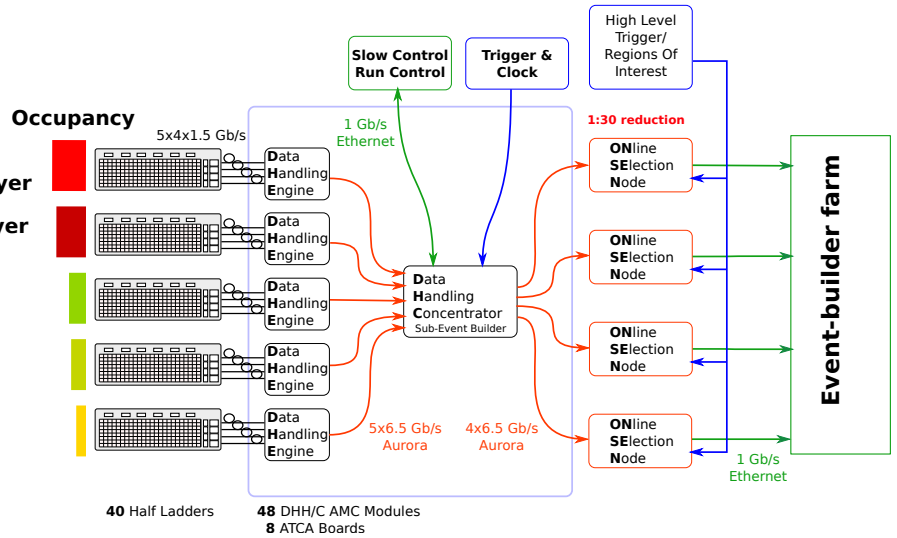


Figure : Data read-out chain

Data Handling Engine

- Data read out
- Detector control
- Cluster reconstruction
- $\frac{\partial E}{\partial x}$ analysis

Data Handling Concentrator

- Sub-event building
  - $\Rightarrow$ data rate averaging
- Trigger distribution
- Slow control distribution

Online Data Reduction

Figure : FPGA-based online data reduction algorithm

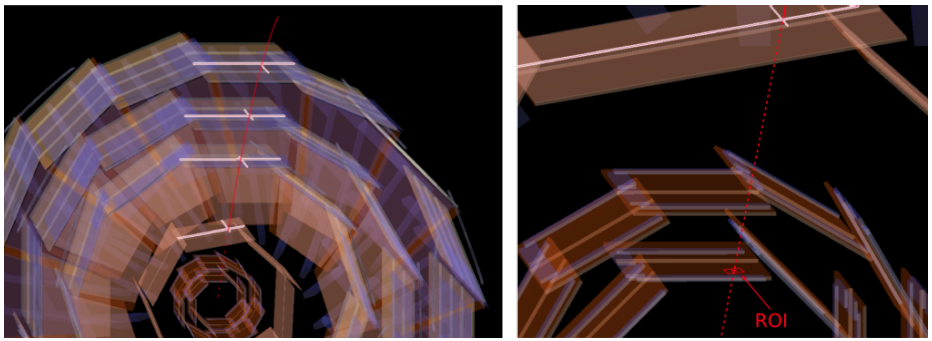


Figure : ROI calculation

- High-level trigger (HLT)
  - ⇒ online event analysis
  - ⇒ uses common Belle II analysis framework
- Regions of interest (ROI)
  - ⇒ HLT and FPGA-based SVD-only tracker
  - ⇒ calculated using Hough transform
- Online data reduction
  - ⇒ reject events without HLT
    - → data reduction by factor 10
  - ⇒ remove pixels unrelated to ROI
    - → data reduction by factor 3

Online Data Reduction

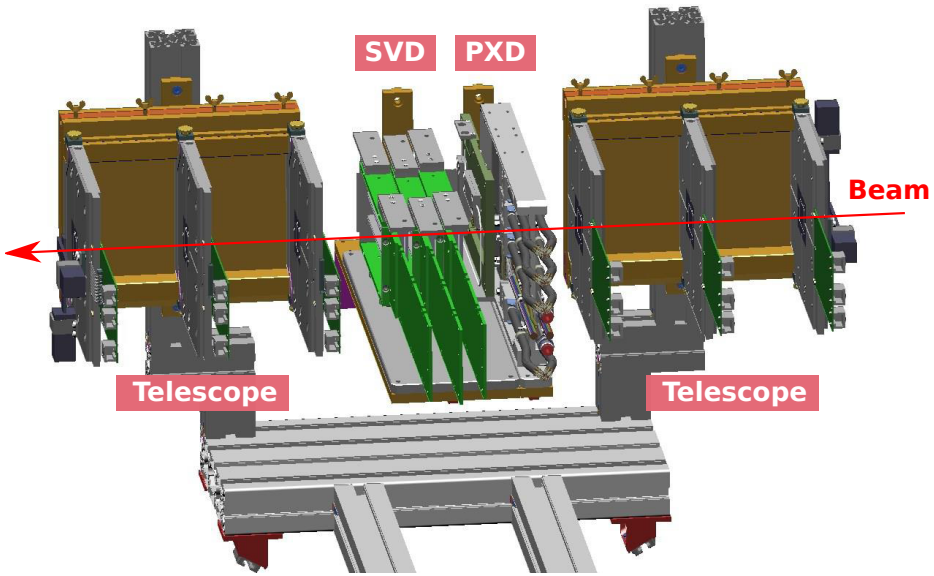


Figure : Beam test setup with a VXD segment, DESY 2014

- High-level trigger (HLT)
  - ⇒ online event analysis
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  - ⇒ HLT and FPGA-based SVD-only tracker
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Online Data Reduction

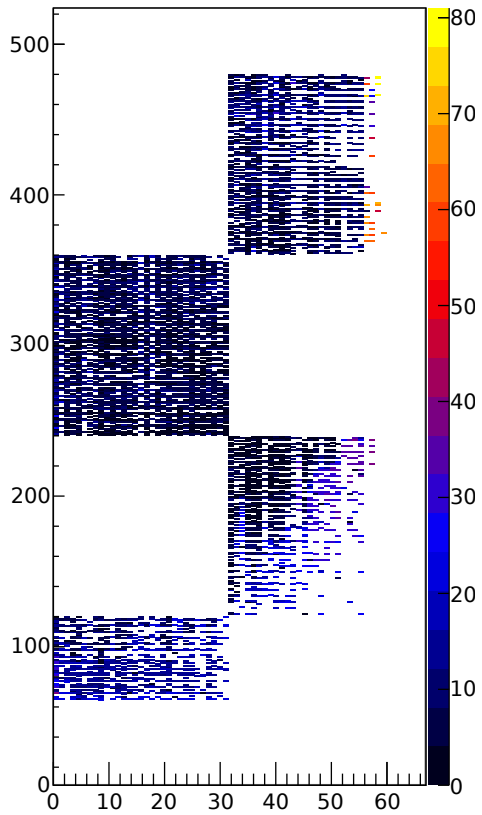

Figure : Data reduction using artificial pattern

- High-level trigger (HLT)
  - ⇒ online event analysis
  - ⇒ uses common Belle II analysis framework
- Regions of interest (ROI)
  - ⇒ HLT and FPGA-based SVD-only tracker
  - ⇒ calculated using Hough transform
- Online data reduction
  - ⇒ reject events without HLT
    - → data reduction by factor 10
  - ⇒ remove pixels unrelated to ROI
    - → data reduction by factor 3

Slow Pions Recovery Using $\frac{\partial E}{\partial x}$

- High stopping power for low momentum particles
- Neural network for recovering slow pions that do not reach other detectors ($p_t < 60 MeV/c^c$)
  - **teacher** in software on a data set
  - **expert** in FPGA
- Classification uses cluster shape and charge deposition
- Pipelined cluster processing

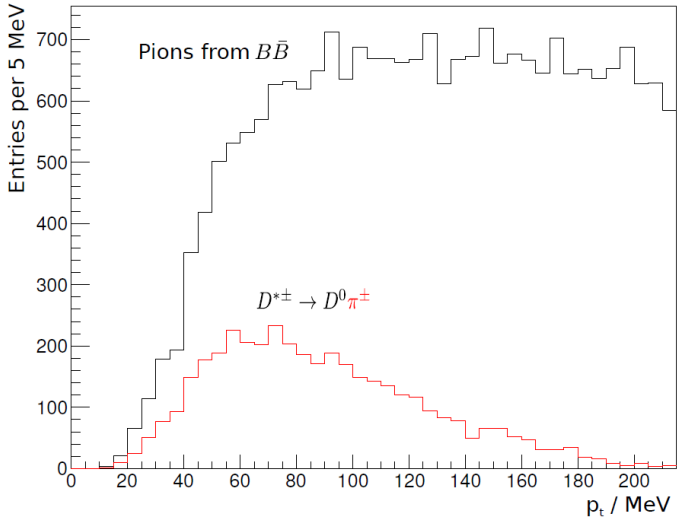

Figure : Transverse momentum distribution of pions from $D^{*\pm}$ and $B\bar{B}$ decays

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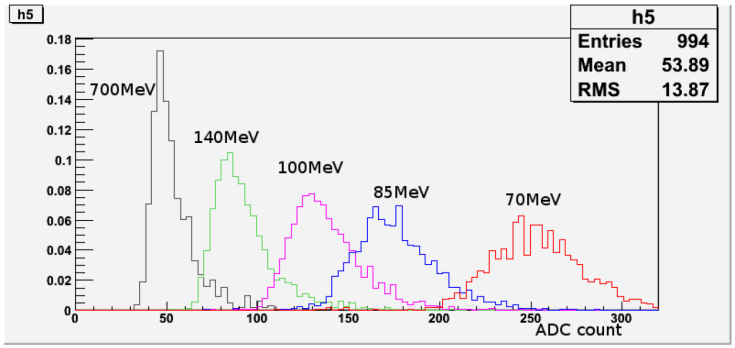

Figure : Pions energy deposition in PXD

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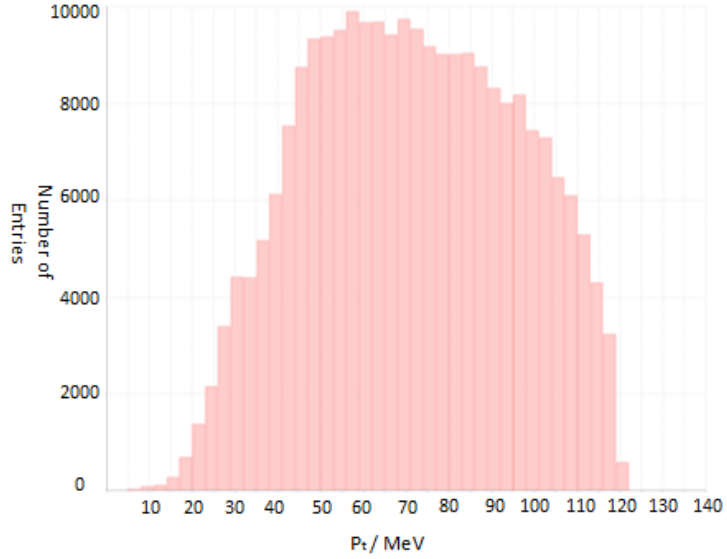

Figure : Neural network training sample including background

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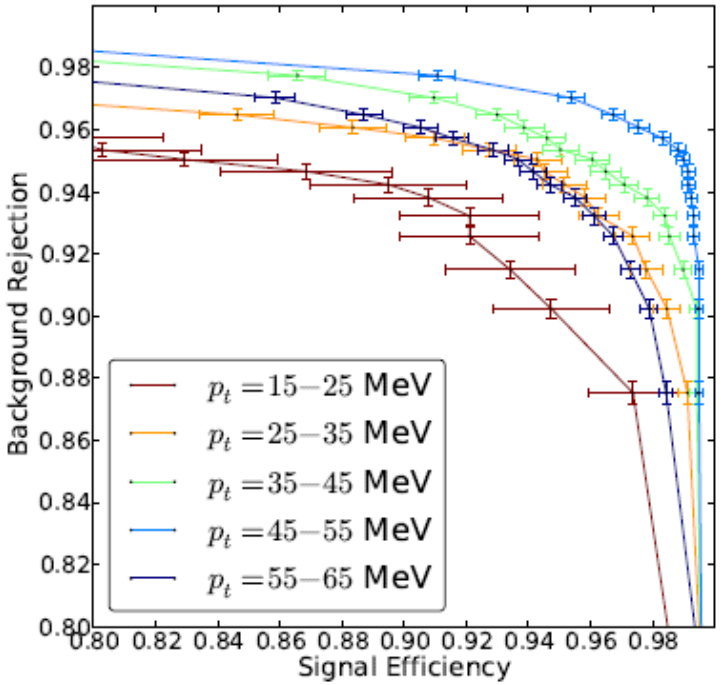


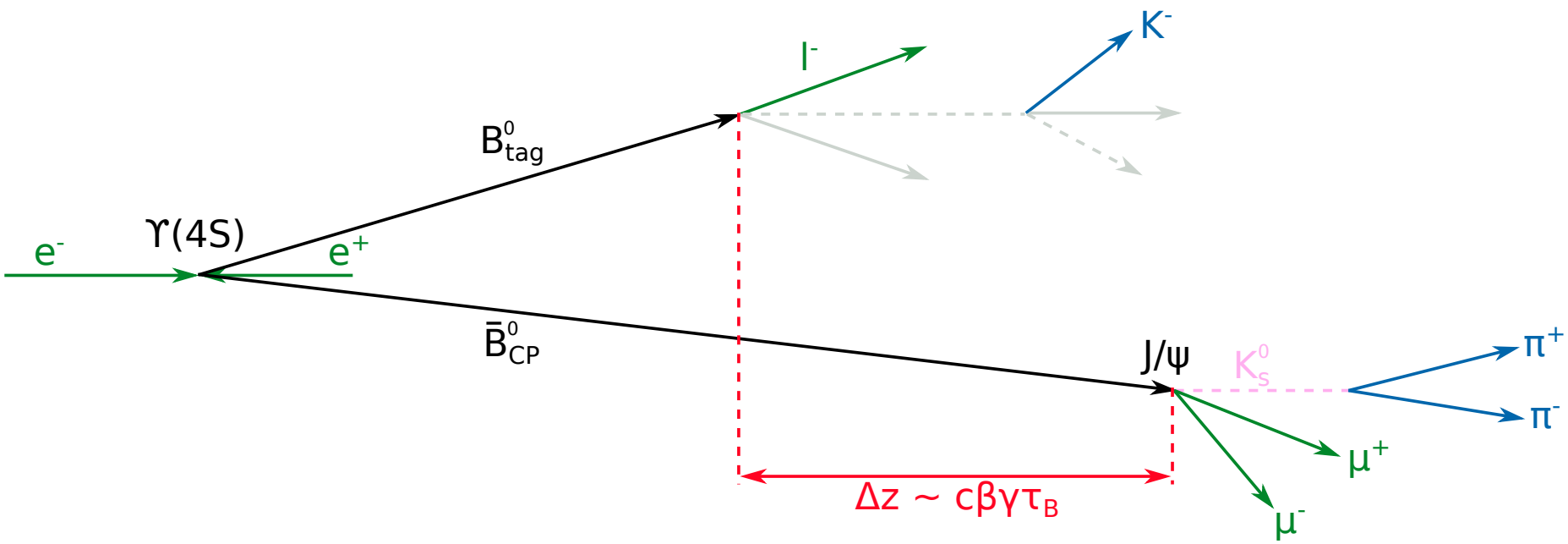
Figure : Efficiency in pion recovery and background rejection

Conclusions

- We developed a pixel detector that fits the requirements of Belle II
- We successfully proved the concept of data reduction in 2014
- Full sector of VXD will be tested in April 2016 at DESY
- Final production of half-ladders is being prepared
- Gated mode will be optimized to Belle II conditions with SuperKEKB input

Thank You!

Backup



	E, GeV	$\beta\gamma$	Δz, μm
Belle	8 - 3.5	0.42	200
Belle II	7 - 4	**0.28**	**130**