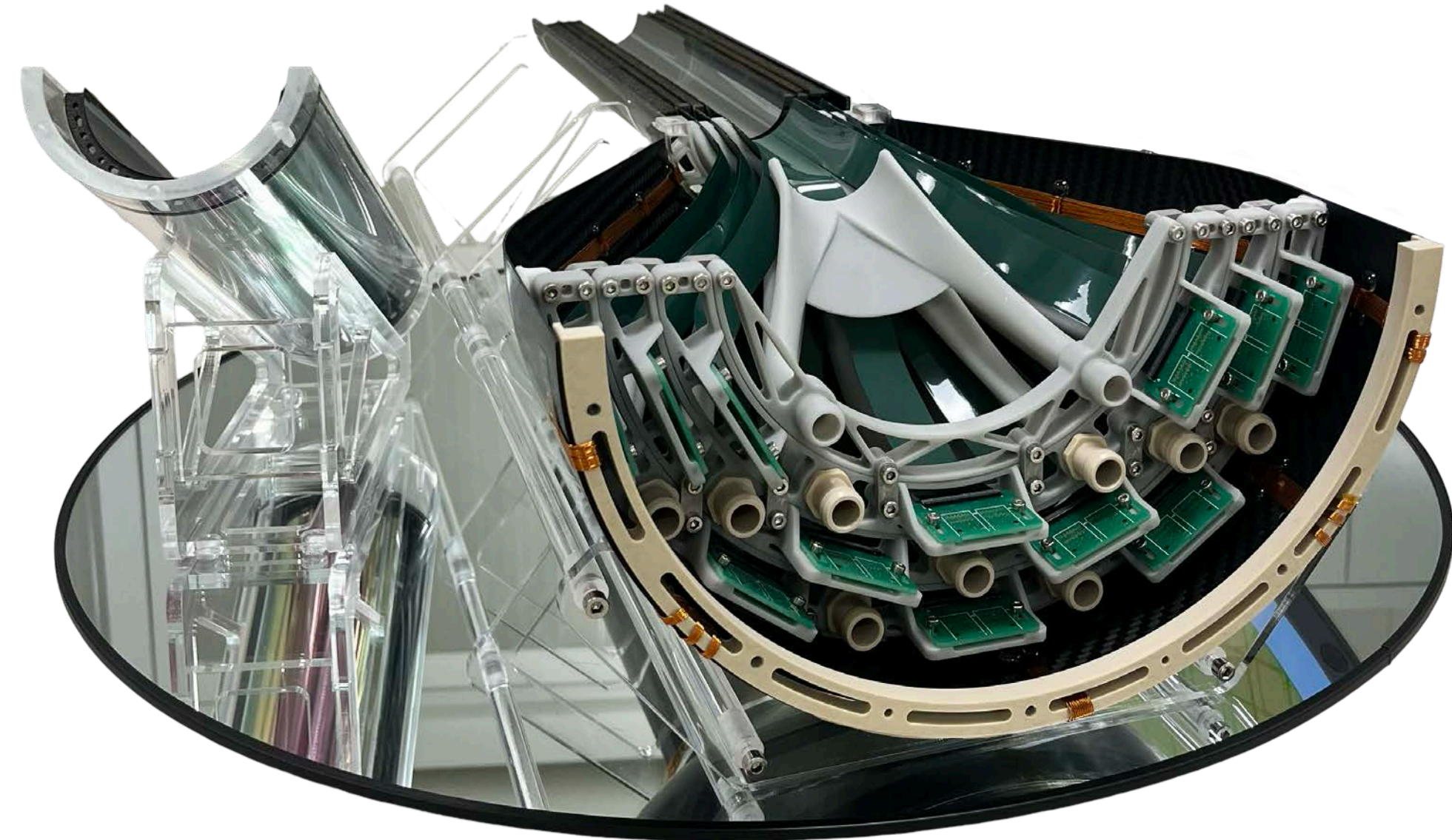
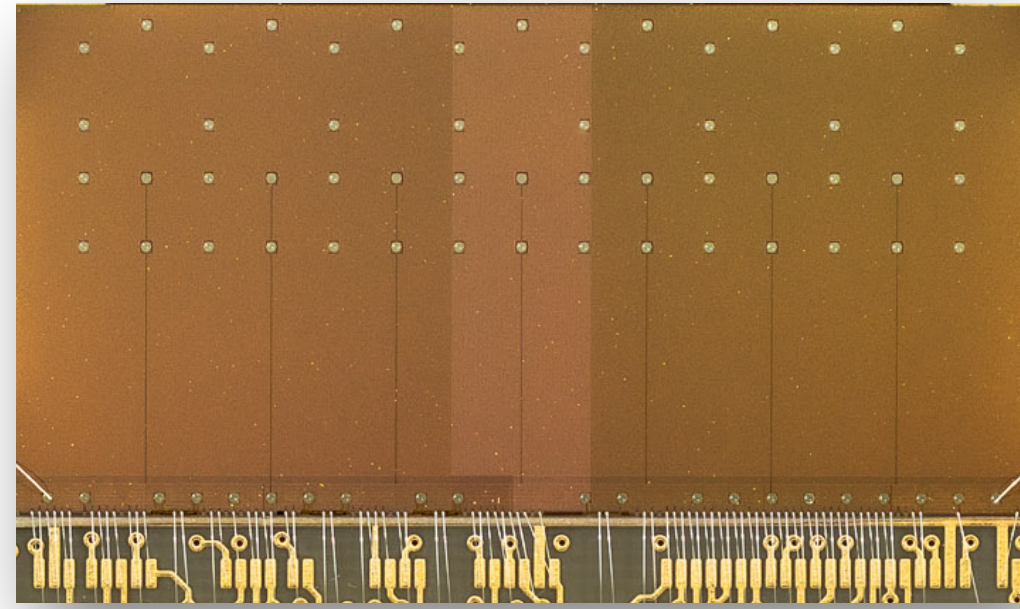
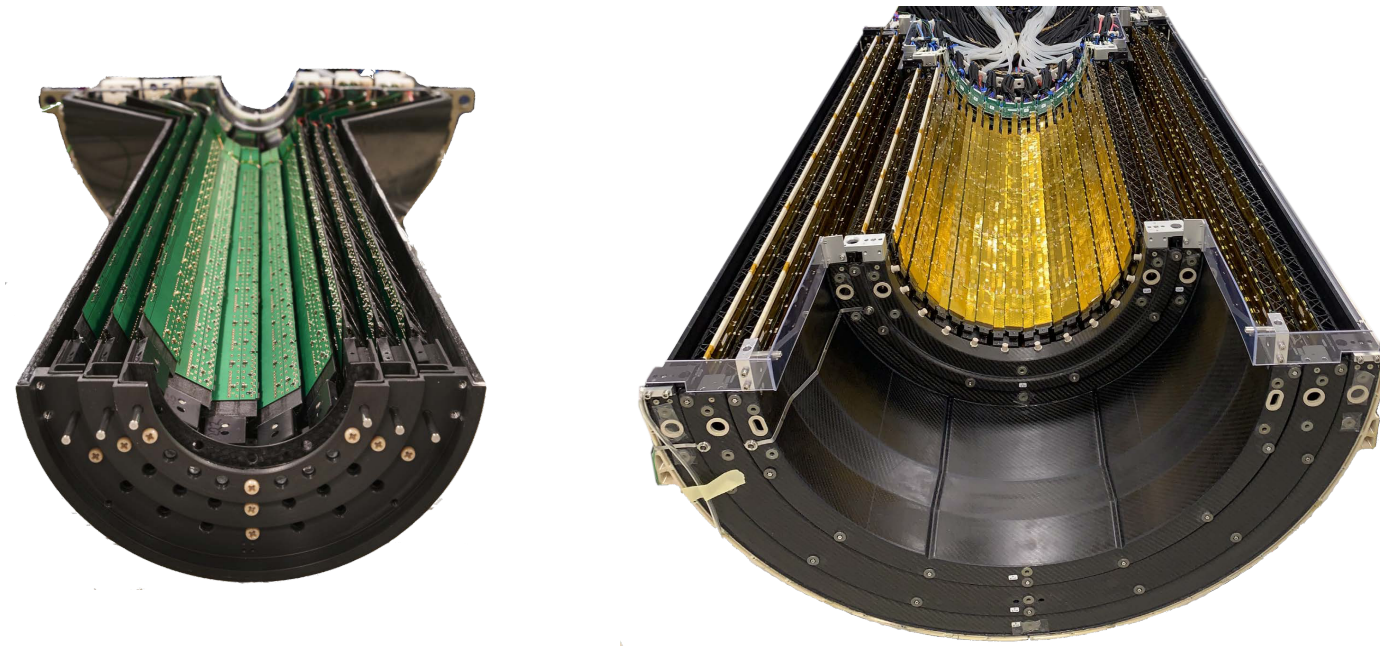
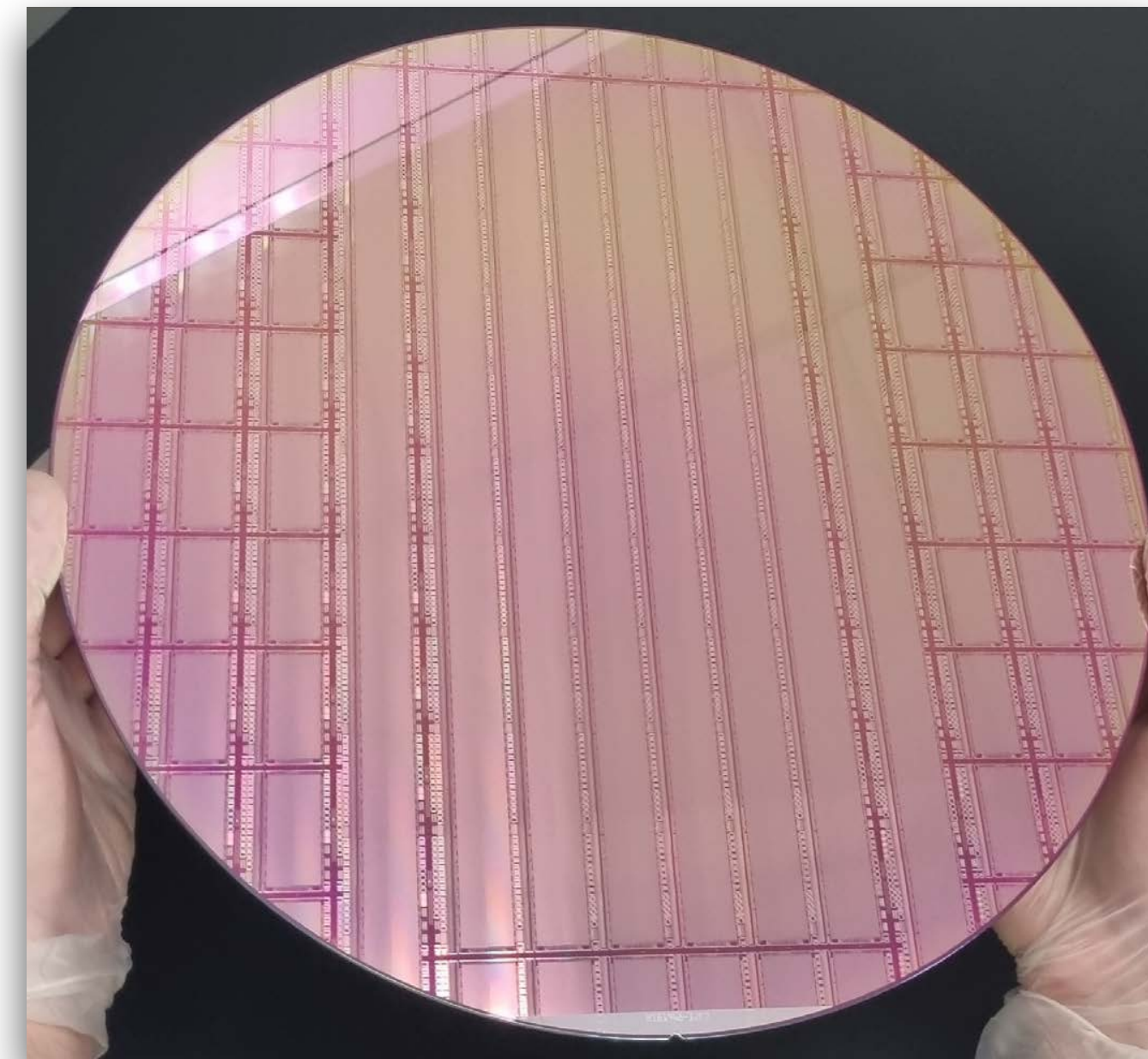
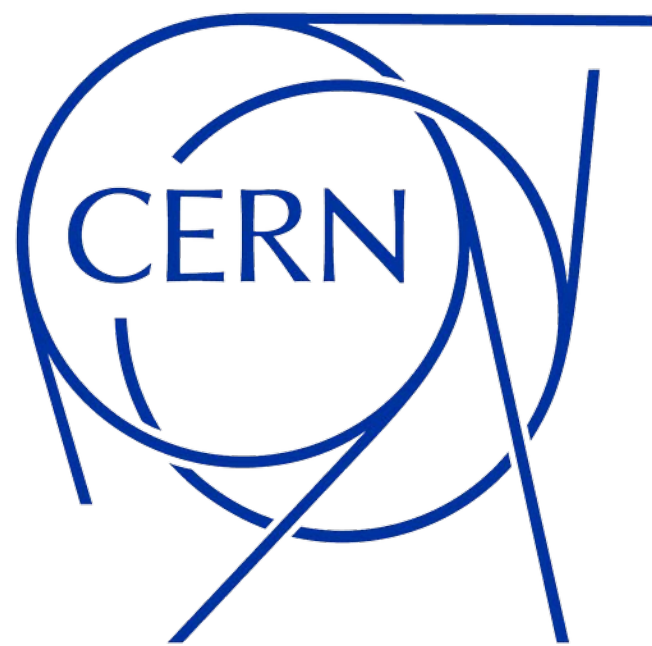




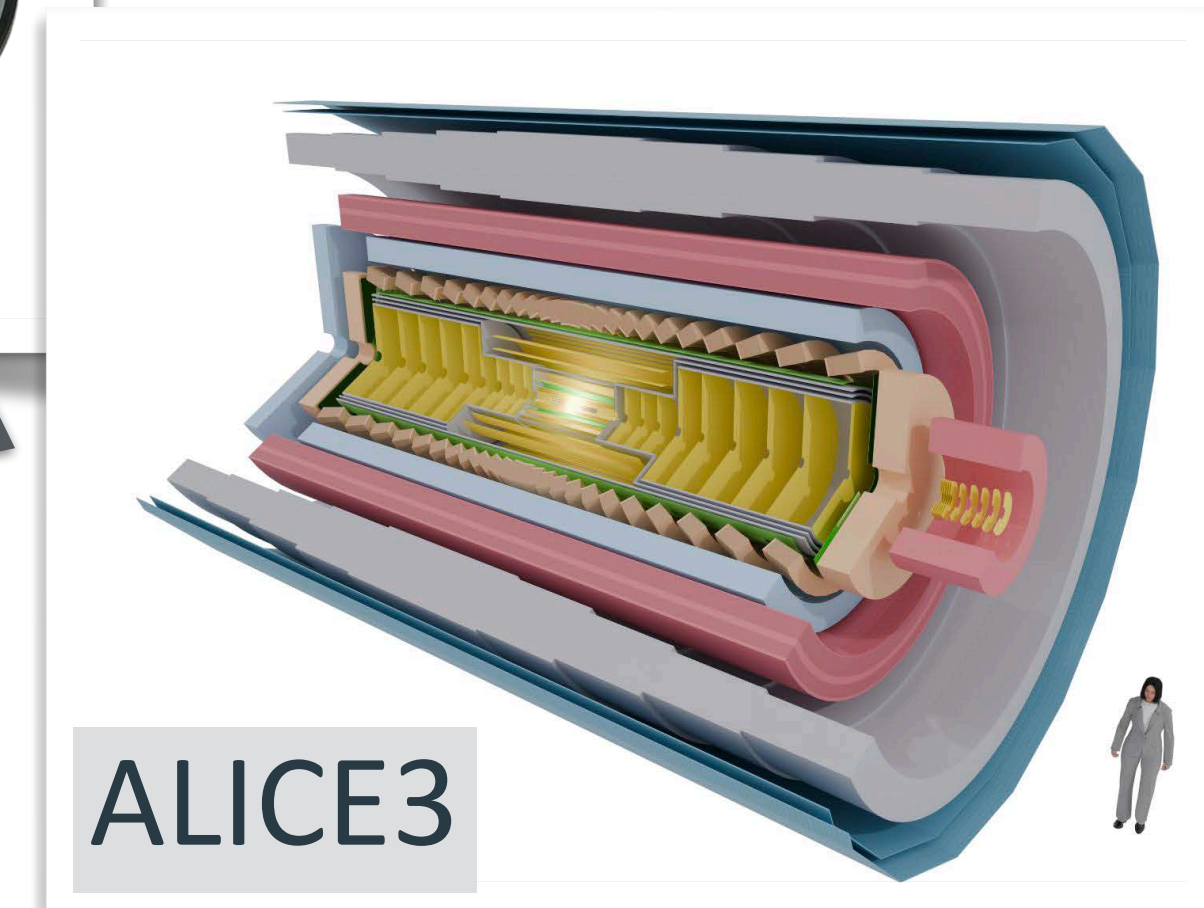
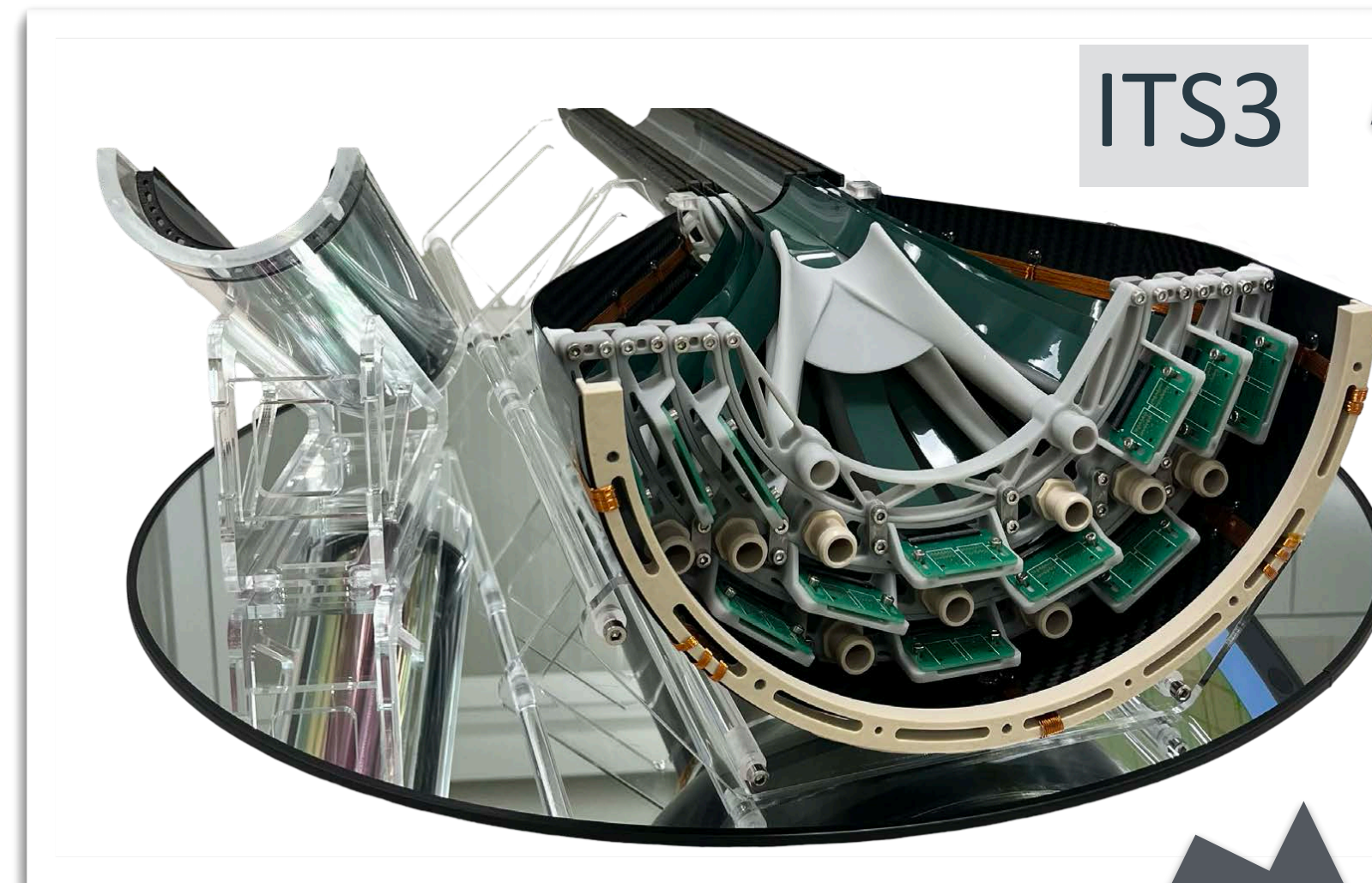
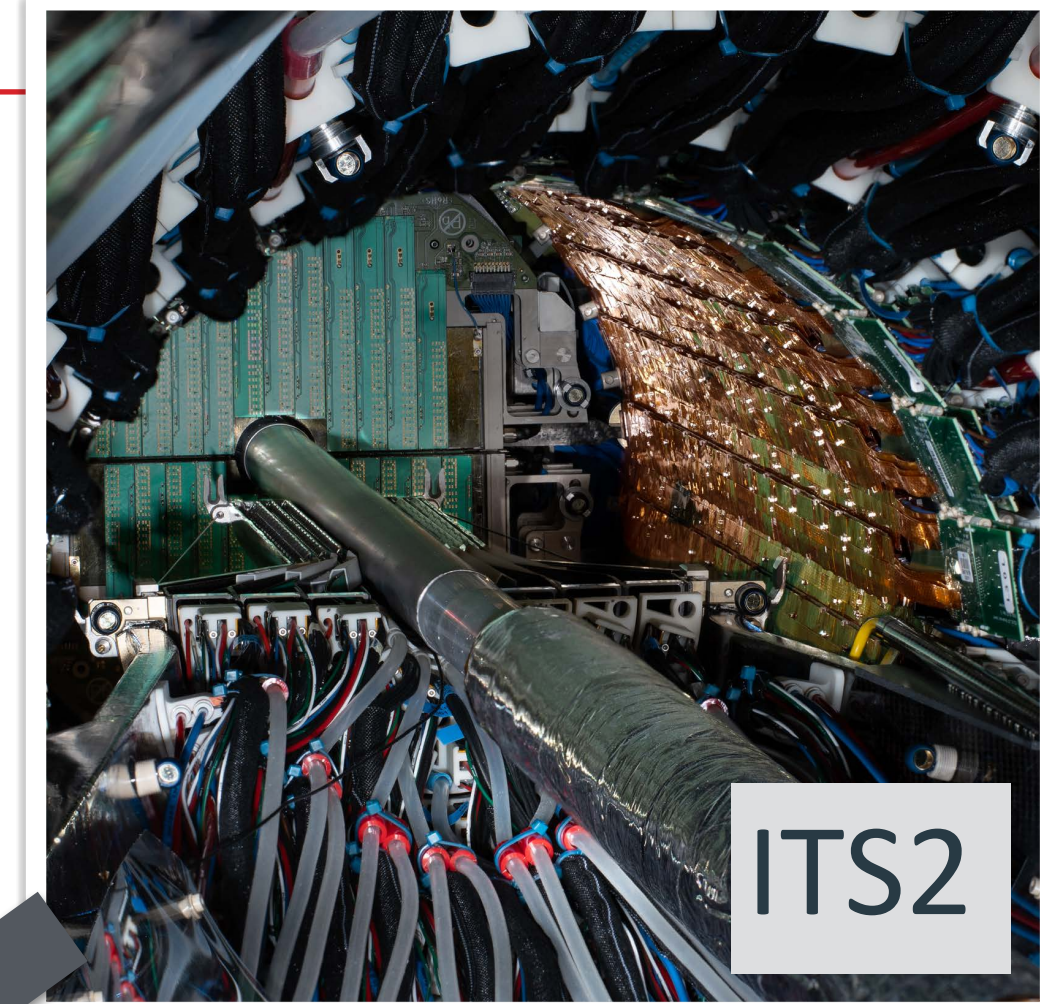
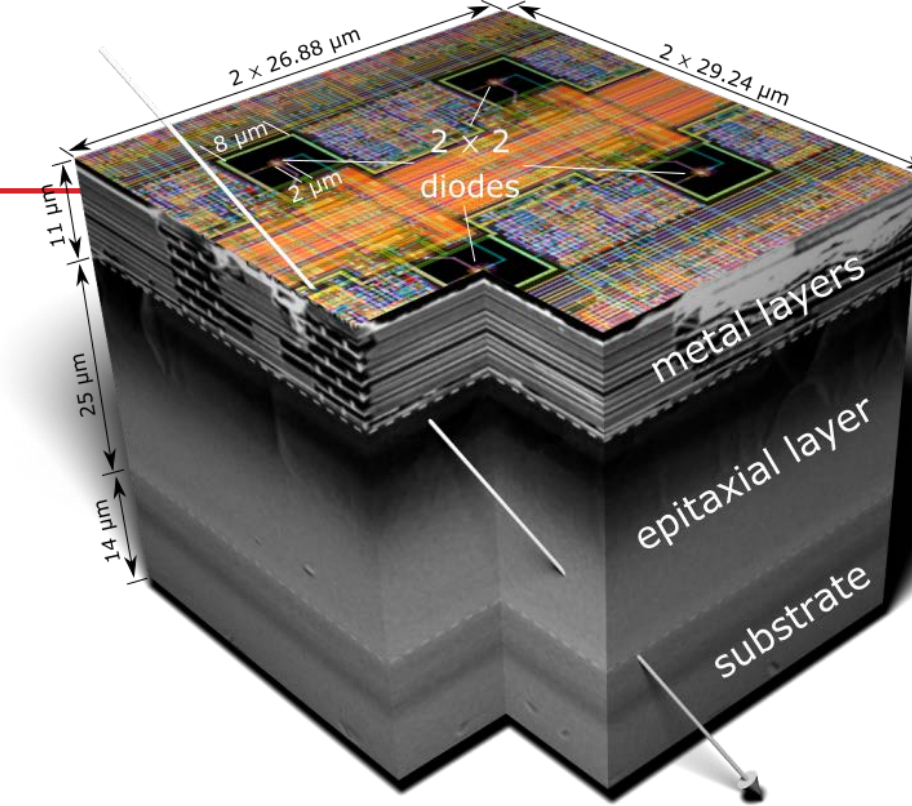
CMOS Pixel Sensors in ALICE

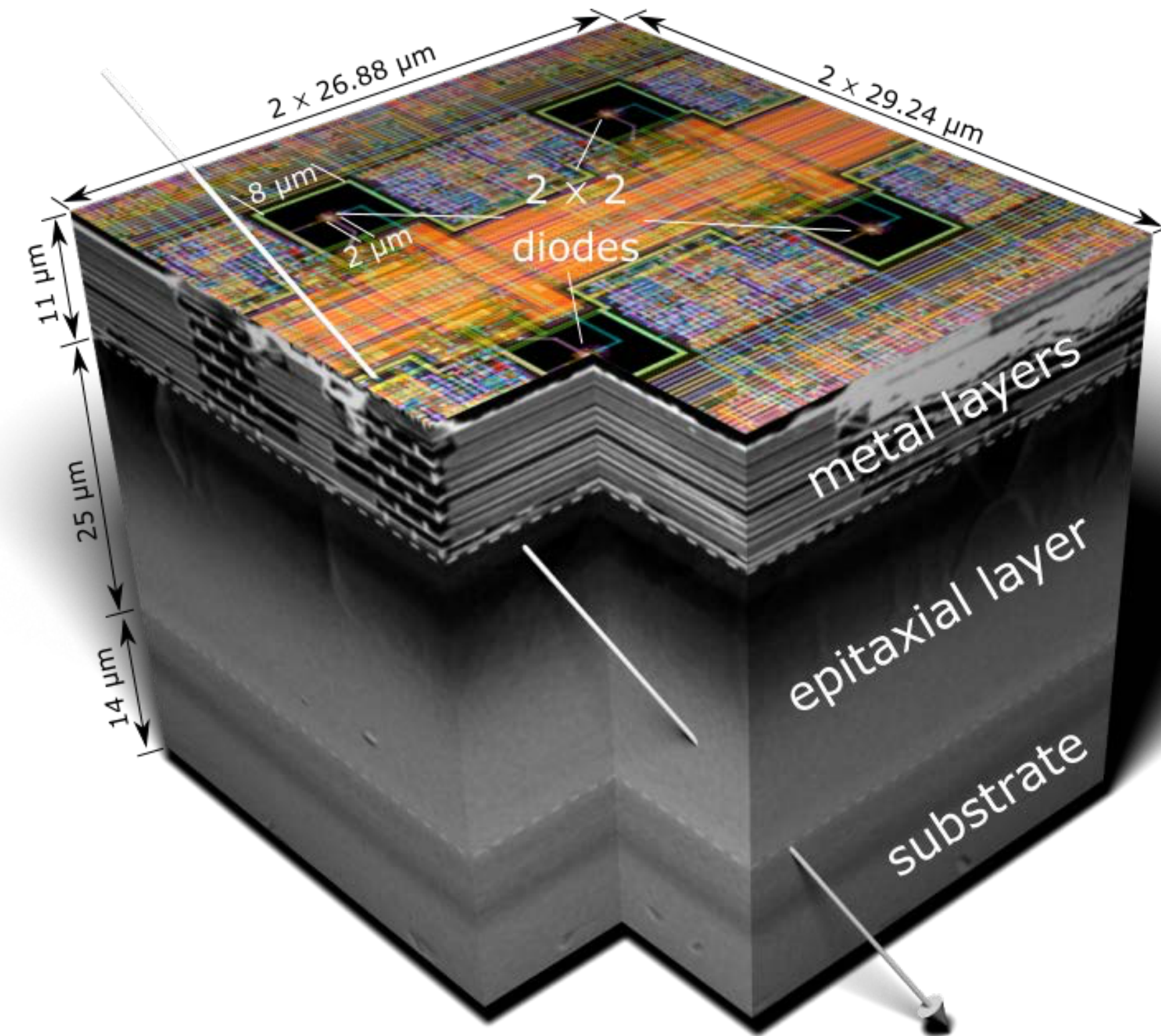
Felix Reidt
on behalf of the ALICE collaboration



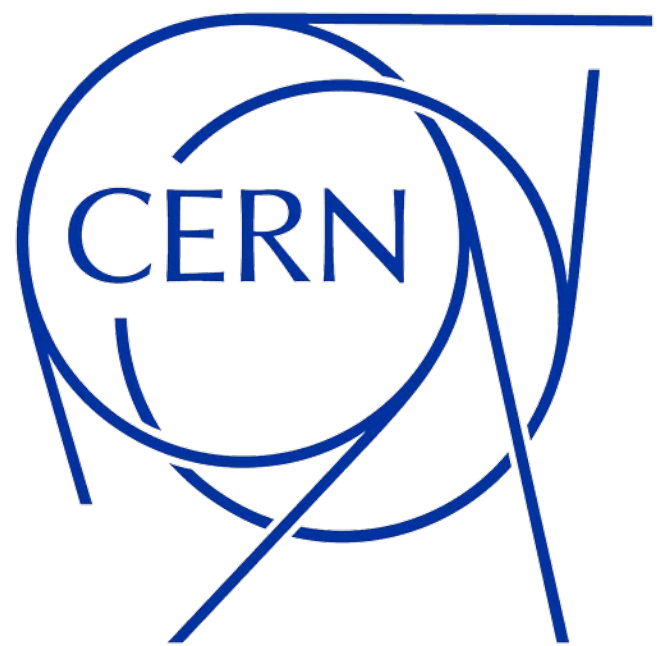
Outline

- Introduction to CMOS Pixel Sensors
- Inner Tracking System 2 (ITS2)
- Inner Tracking System 3 (ITS3)
- ALICE 3
Vertex Detector
and Tracking Detectors





Introduction to CMOS Pixel Sensors



Pixel detectors

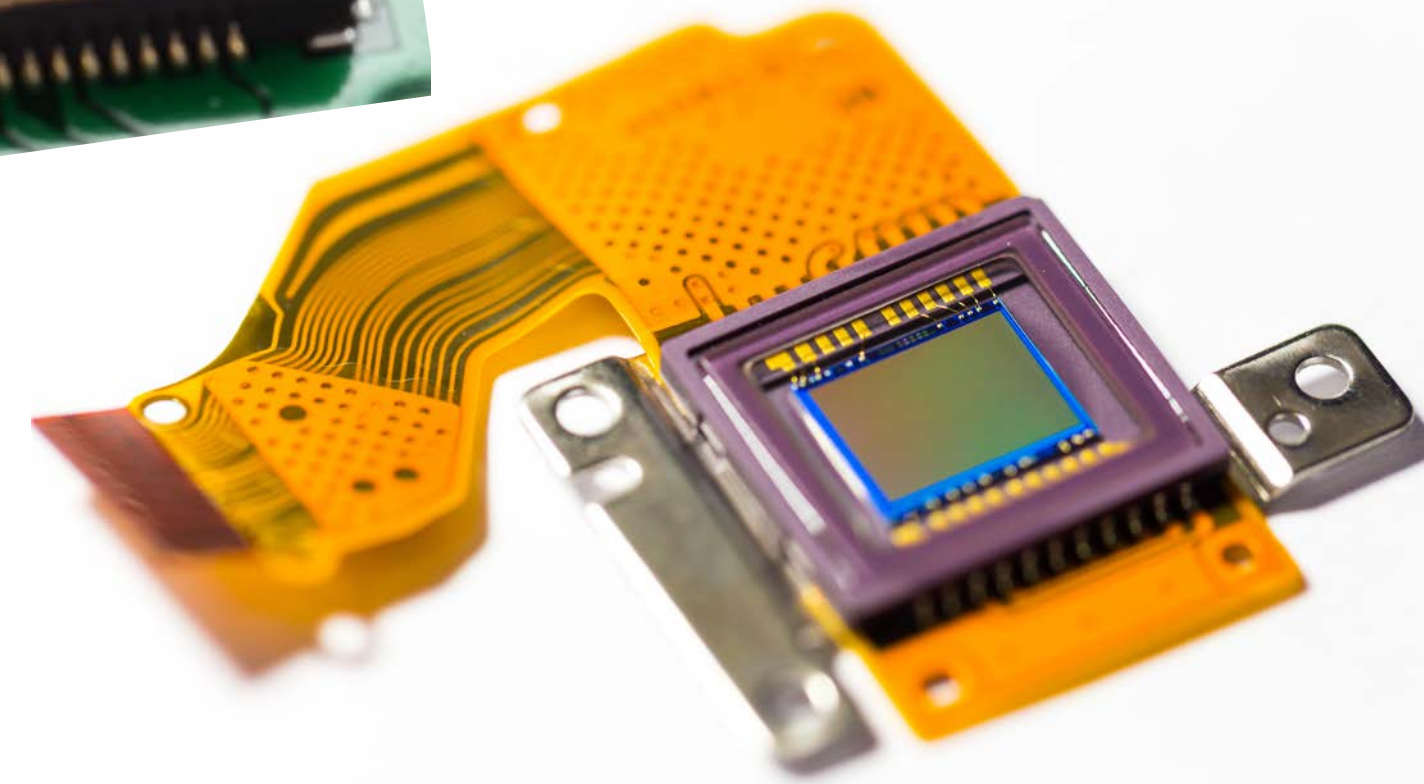
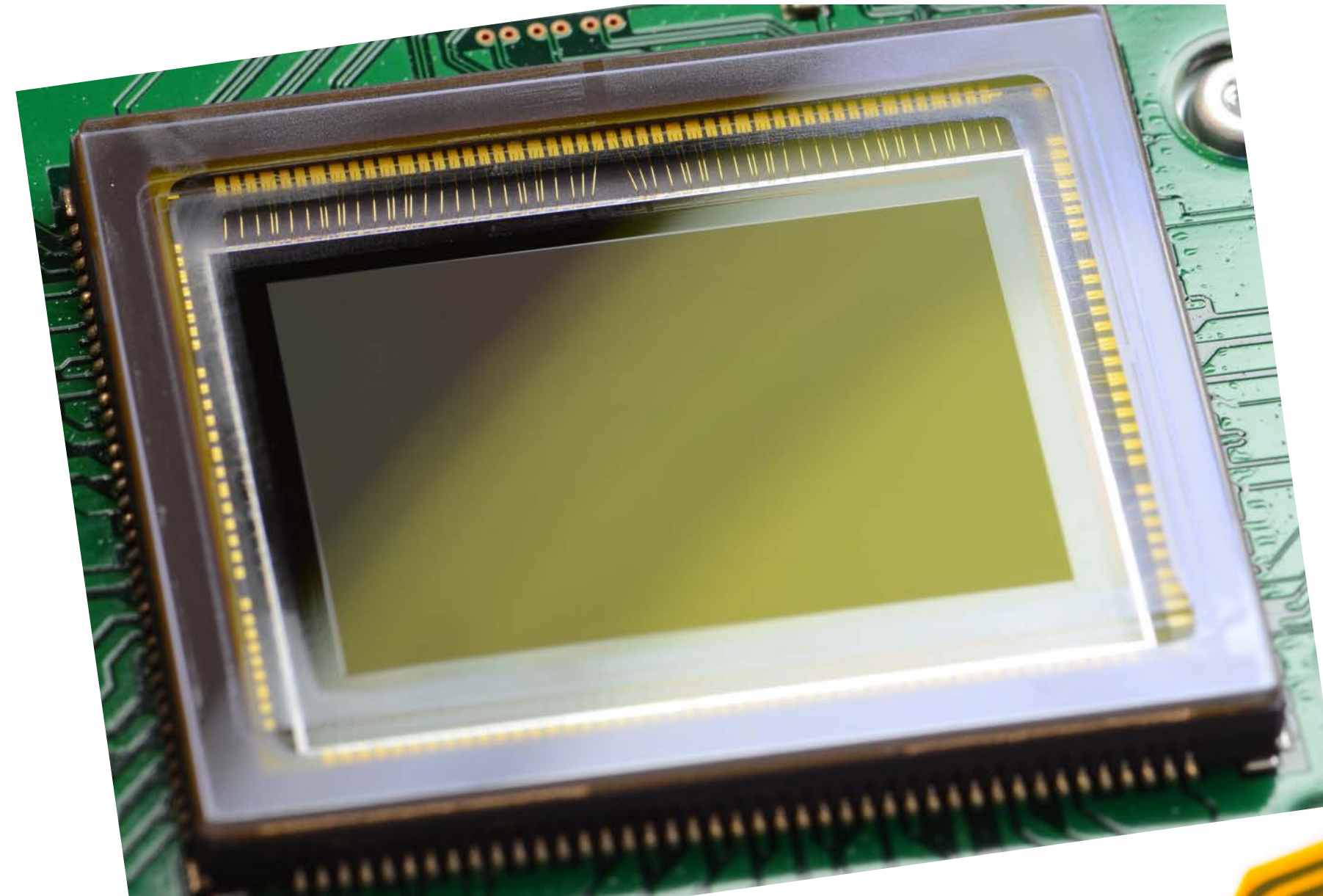
... are nowadays present everywhere



Nobel Prize in Physics 2009

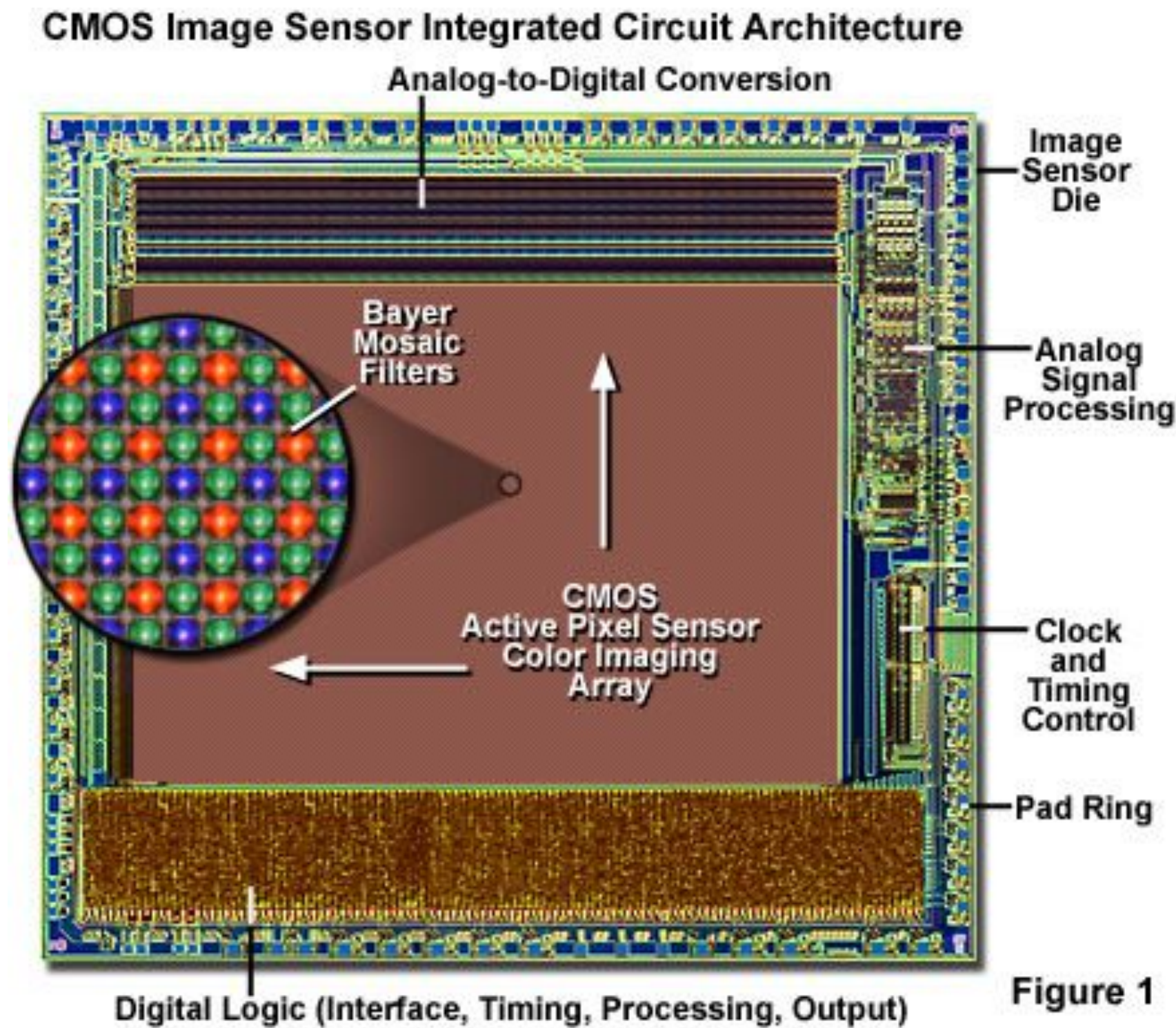
Willard S. Boyle and George E. Smith

"for the invention of an imaging semiconductor circuit – the CCD sensor."



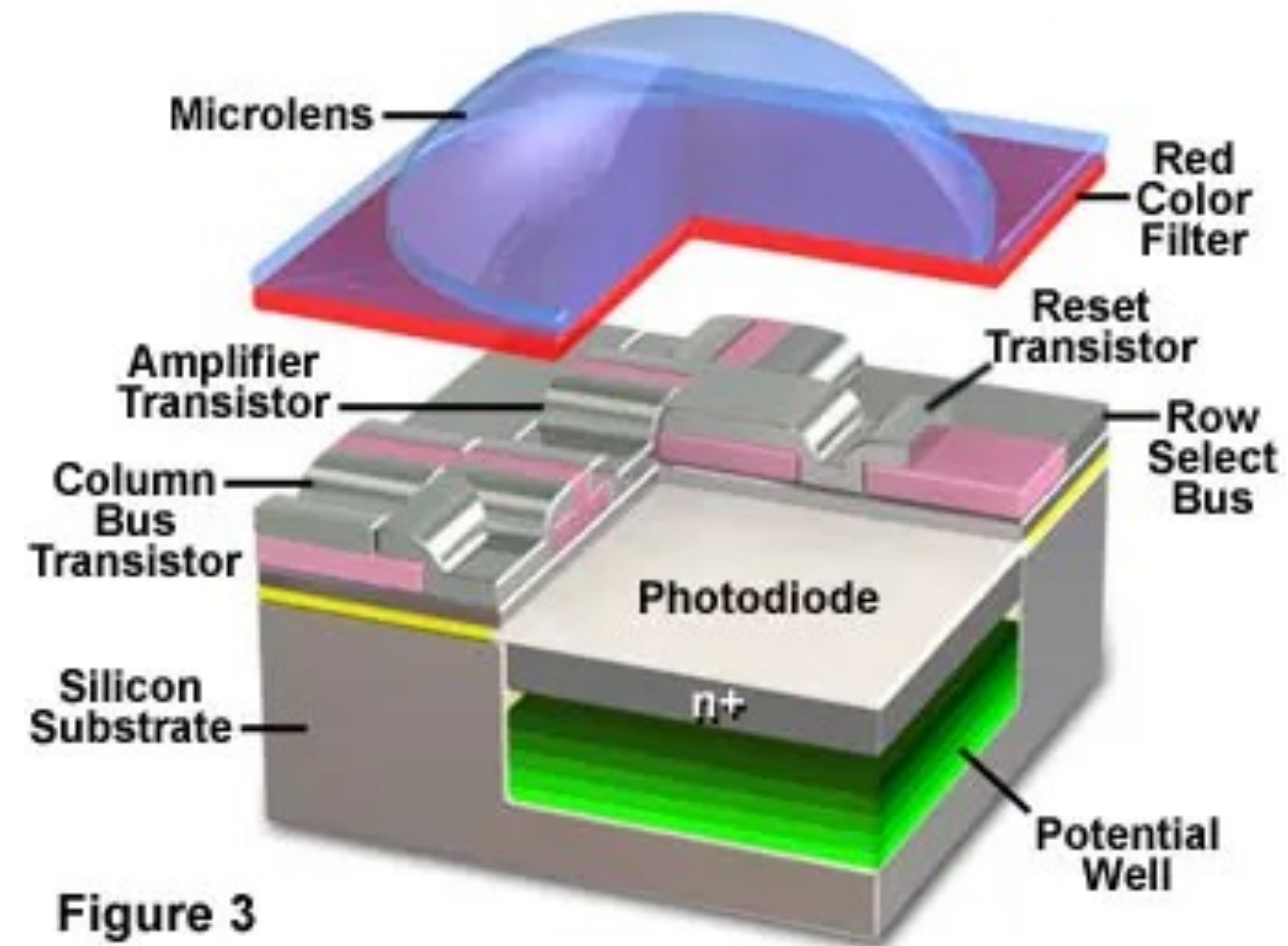
Pixel detectors are abundant, e.g. in digital cameras (top left) smartphones (bottom right), portable computers, surveillance, etc.
though mostly for (visible) light

CMOS Image Sensors



- Nowadays the most widespread implementation of image sensors
 - Main advantage: price

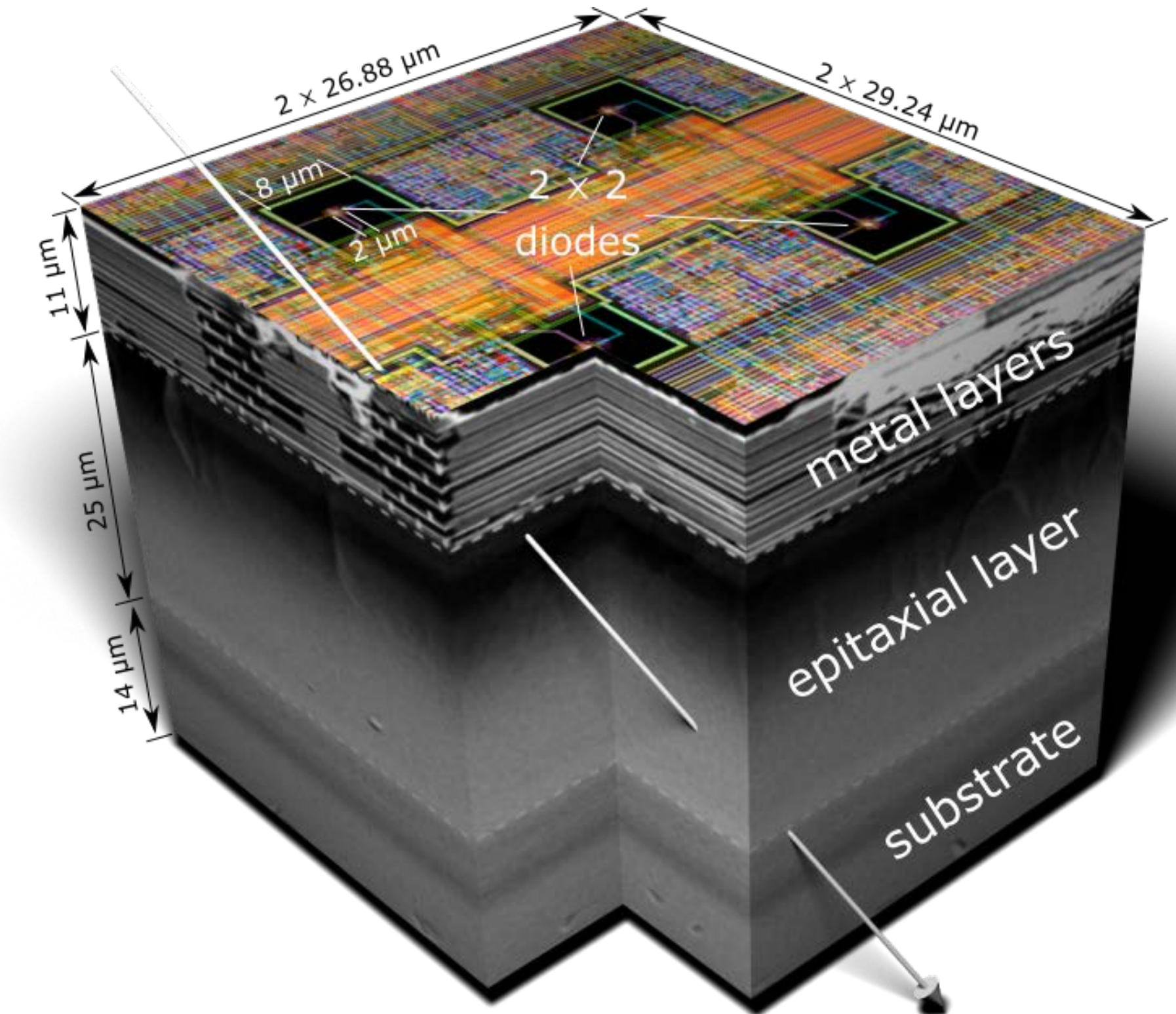
Anatomy of the Active Pixel Sensor Photodiode



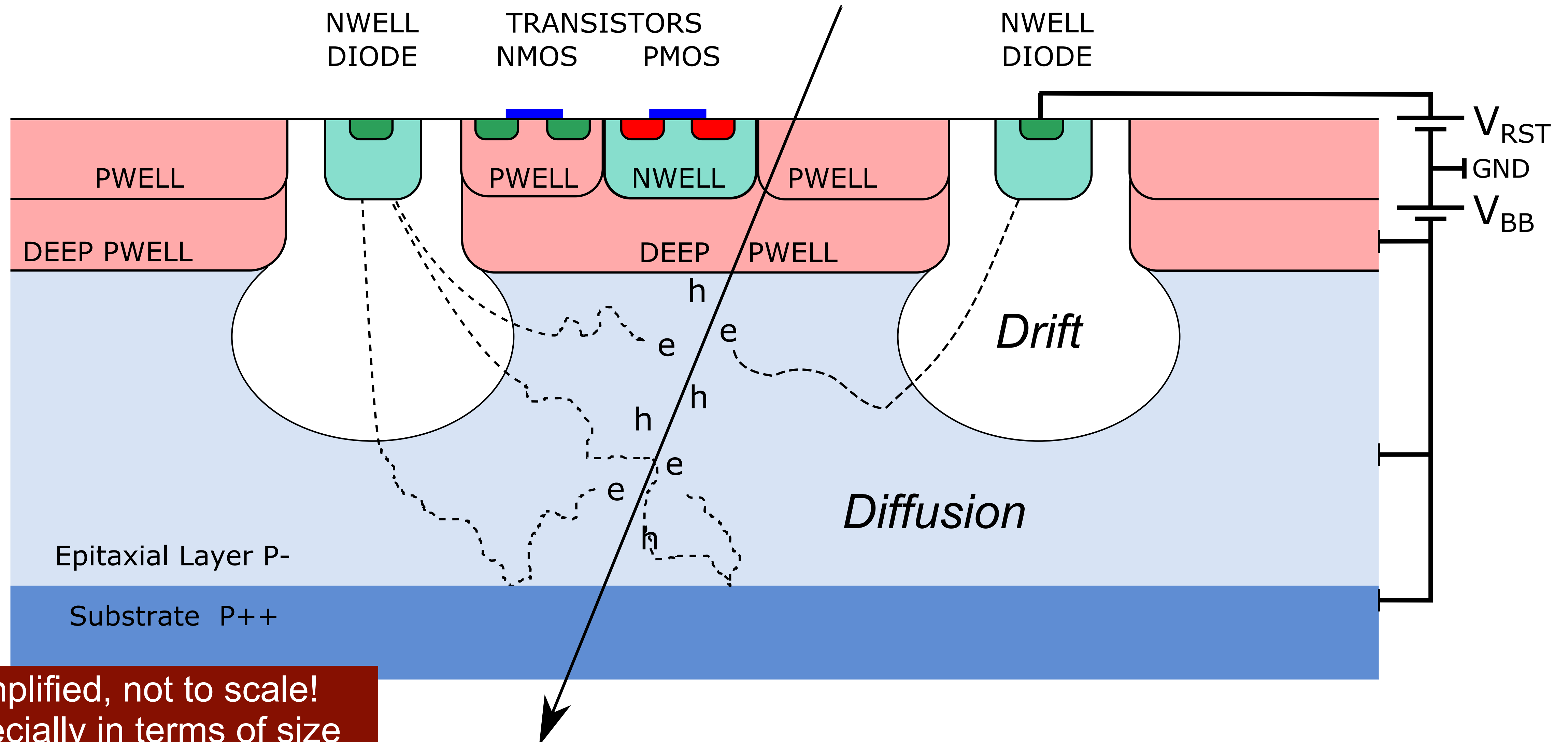
- CMOS pixel structure
 - Microlens focusing light on to sensitive area
 - Color filter
 - Few transistors

CMOS pixel sensors for charged particle detection

- Using the same (or similar) CMOS manufacturing process as CMOS Imaging Sensors
 - Light and charged particles produce electron hole pairs
- Single silicon chip can contain both the detection volume and the readout electronics
 - As opposed to hybrid pixel sensors, which use two chips that need to be interconnected
- Design differences compared to imaging sensors:
 - Larger pixels: $O(10\ \mu\text{m})$ vs. $O(1\ \mu\text{m})$
 - Necessity to achieve 100% sensitive area
 - More complex in-pixel circuitry $O(100)$ transistors vs. few transistors
 - Not using optical components (color filters, micro lenses)
 - No need for single photon efficiency
- Advantages compared to hybrid pixel detectors:
 - small pixel pitches: $O(10\text{-}30\ \mu\text{m})$
 - very low capacitances = low power consumption $O(10\text{-}100\ \text{mW}/\text{cm}^2)$
 - thin: $<50\ \mu\text{m}$ ($\sim 0.05\% X_0$)
 - commercial process

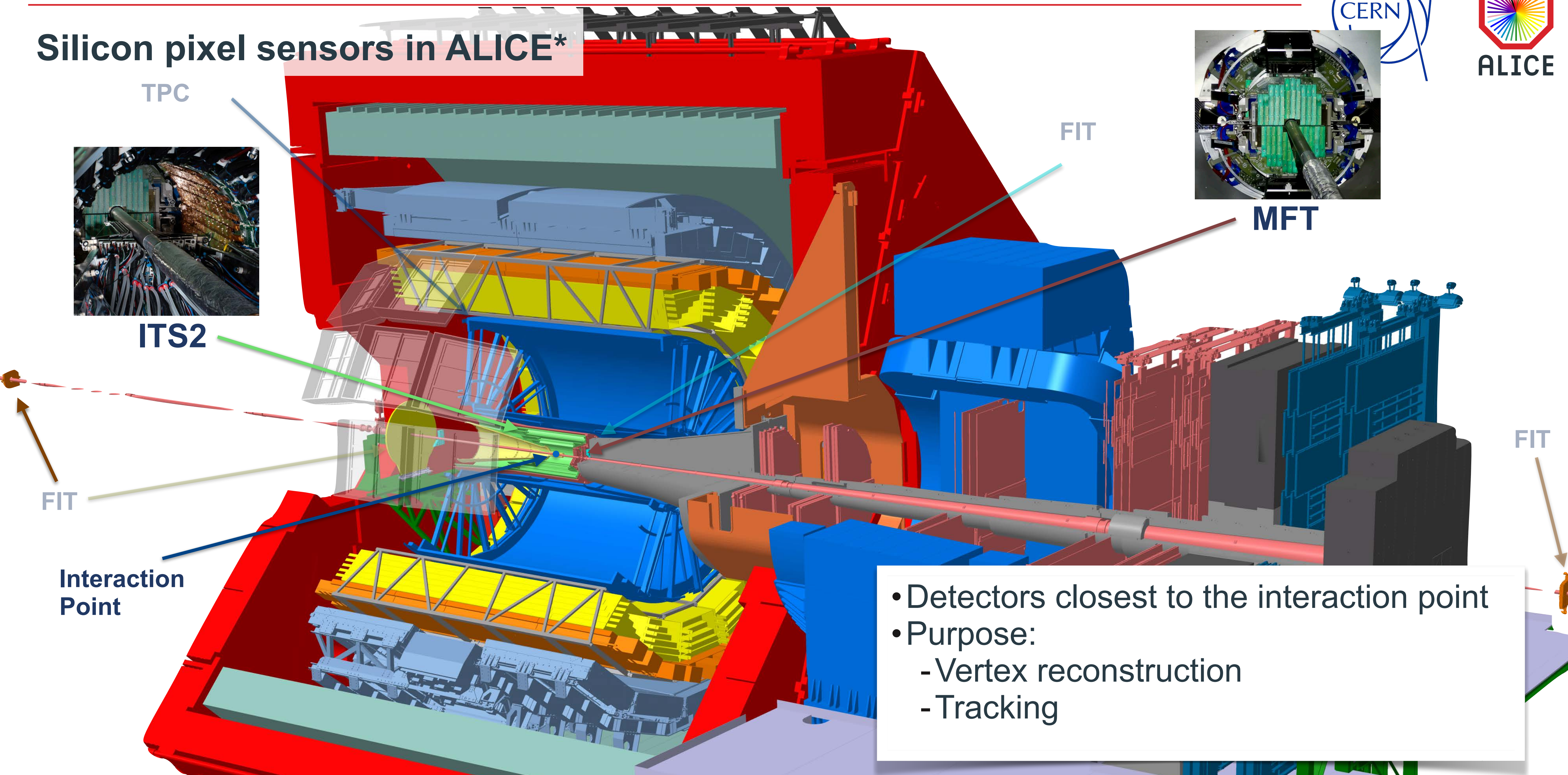


CMOS pixel sensors for charged particles — working principle

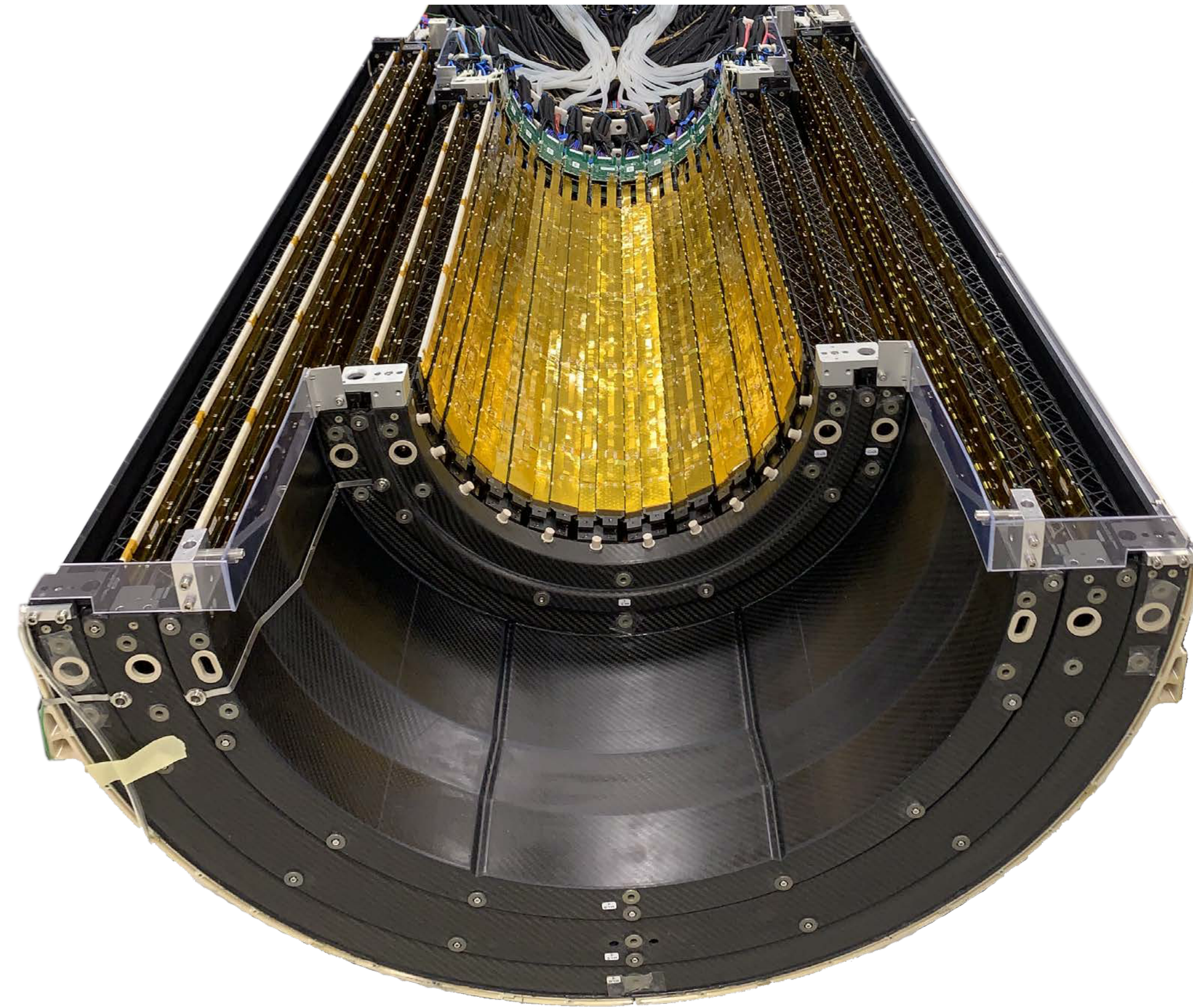
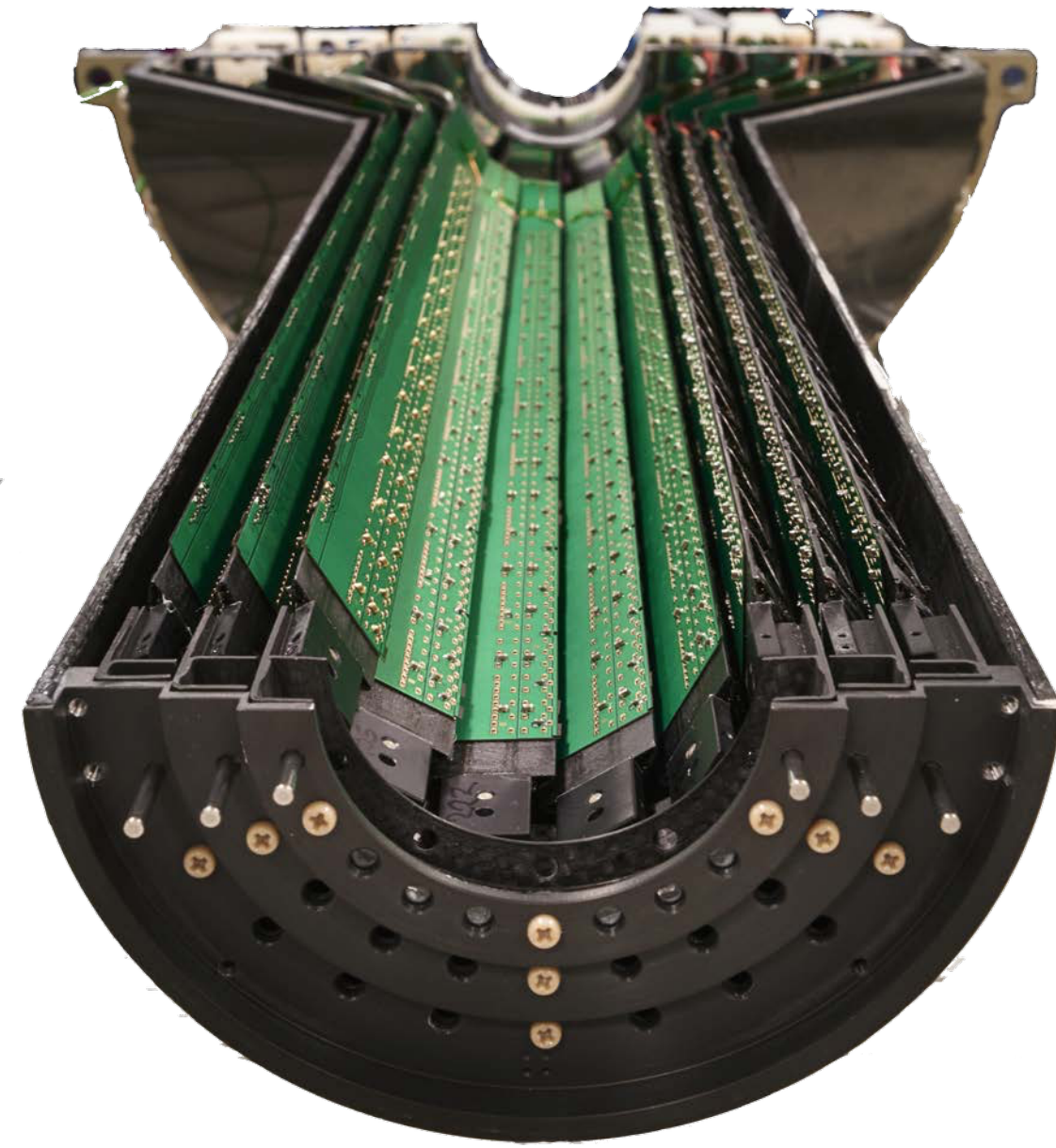


Simplified, not to scale!
Especially in terms of size
and number of transistors.

Silicon pixel sensors in ALICE*



* and in heavy-ion physics and particle physics experiments in general



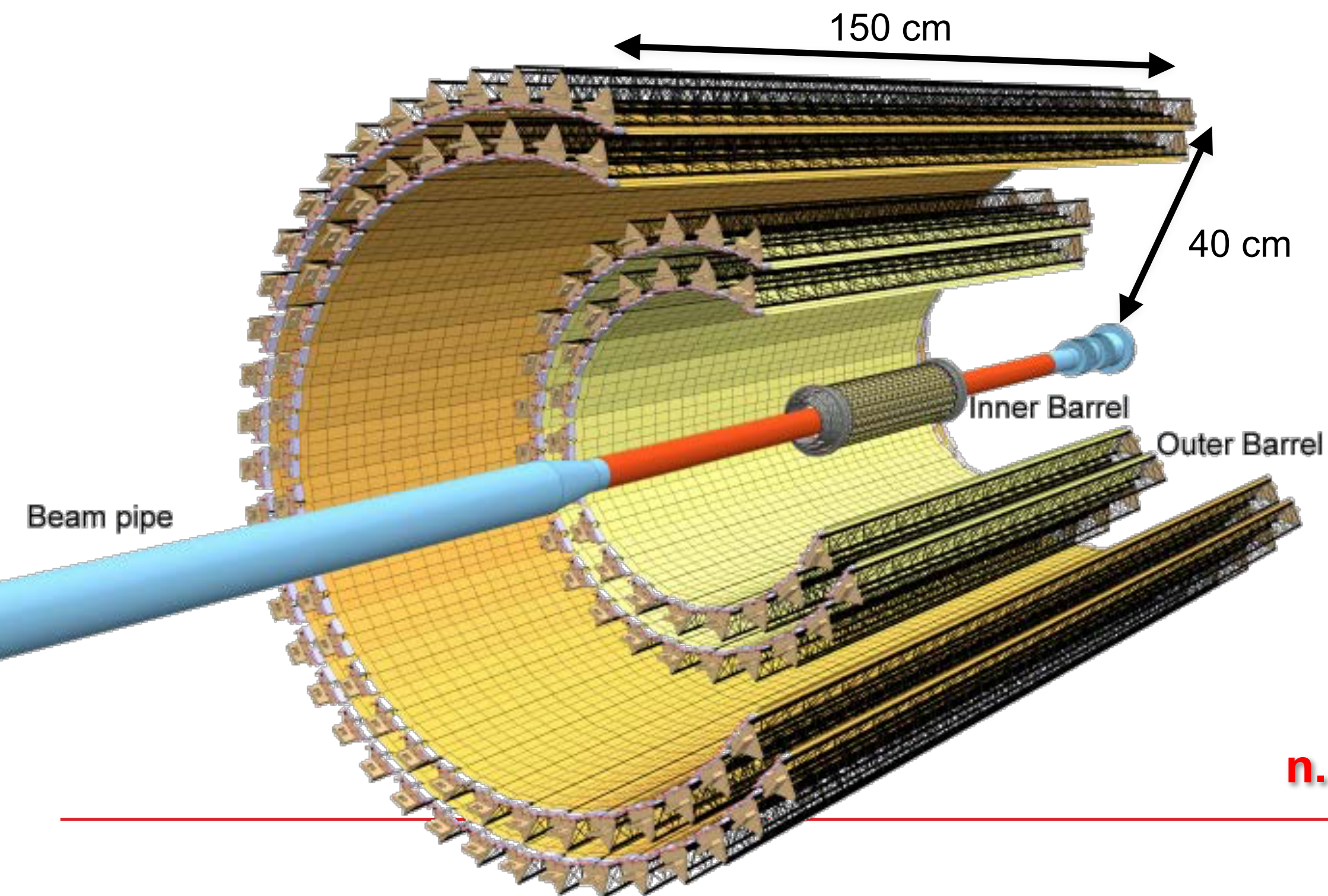
ITS2



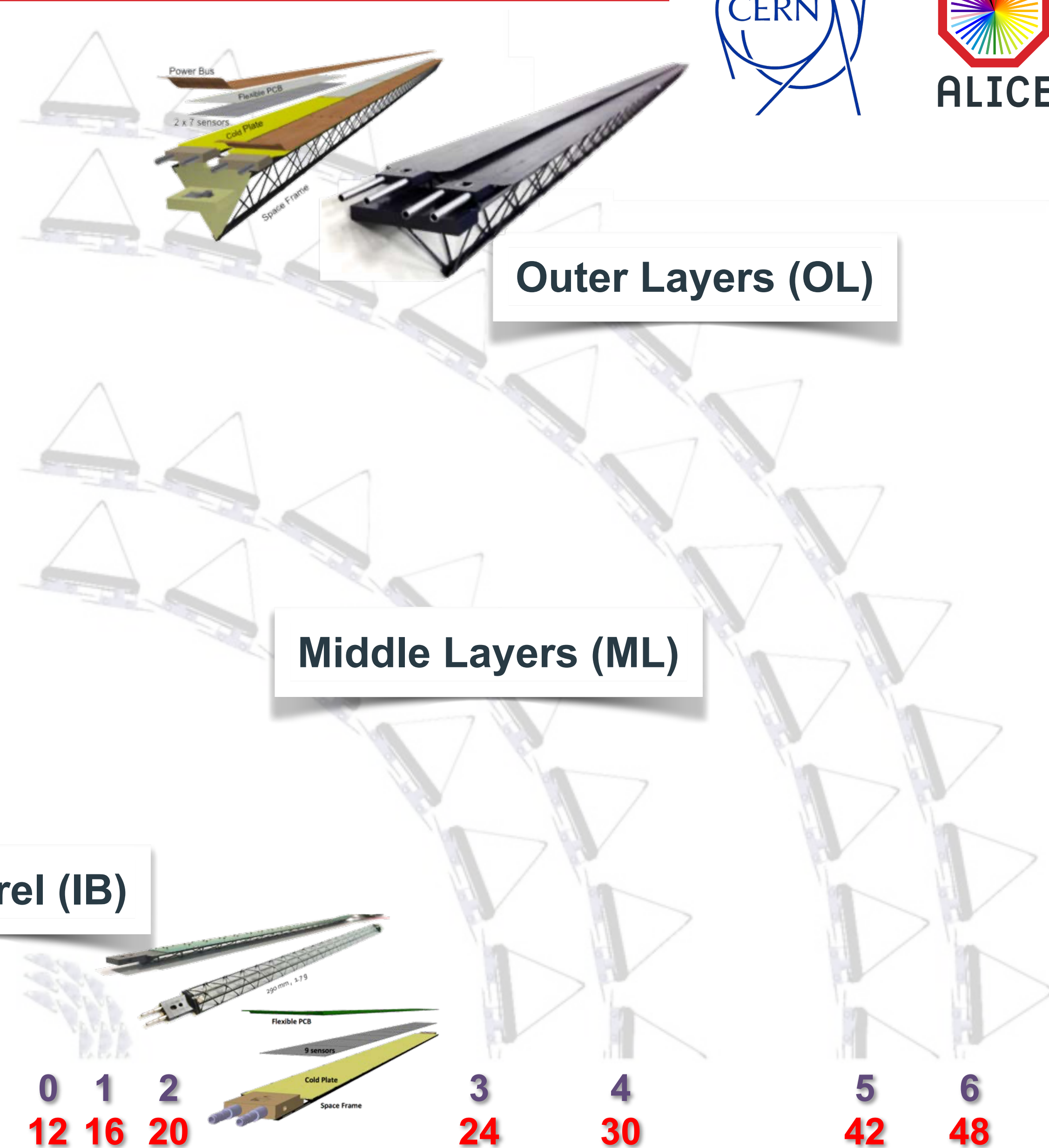
ITS2 layout

- 7 layers (inner/middle/outer): **3/2/2** from $R = 23 \text{ mm}$ to $R = 400 \text{ mm}$
- 192 staves (IL/ML/OL): **48/54/90**
- Ultra-lightweight support structure and cooling

10 m² active silicon area, 12.5×10⁹ pixels



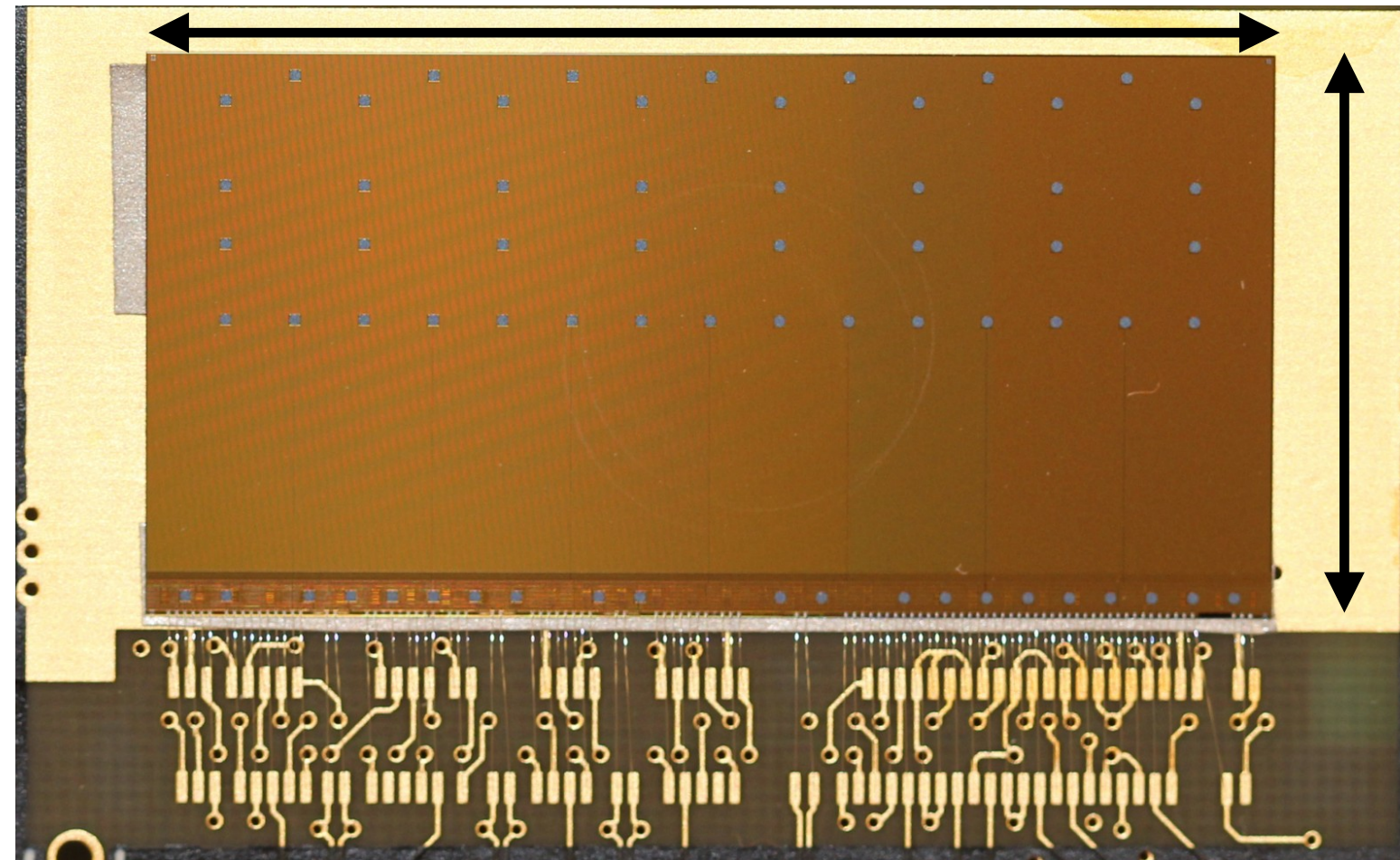
**Outer Barrel (OB)
= ML + OL**



ALPIDE — the CMOS pixel sensor for ITS2

ALice Pixel DEtector

3 cm / 1024 pixels



1.5 cm / 512 pixels

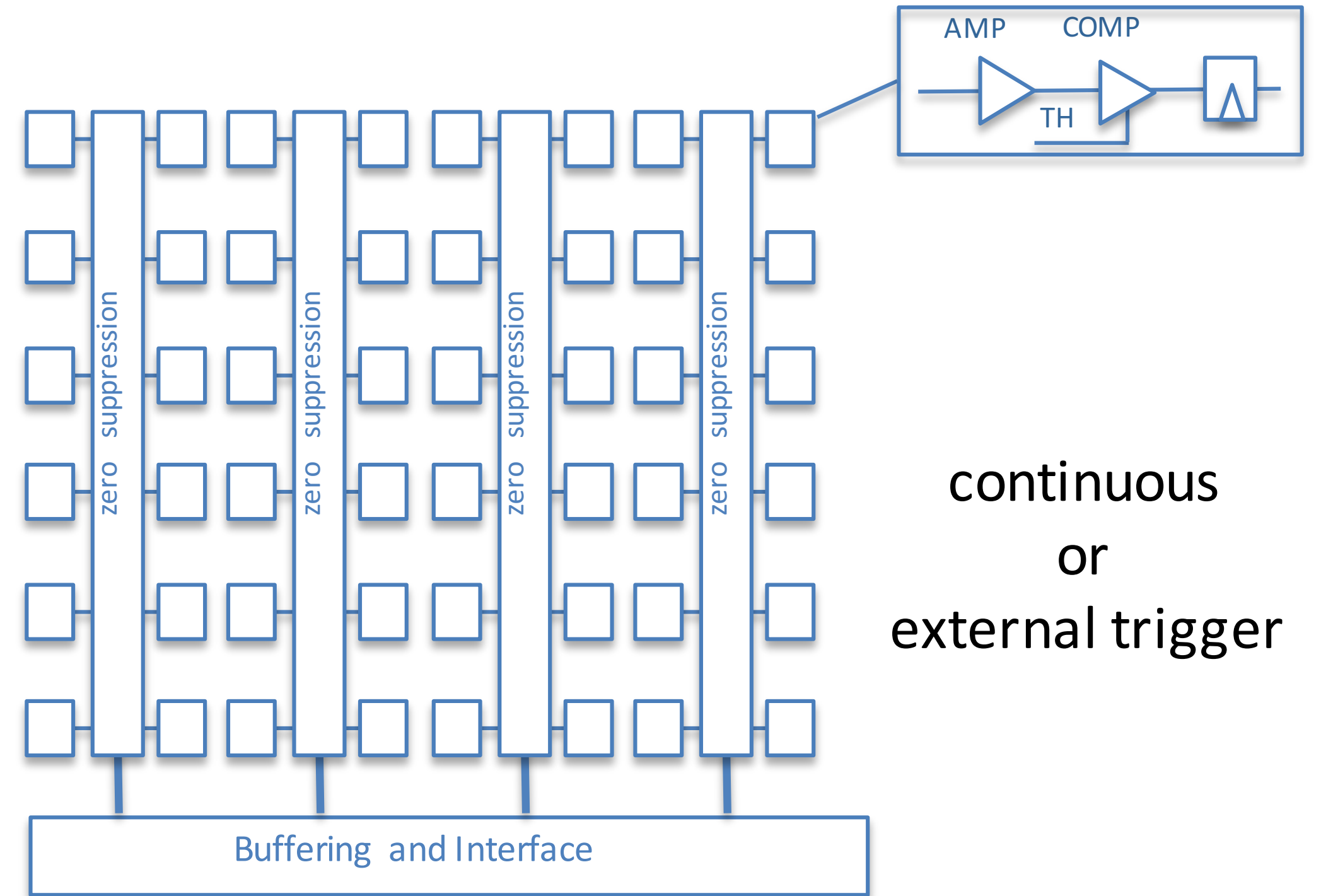
ALPIDE die on carrier card

- Developed within the ITS2 project

Key features

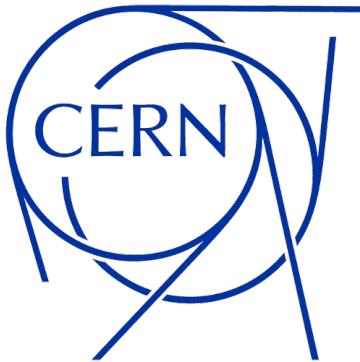
- Full CMOS circuitry within active area
- In-pixel amplification and shaping, discrimination and Multiple-Event Buffers (MEB)

Technology now used in other applications



ALPIDE architecture

- In-matrix data sparsification
- On-chip high-speed link (1.2 Gbps)
- Low total power consumption $< 47.5 \text{ mW/cm}^2$
 - Achieved by a 40 nW/pixel front-end



ALPIDE requirements and performance

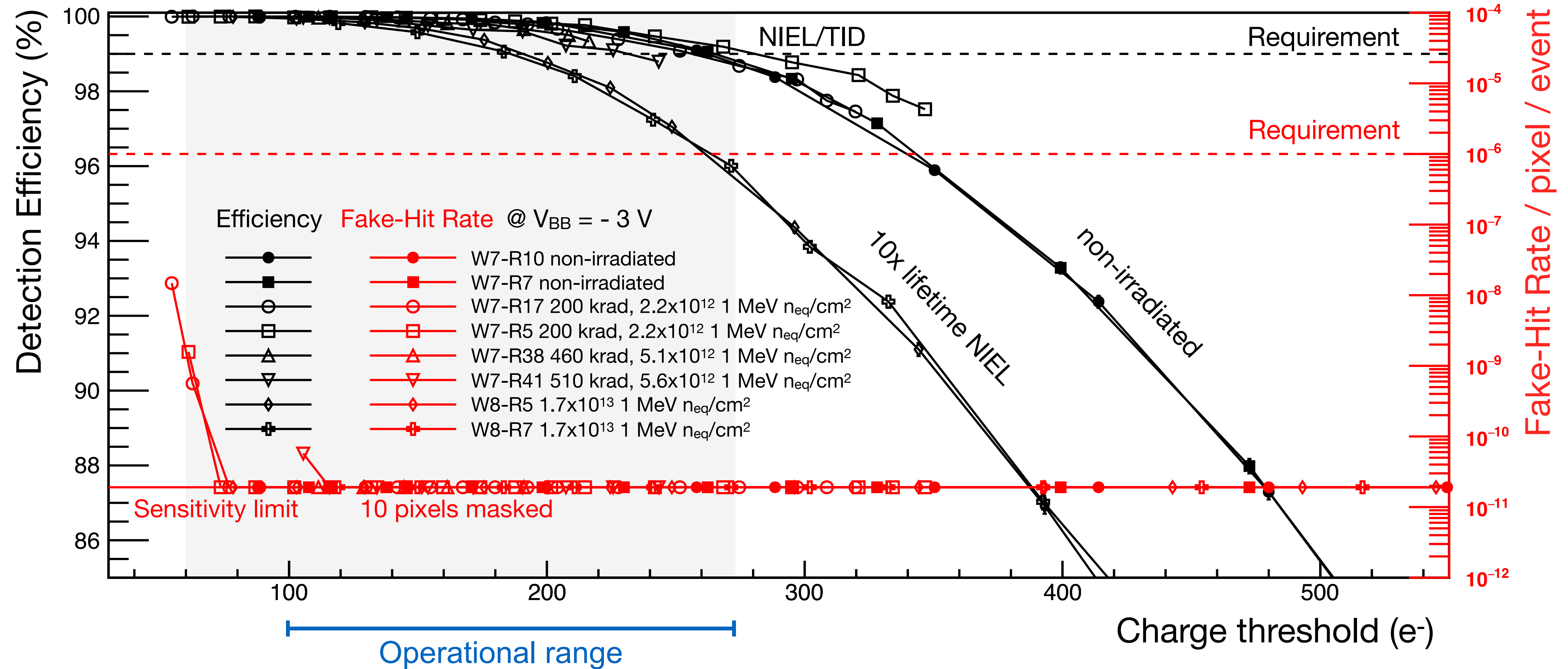
Parameter	Requirement	ALPIDE
Spatial resolution (μm)	≈ 5	≈ 5
Integration time (μs)	< 30	< 10
Fake-hit rate (/ pixel / event)	< 10 ⁻⁶	<< 10 ⁻⁶
Detection efficiency	> 99%	>>99%
Power consumption (mW / cm ²)	< 100	< 50
Total Ionising Dose (TID) (krad)	> 270 (IB) > 10 (OB)	OK
Non-Ionising Energy Loss (NIEL) (1 MeV n _{eq} / cm ²)	> 1.7x10 ¹²	OK

These are not technology limits,
but mostly design choices!

> 70k chips produced and tested

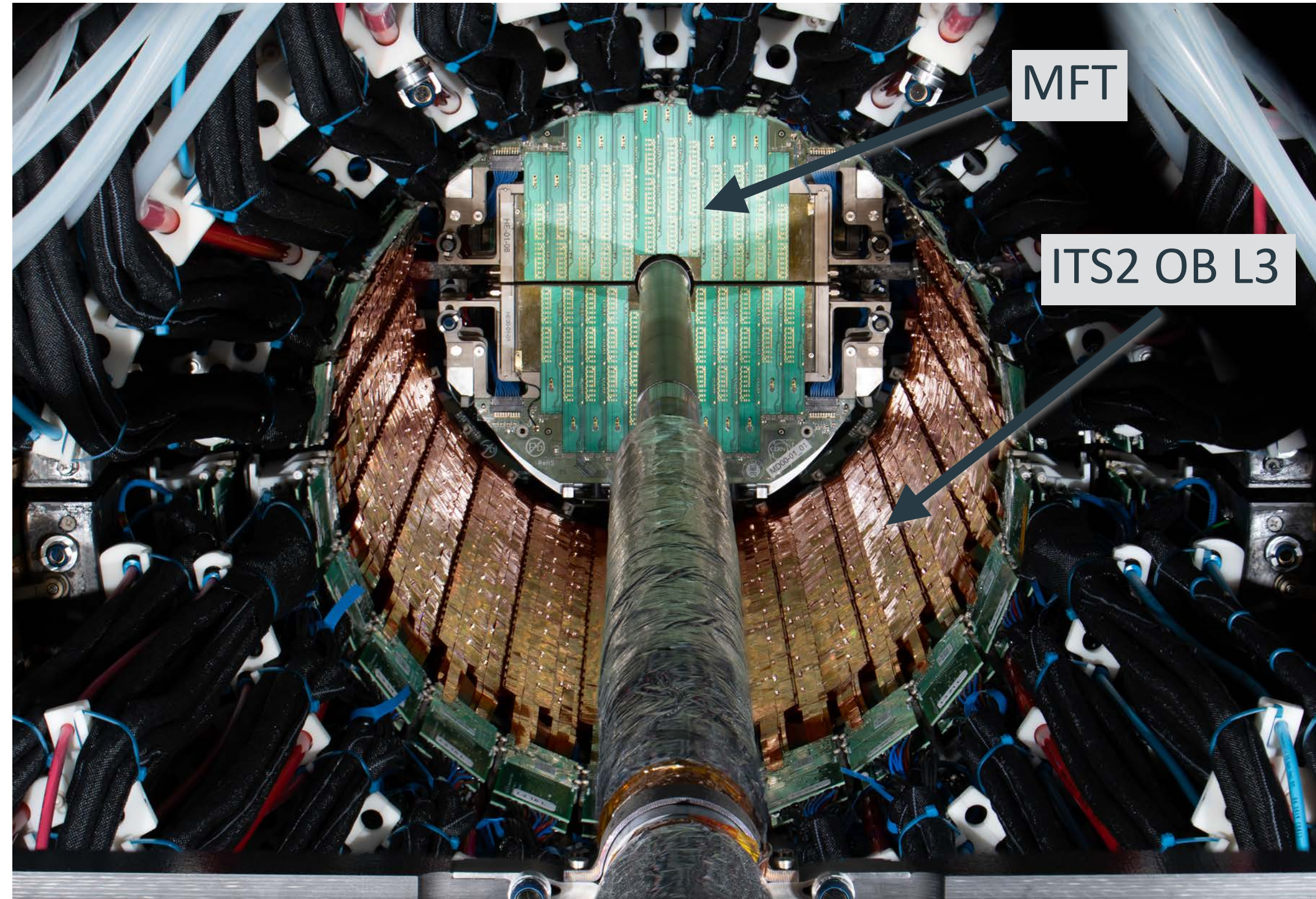
24k in continuous operation on ITS2
+ several other applications

ALPIDE performance — detection efficiency and fake-hit rate

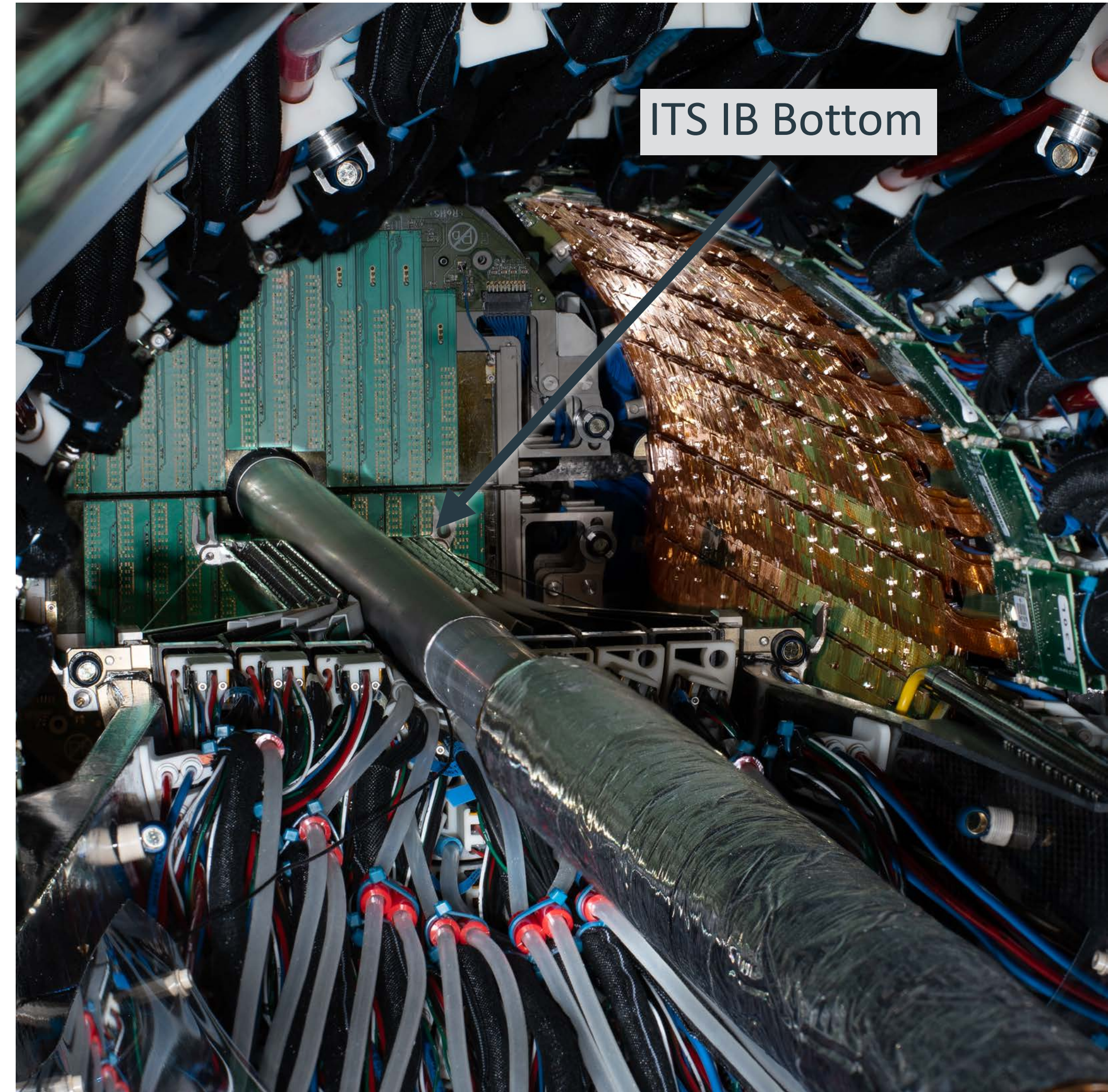


Very efficient ($> 99\%$) and low noise ($\ll 10^{-6}$ / pixel / event) even after irradiation

ITS2 in the ALICE experimental apparatus



ITS Outer Barrel surrounding the beam pipe, MFT in the back



ITS Inner Barrel Bottom and Outer Barrel



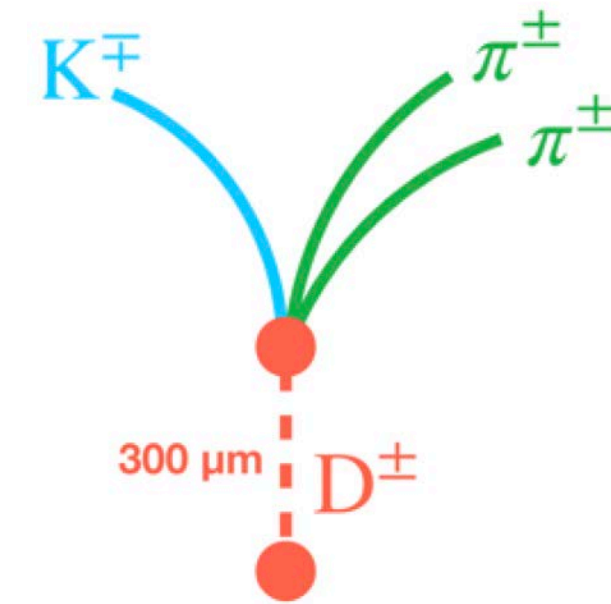
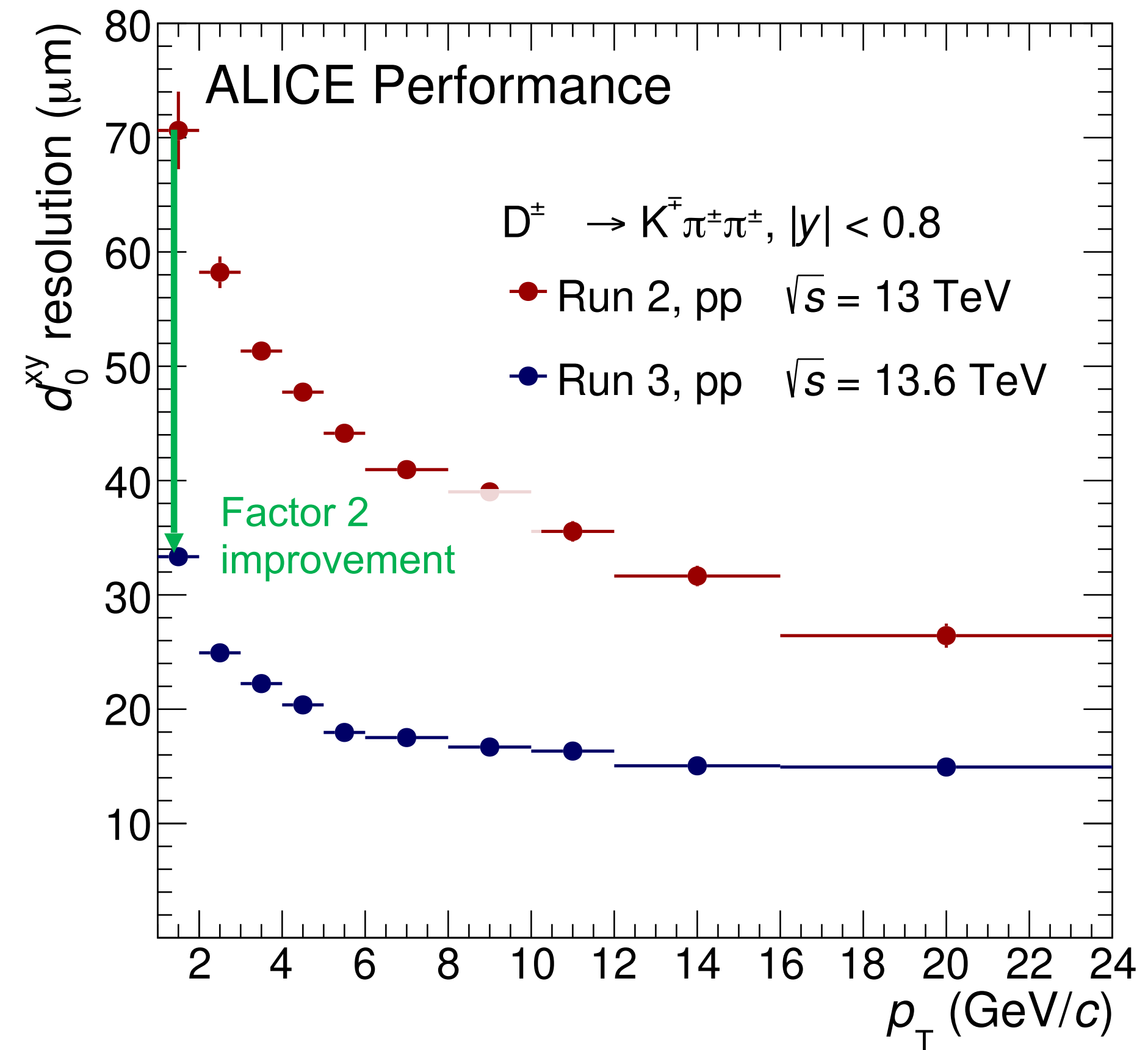
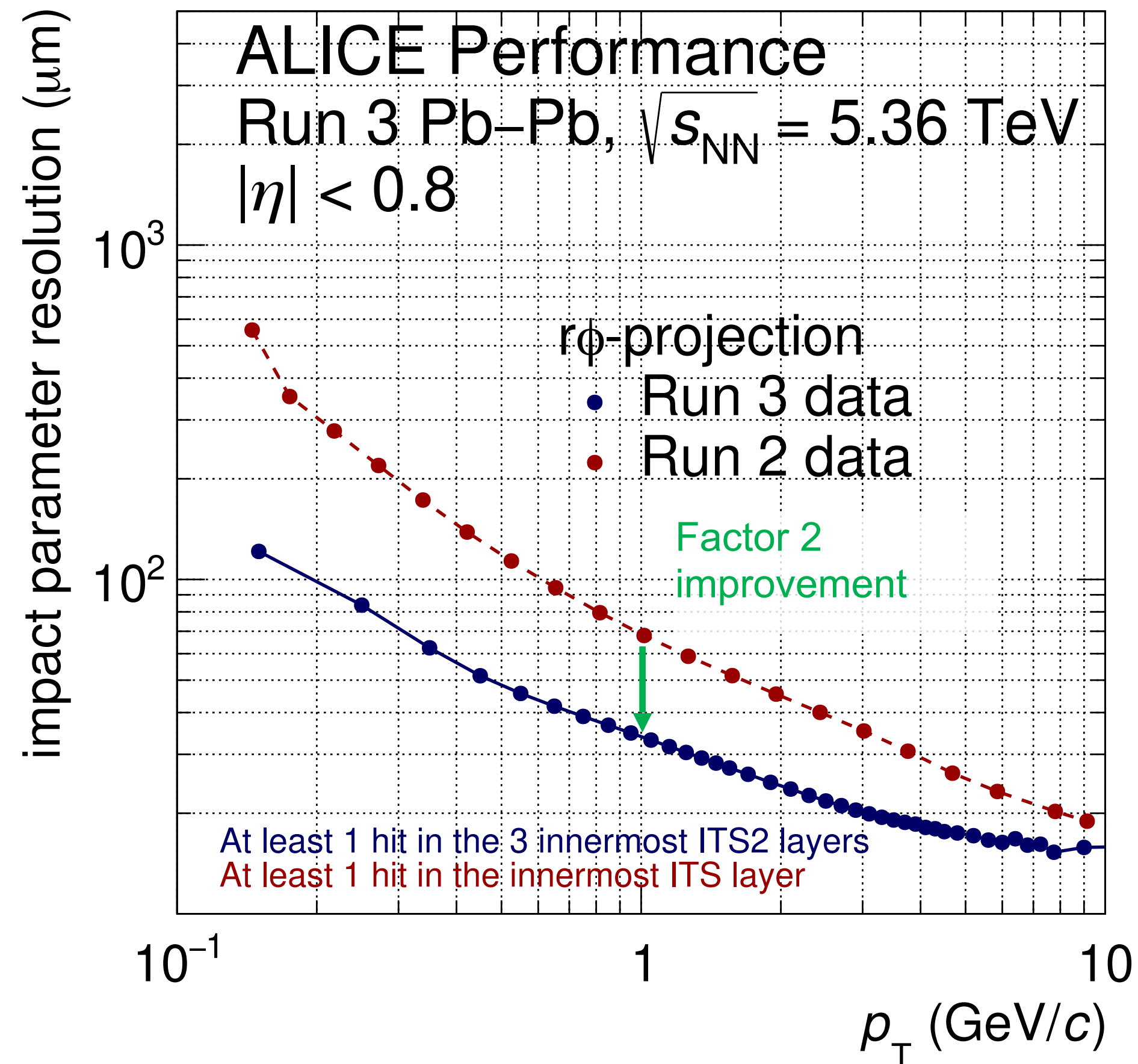
ALICE

Pb-Pb 5.36 TeV

LHC22s period
18th November 2022

16:52:47₈₉₃

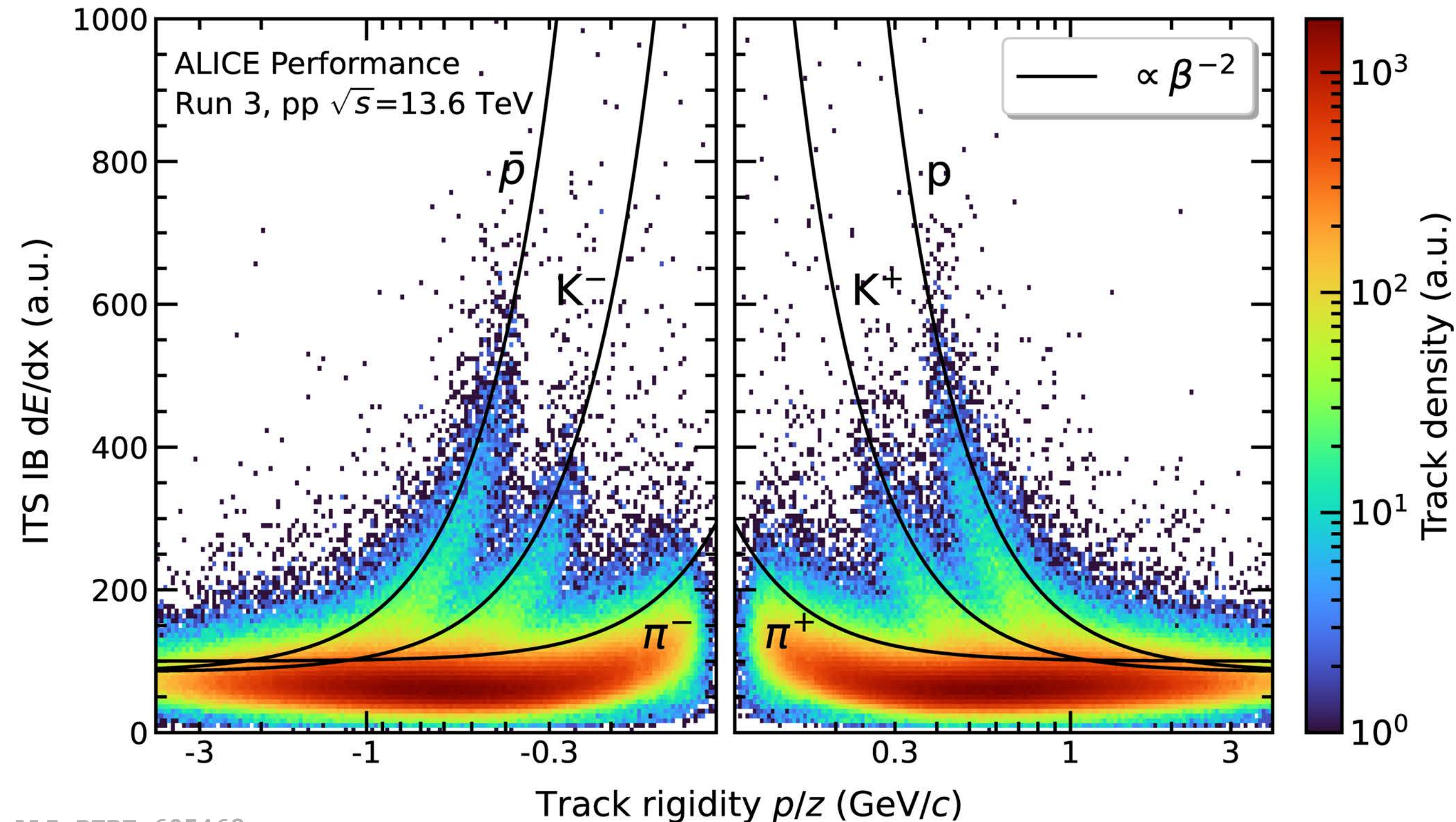
Detector performance



Improved impact parameter resolution for charged tracks and $D^\pm$ mesons

F. Schlepper - 3+1D reconstruction of the Inner Tracking System (ITS2) for ALICE Run 3

R&D — dE/dx using Time-over-Threshold

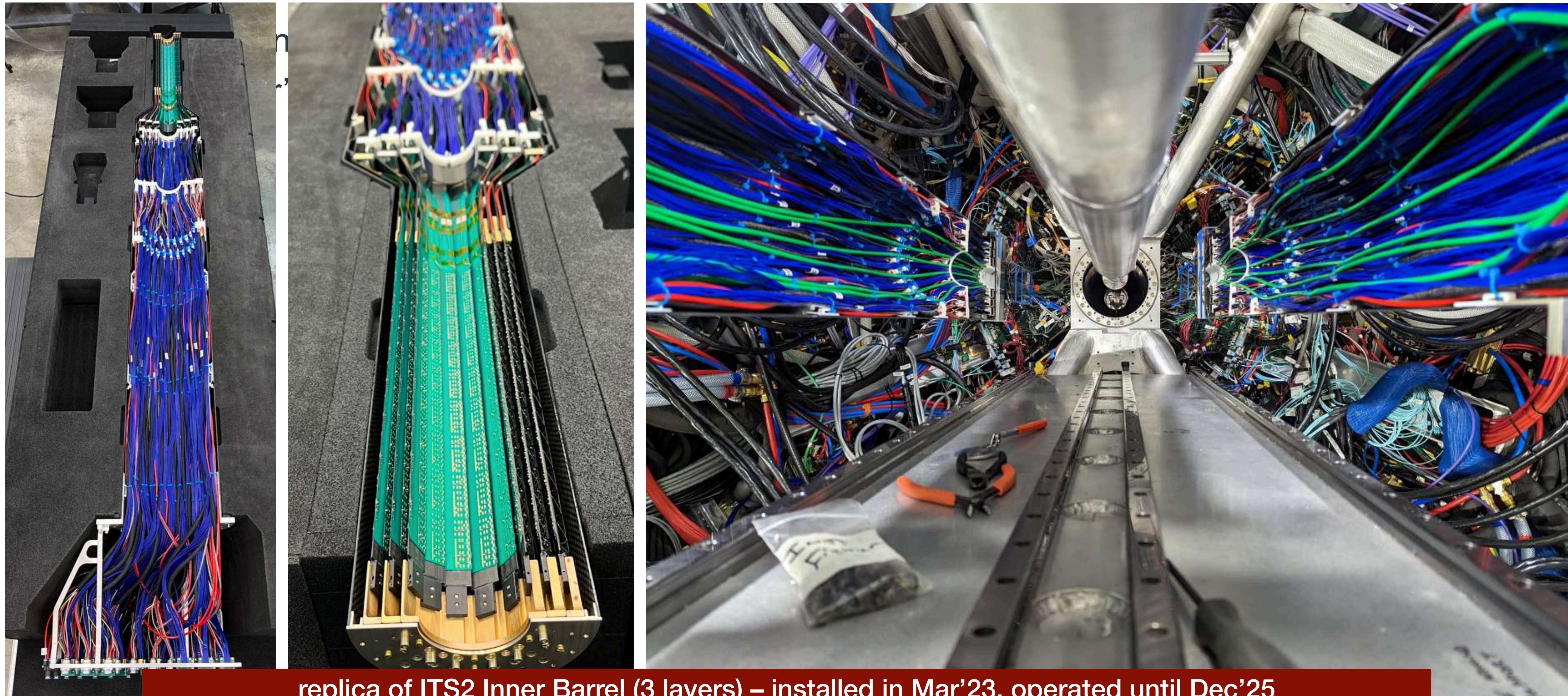


ALI-PERF-605468

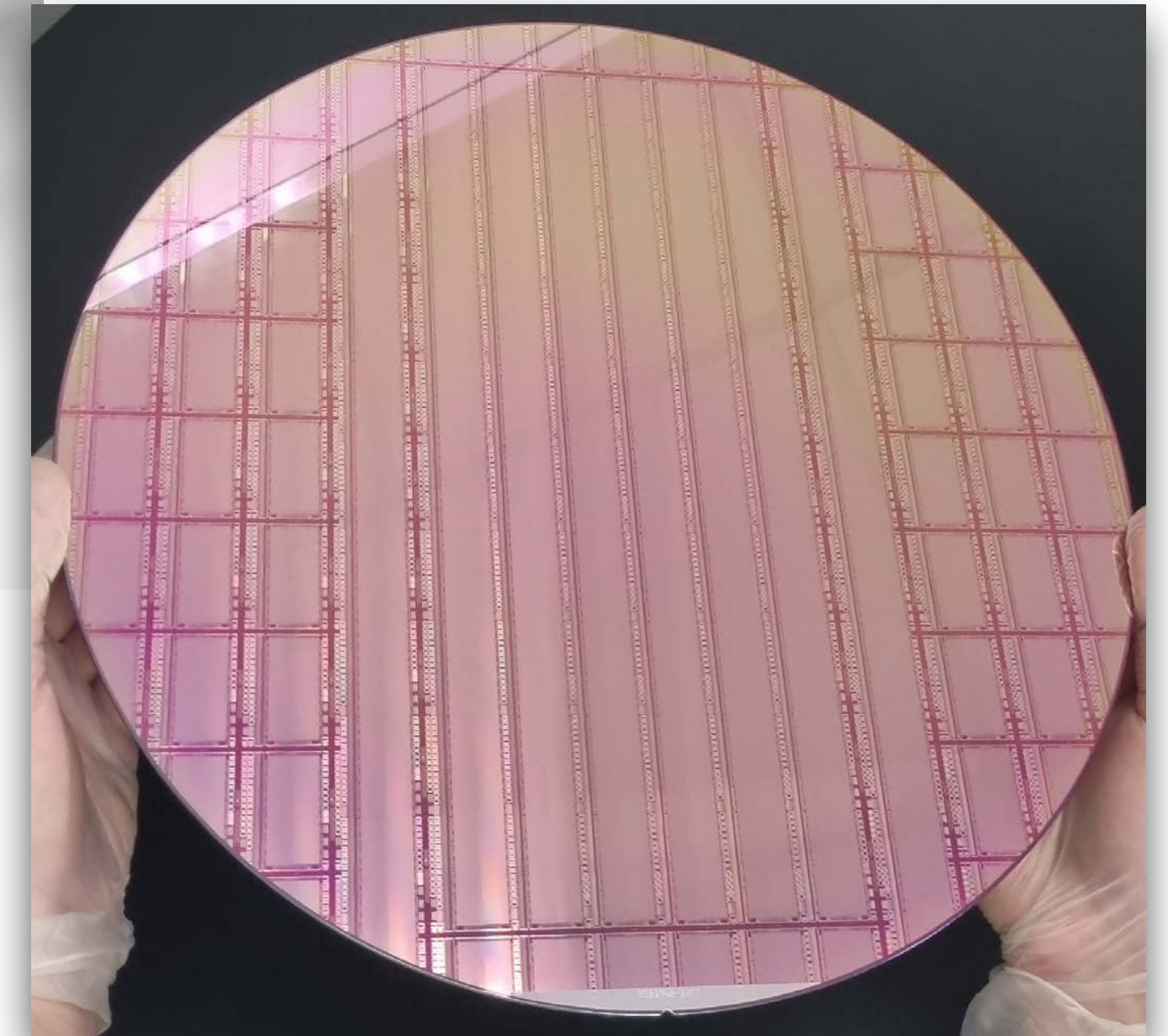
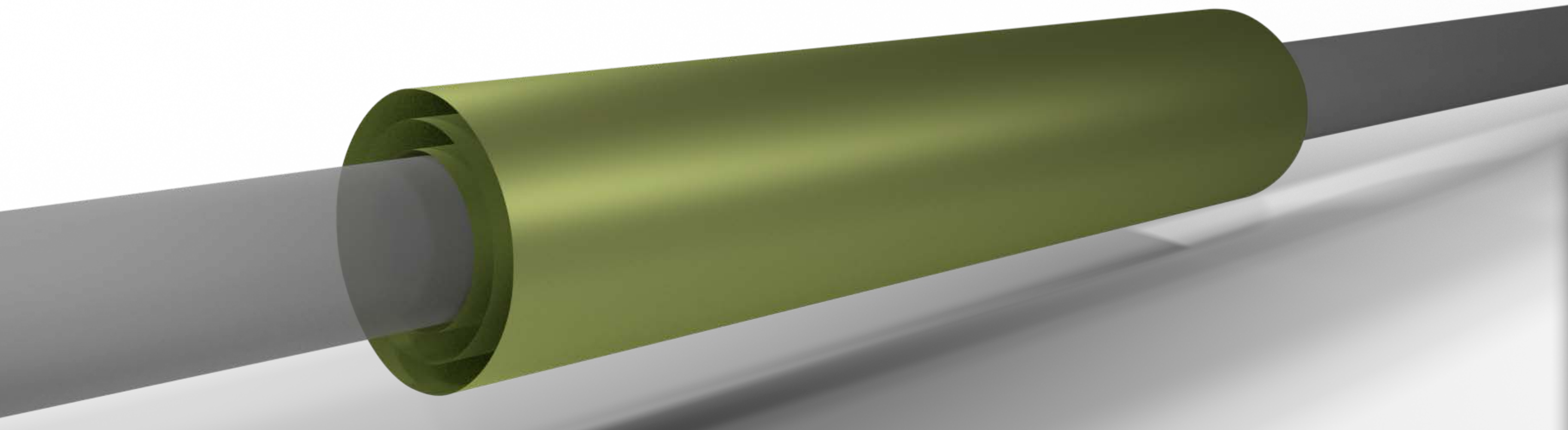
ITS dE/dx signal from 3 layers using Time-over-Threshold

- ITS2 does not feature reading charge information by default
- Using special operation mode:
 - Deactivation of the signal clipping in the front-end circuit
⇒ Signal duration corresponding to charge
 - Increased sampling frequency 200 kHz → 2 MHz
⇒ Time-over-Threshold (ToT) information
⇒ Sampling individual hits up to ~100 times
 - Reduction of interaction rate
⇒ free up bandwidth for the oversampling
 - Only working in the innermost three layers due to readout bandwidth limitation

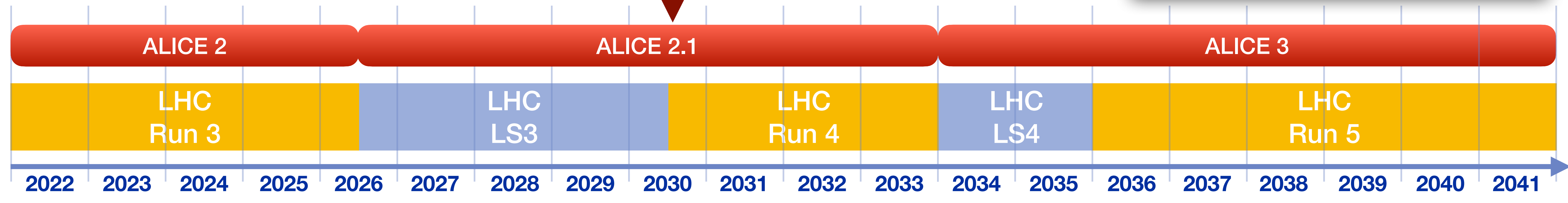
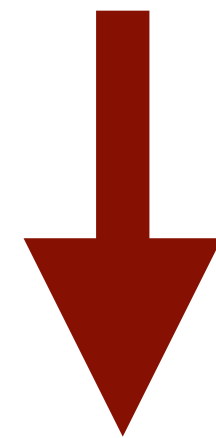
ITS2 offspring — example sPhenix MVTX



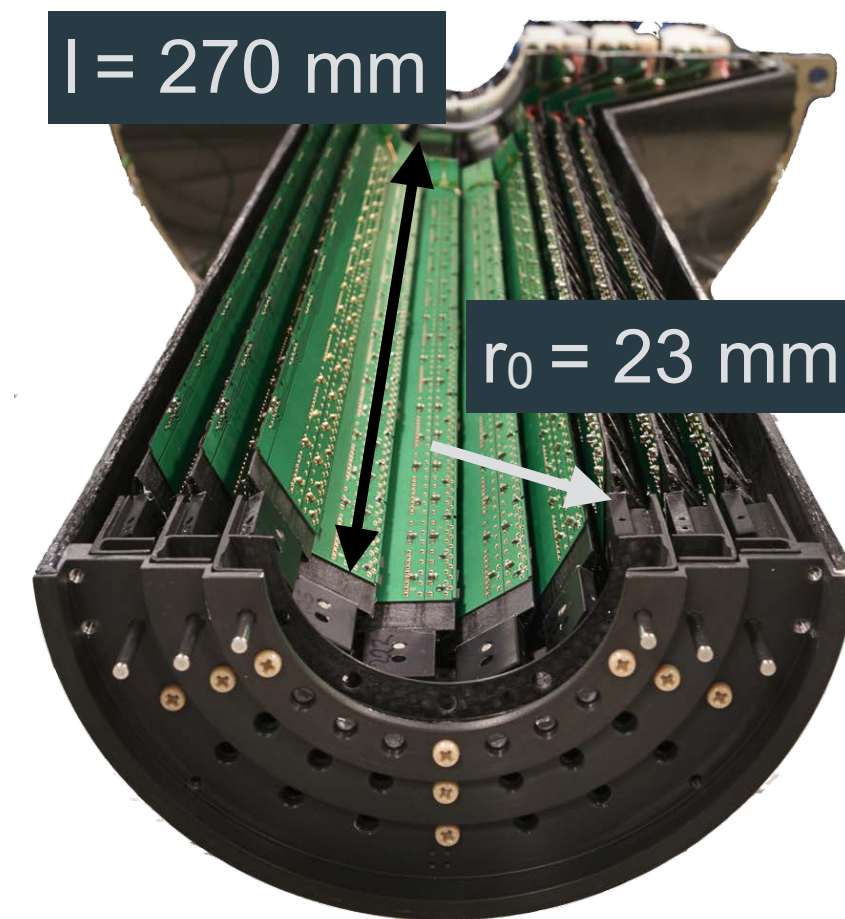
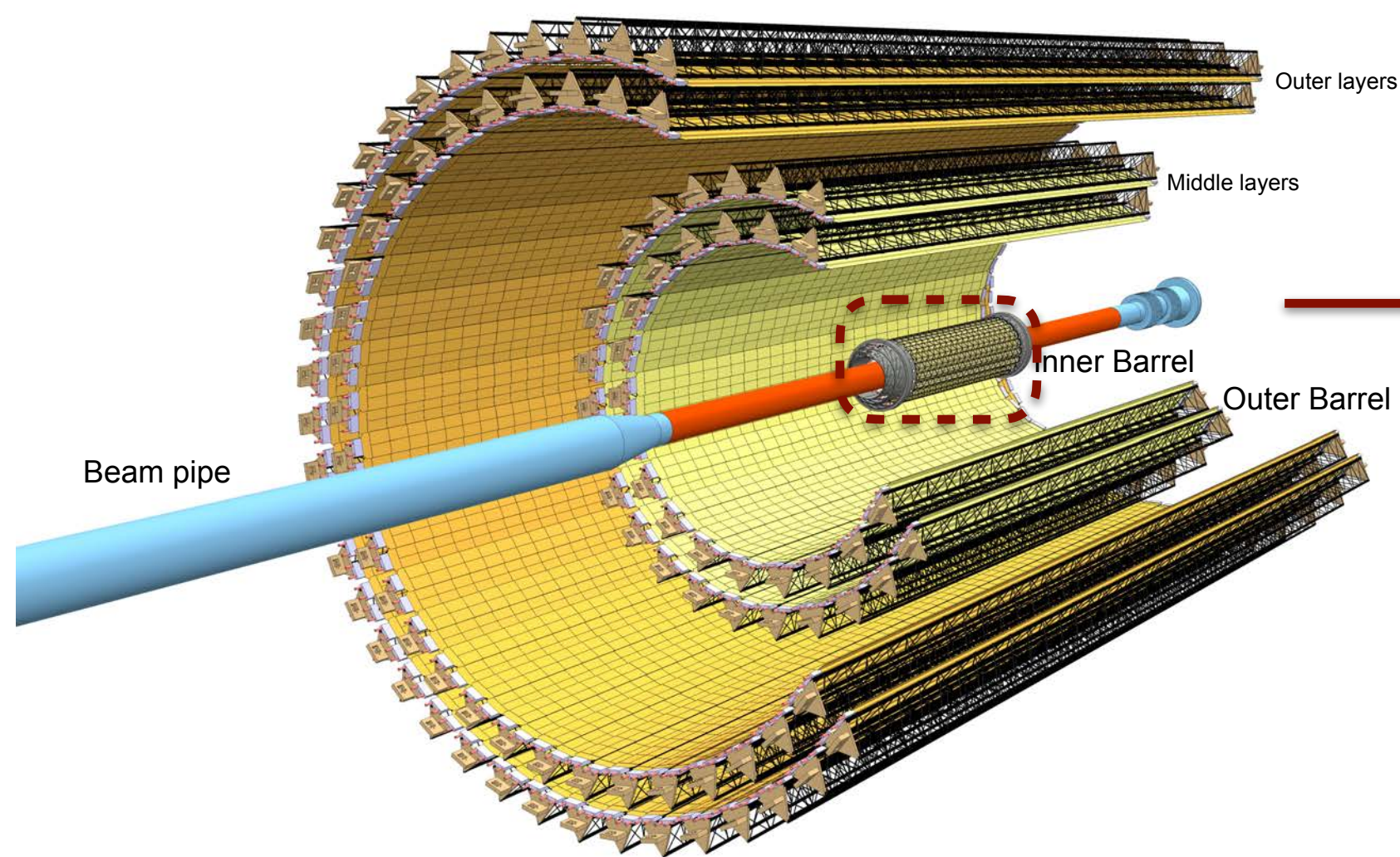
replica of ITS2 Inner Barrel (3 layers) – installed in Mar'23, operated until Dec'25



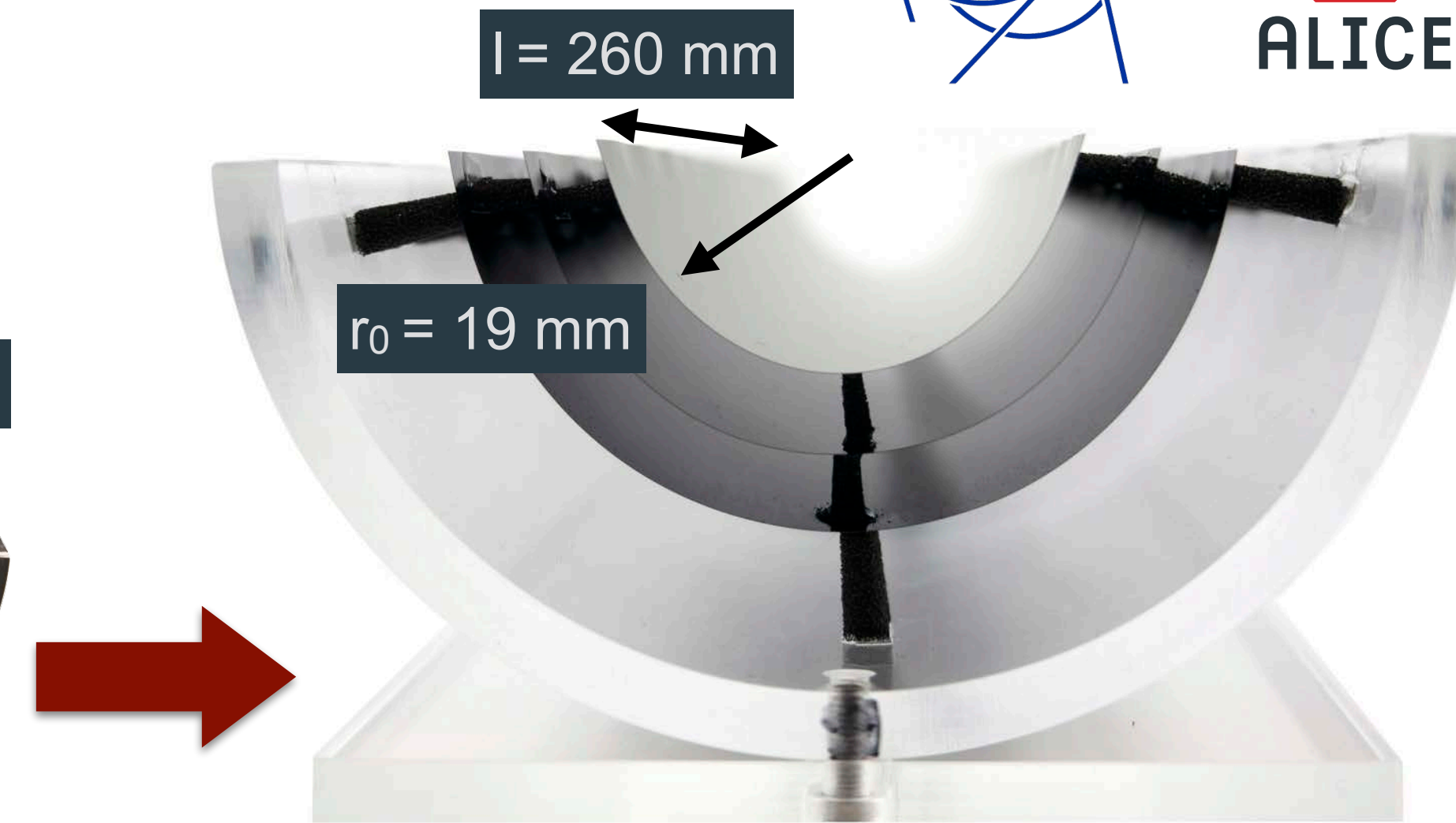
ITS3



The Inner Tracking System 3 (ITS3)

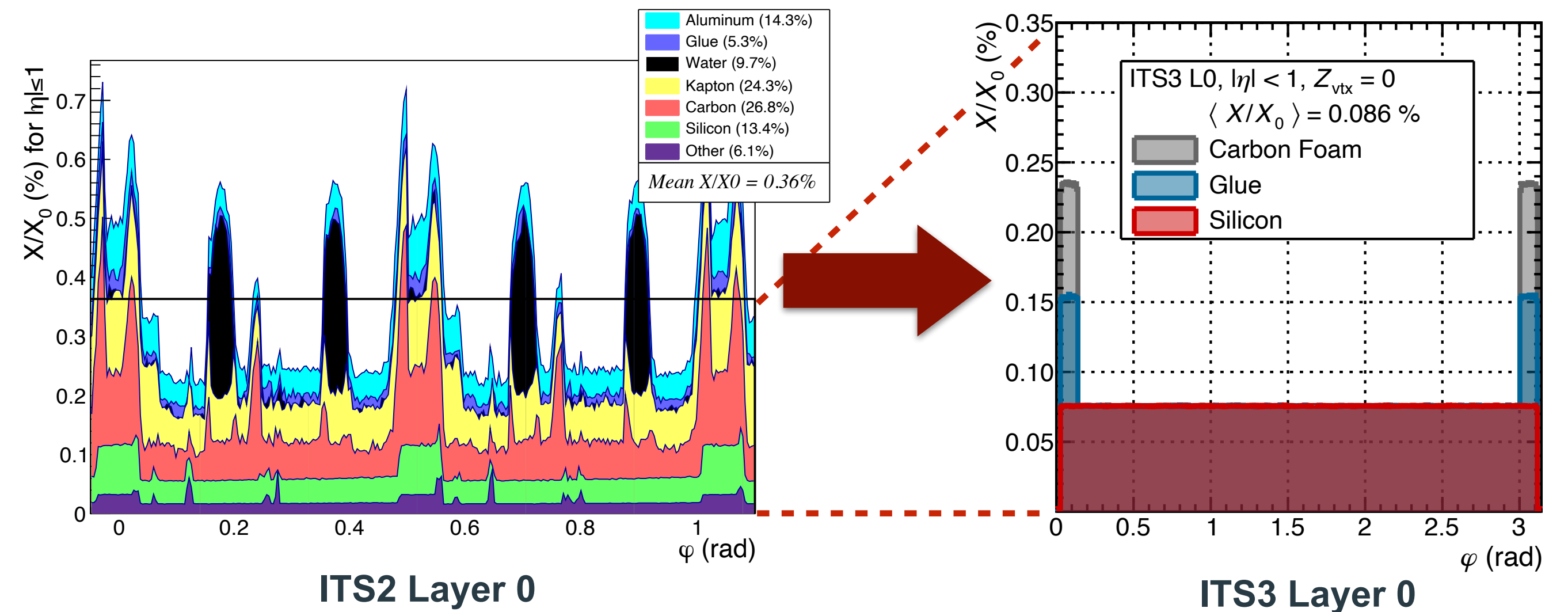


ITS2 Inner Barrel

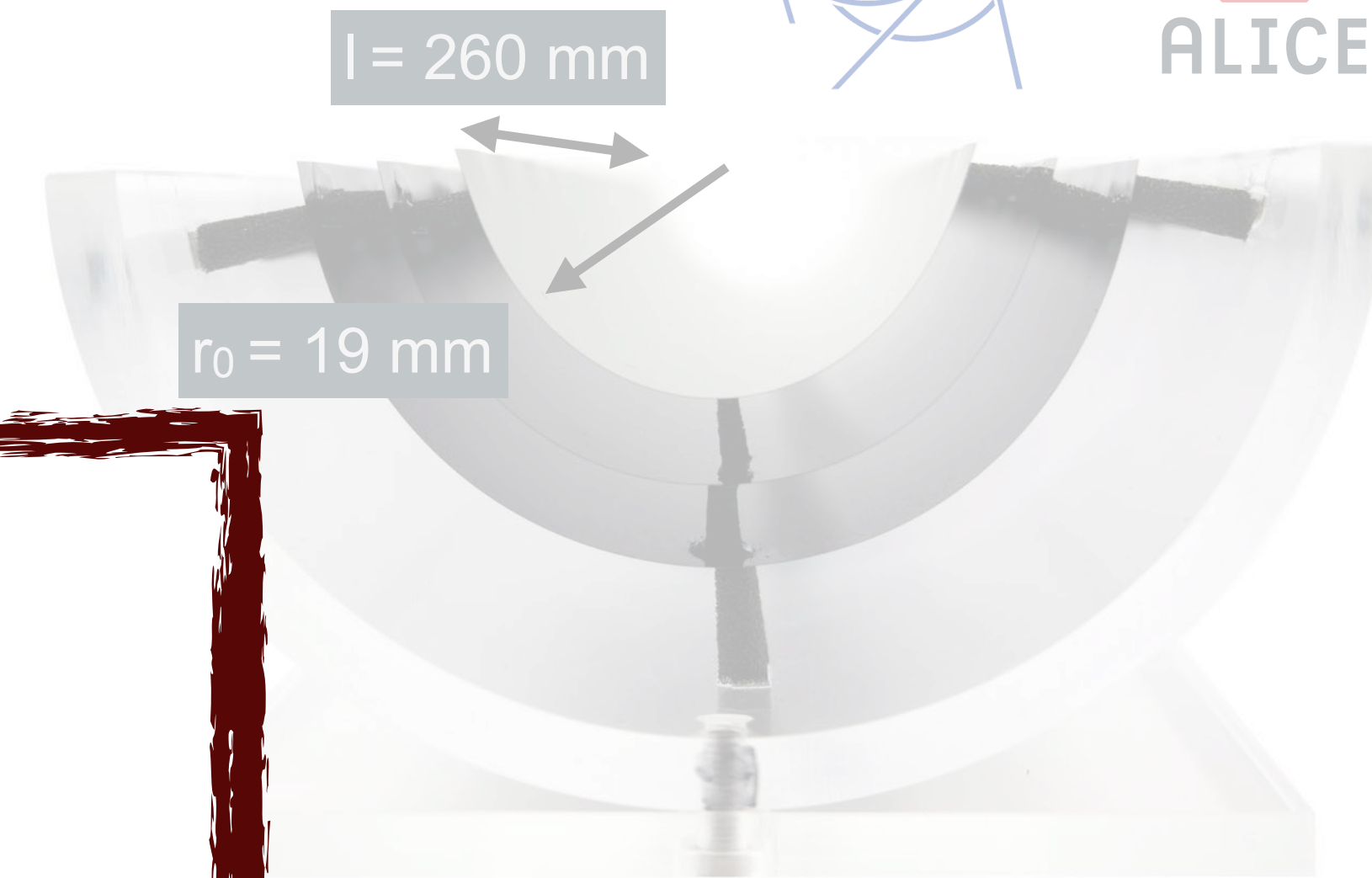
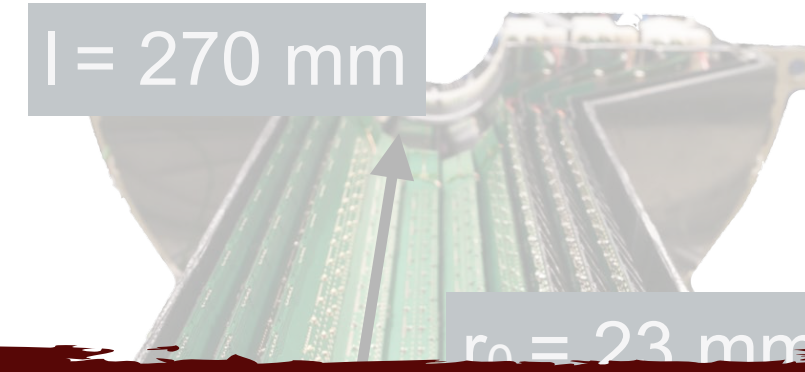
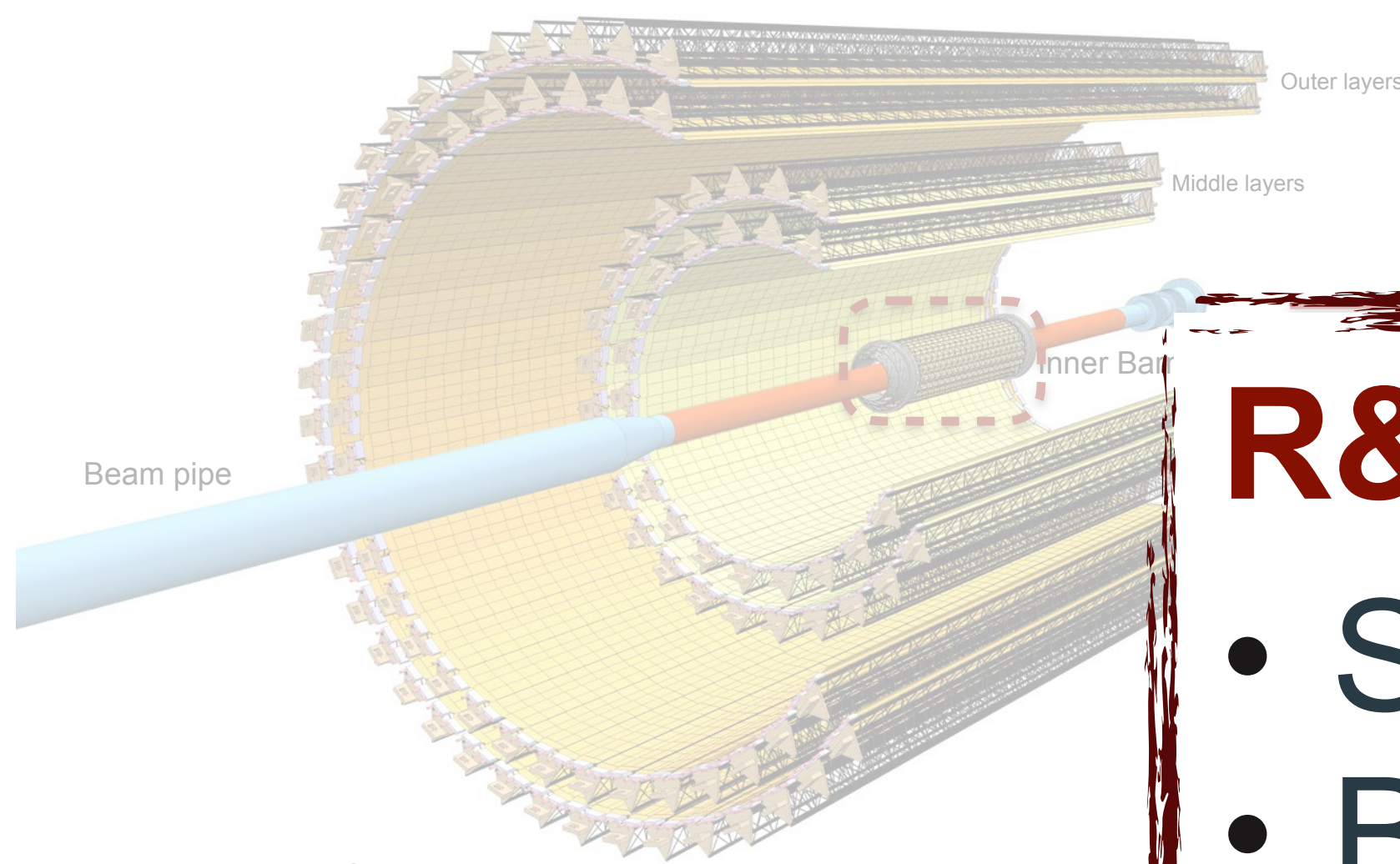


ITS3 Engineering Model 1

- Replacement of ITS2 Inner Barrel with 3 layers of curved, $50 \mu\text{m}$ thick, wafer-scale MAPS
- Air cooling & ultra-light mechanical supports
- Reduced material budget of on average **$0.09\% X_0$** instead of **$0.36\% X_0$** per layer
- Smaller radius of the innermost layer: **19 mm** instead of **23 mm**
- New thinner, smaller diameter beam pipe



The Inner Tracking System 3 (ITS3)

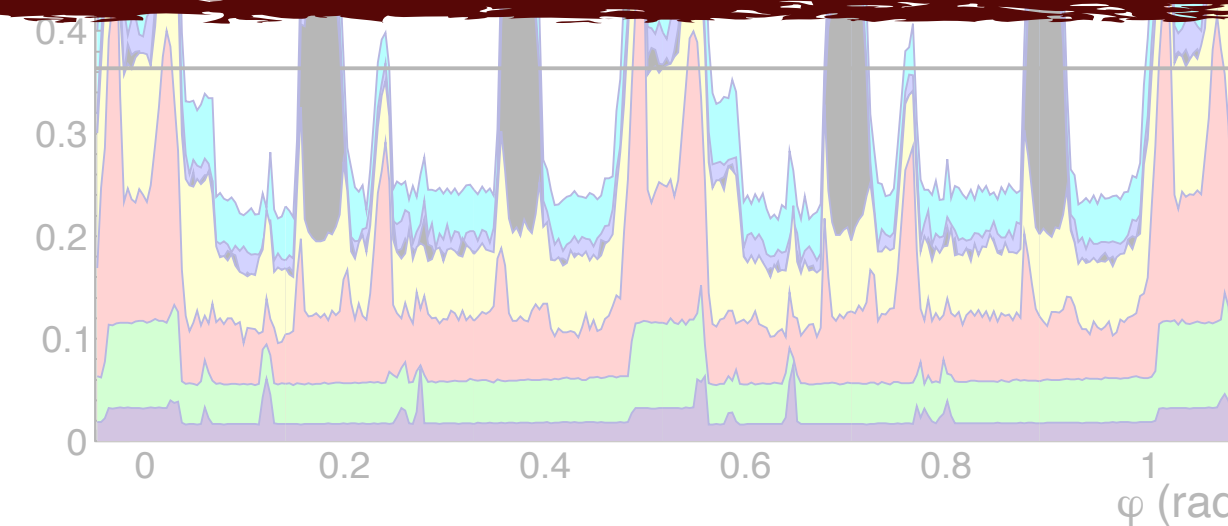


ITS3 Engineering Model 1

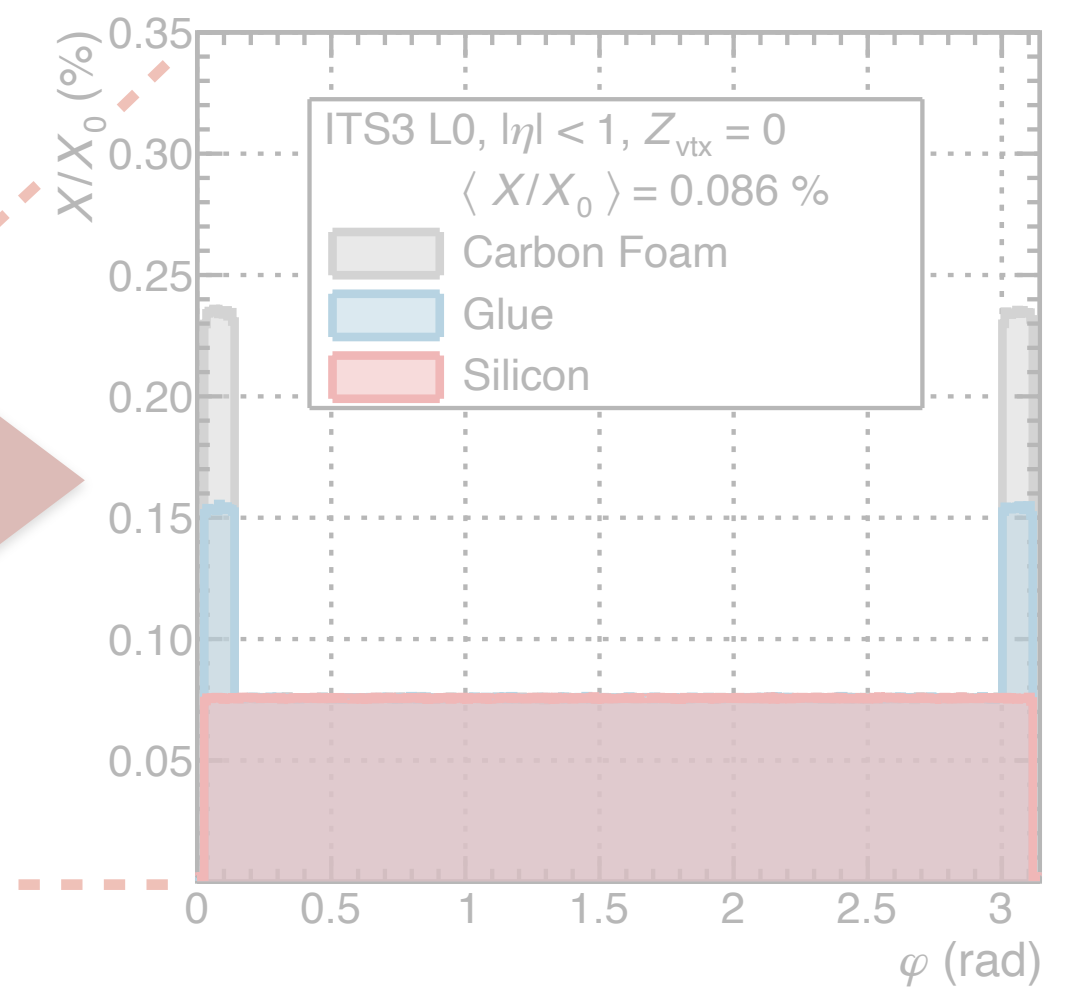
R&D items

- Stitching
- Bending of silicon wafers
- Air cooling
- No electrical substrate

- Replacement of ITS2 Inner with 3 layers of curved, 50 μ m wafer-scale MAPS
- Air cooling & ultra-light mechanical structure
- Reduced material budget of on average **0.09% X_0** instead of **0.36% X_0** per layer
- Smaller radius of the innermost layer: **19 mm** instead of **23 mm**
- New thinner, smaller diameter beam pipe



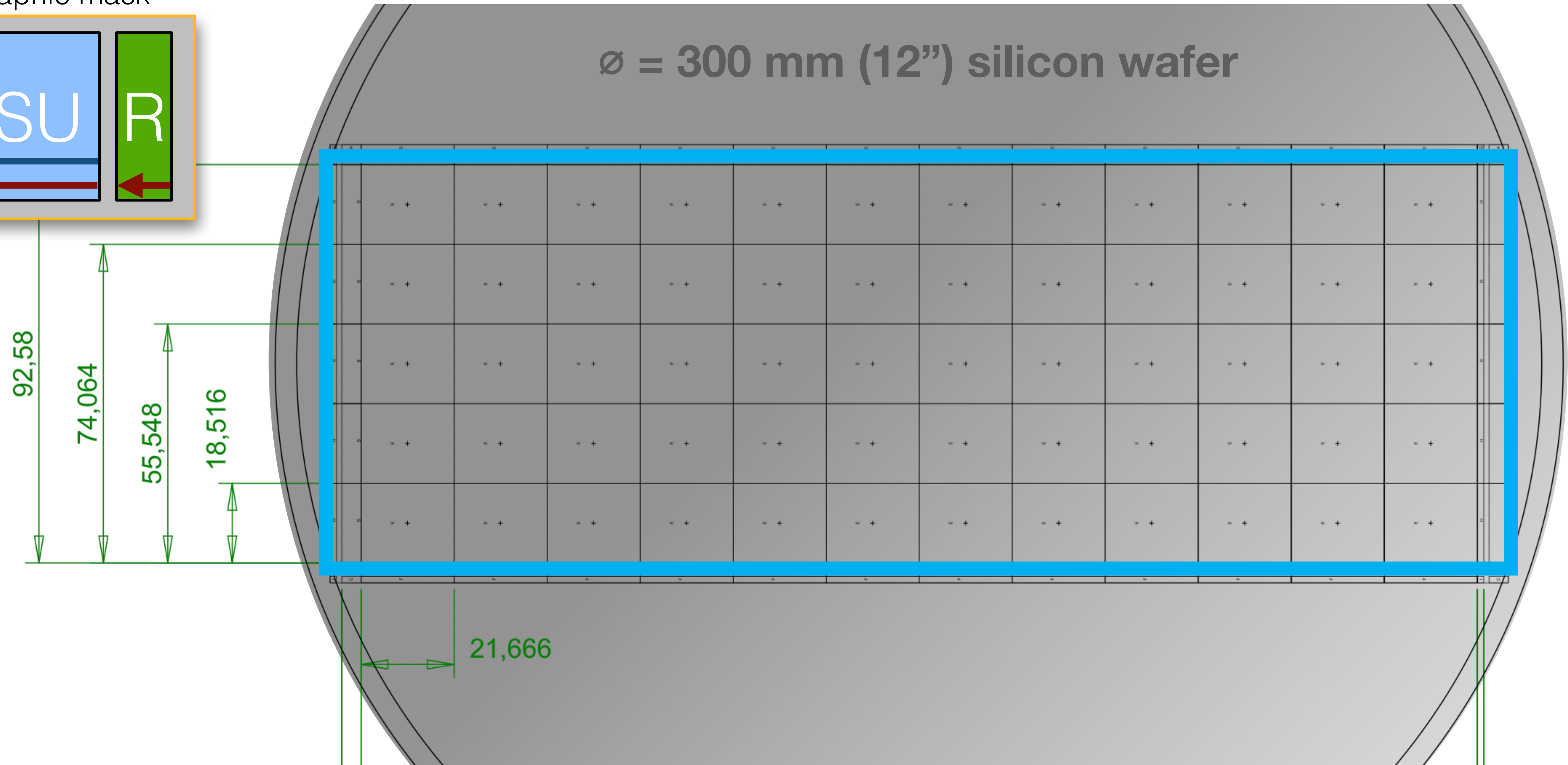
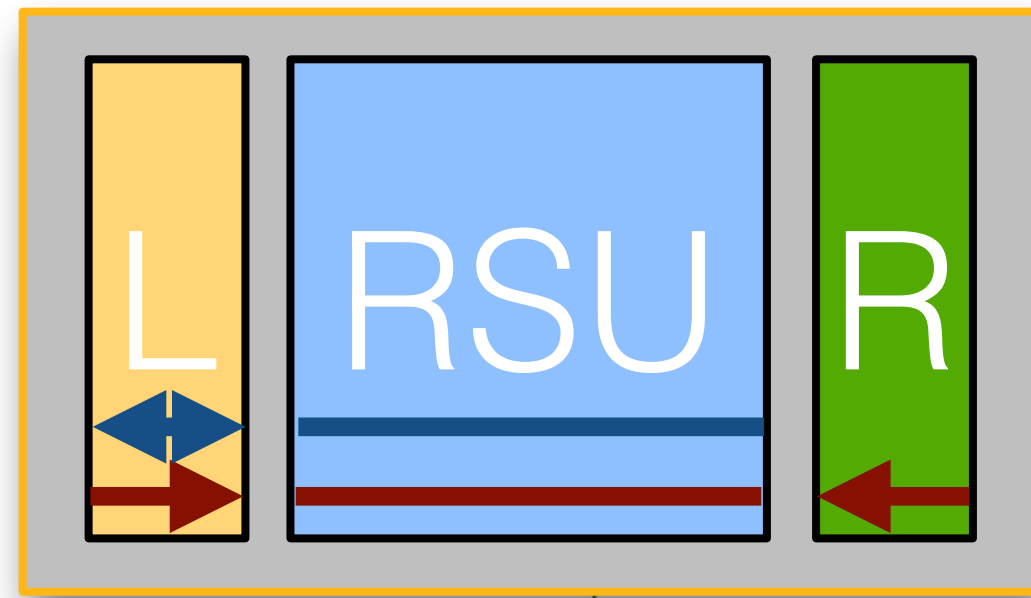
ITS2 Layer 0



ITS3 Layer 0

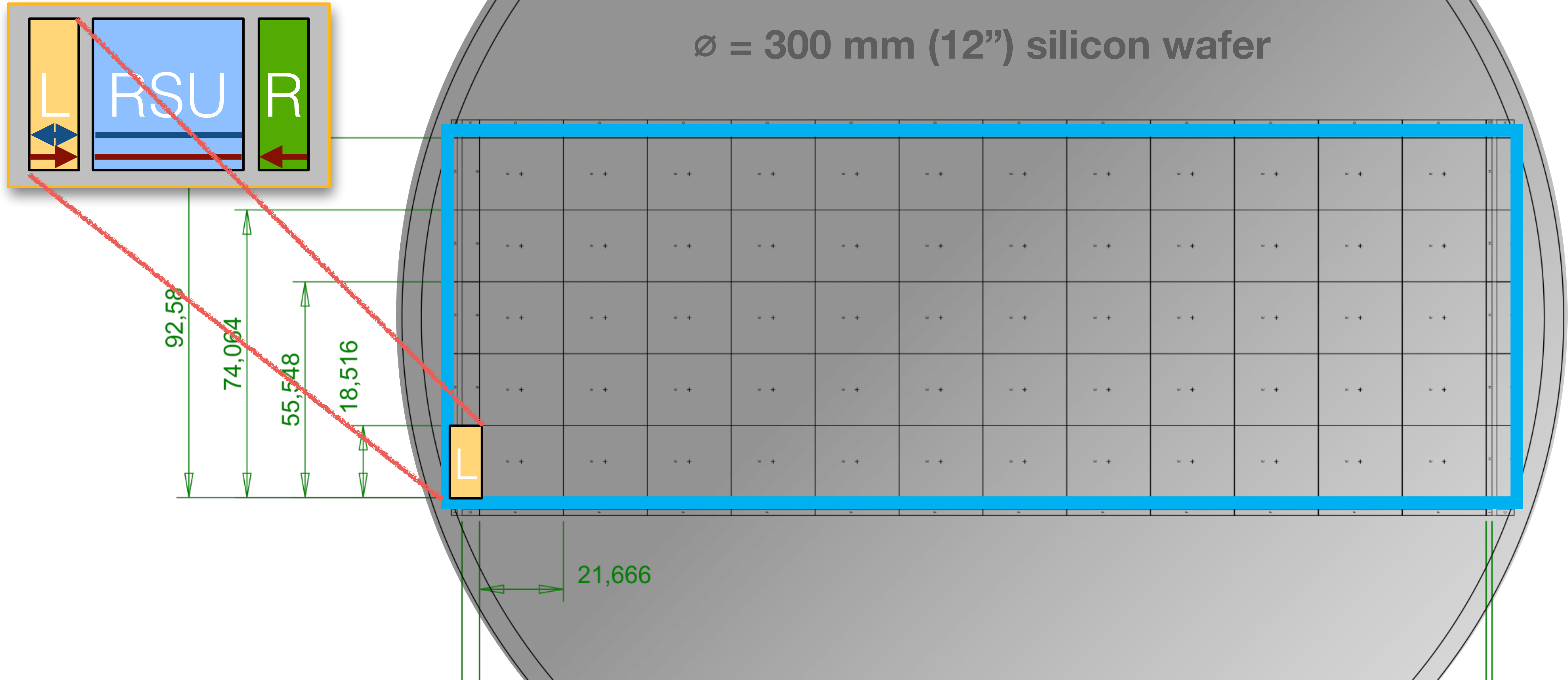
Stitching

Lithographic mask



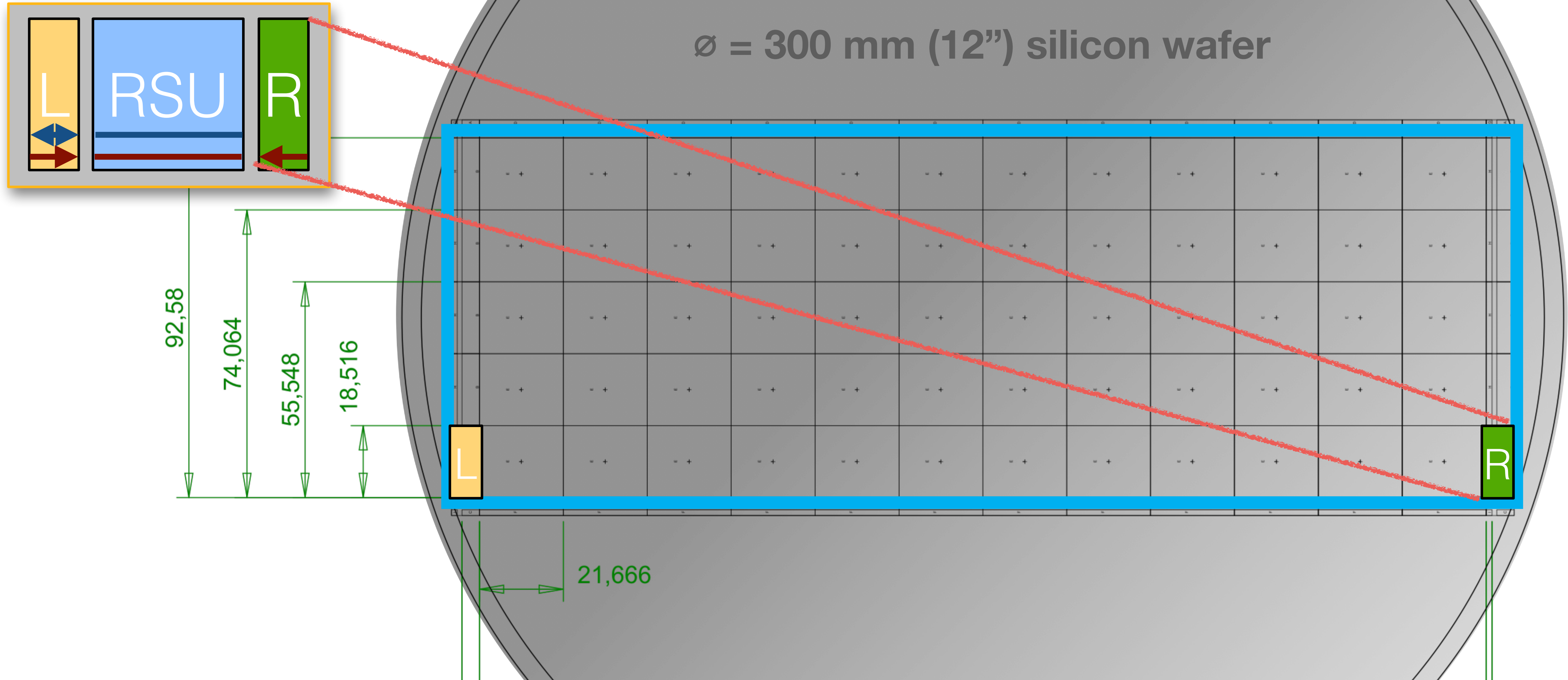
Stitching

Lithographic mask



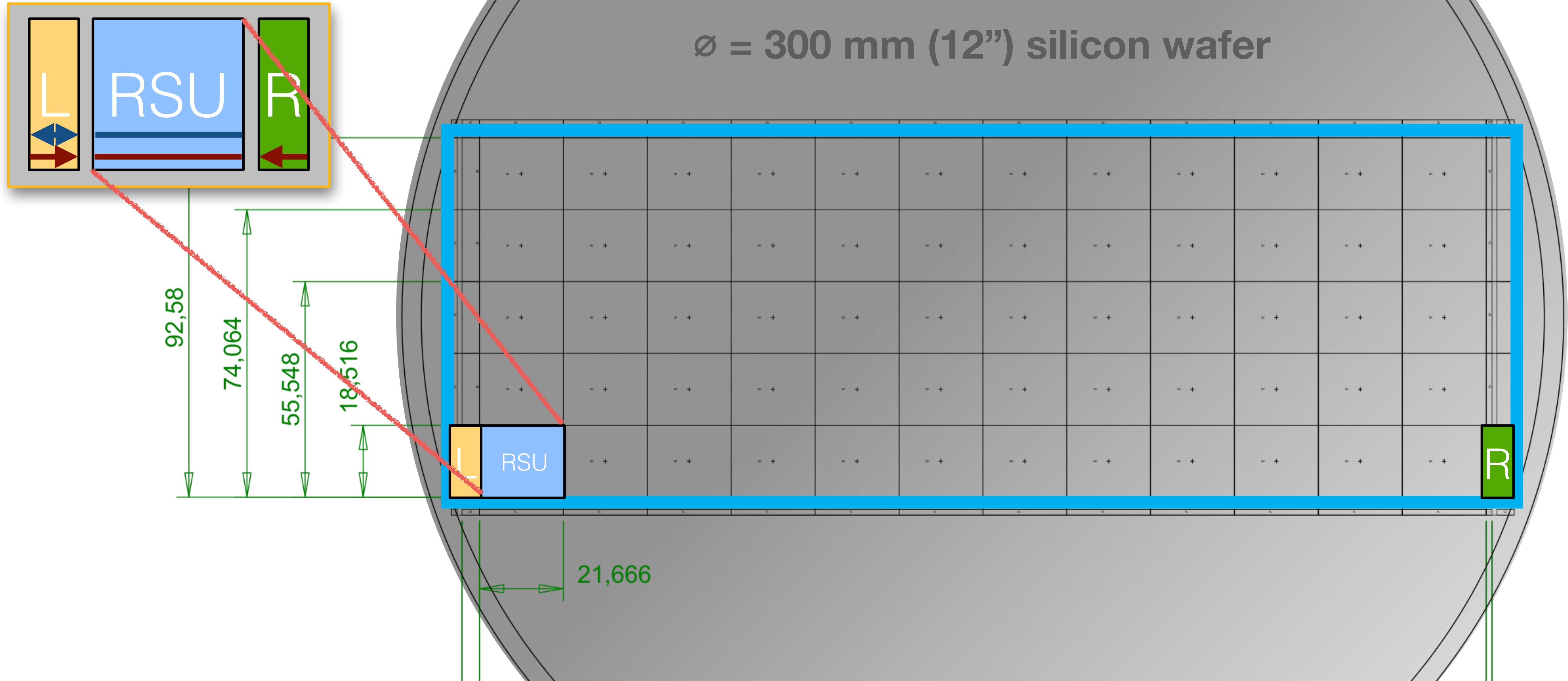
Stitching

Lithographic mask



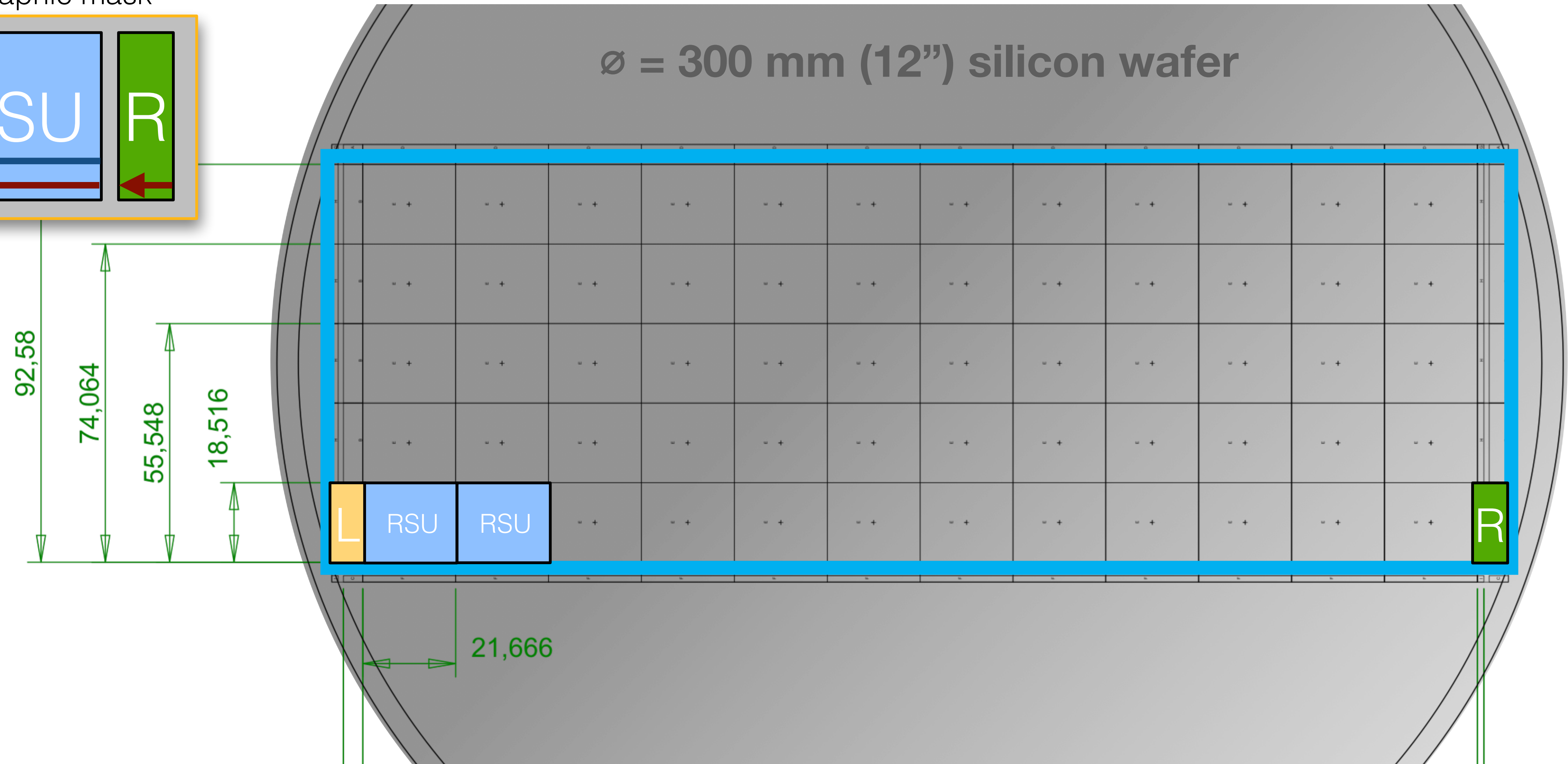
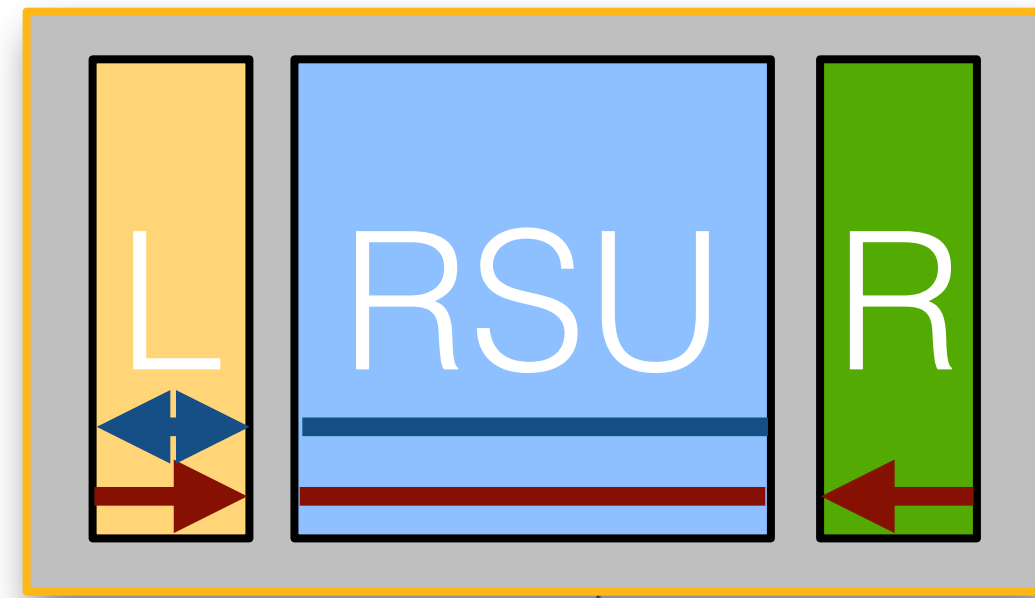
Stitching

Lithographic mask



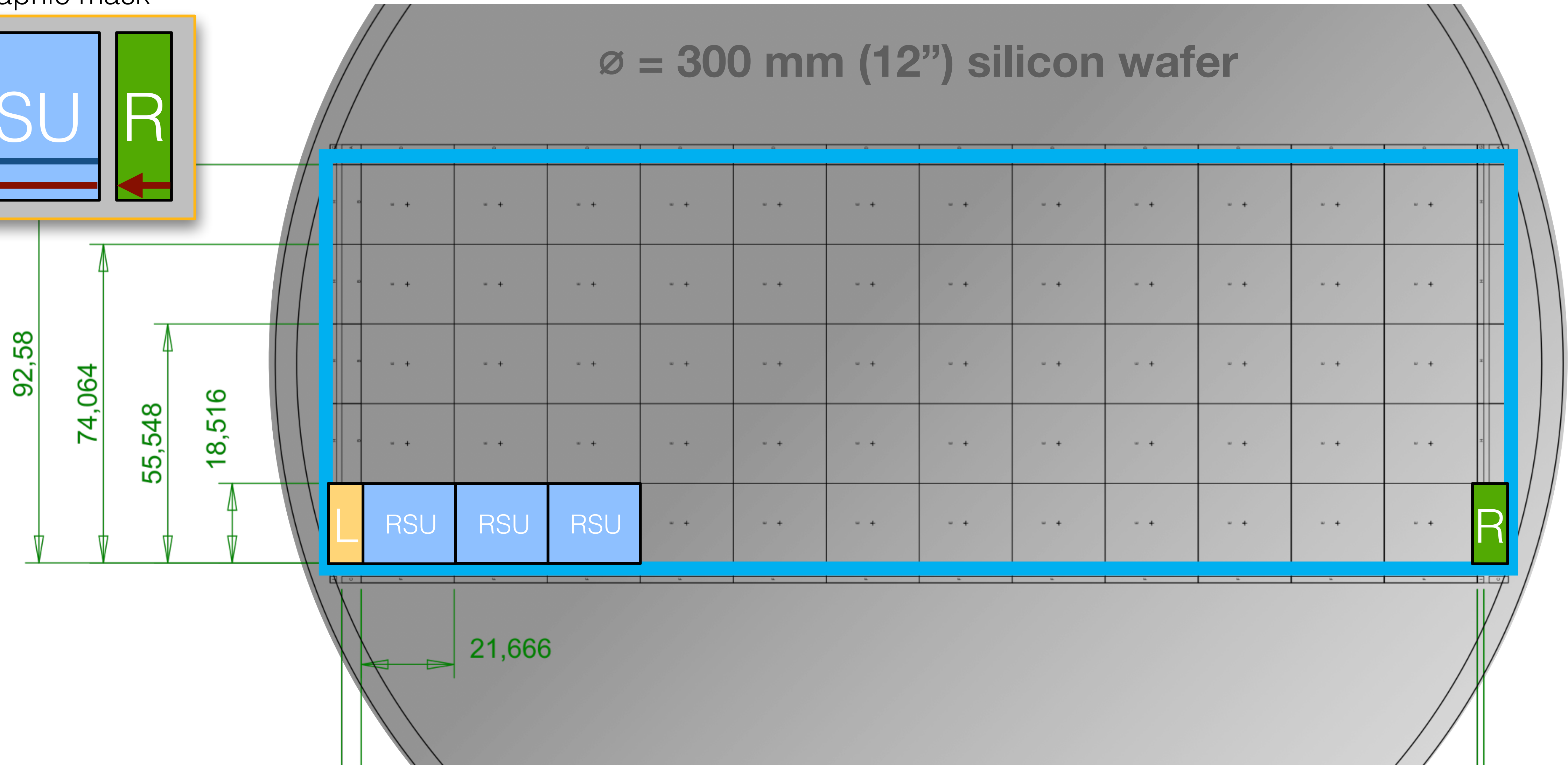
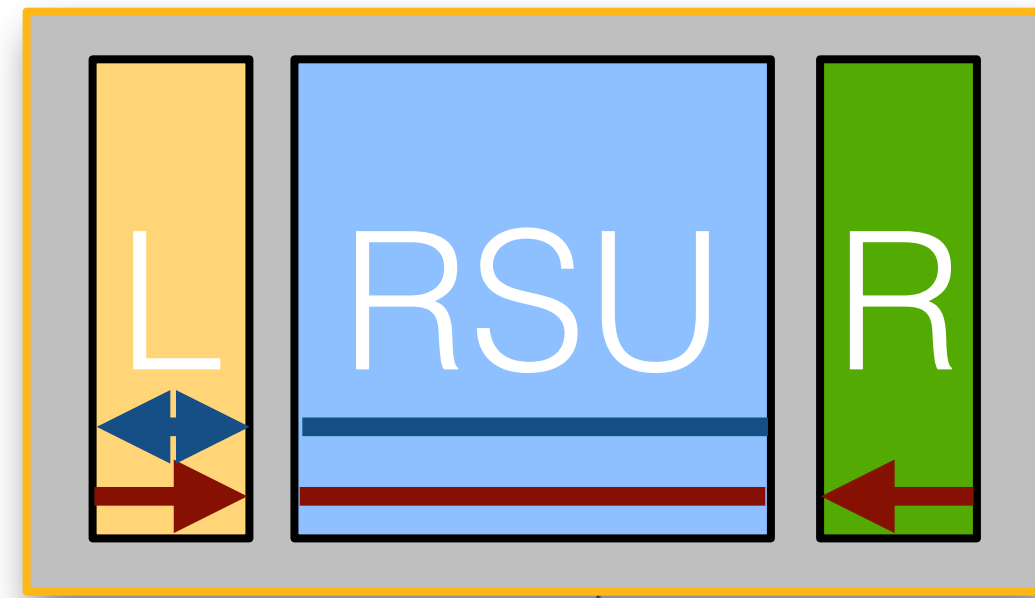
Stitching

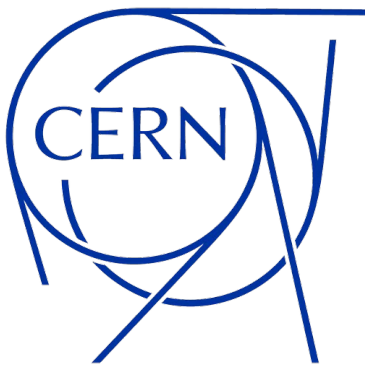
Lithographic mask



Stitching

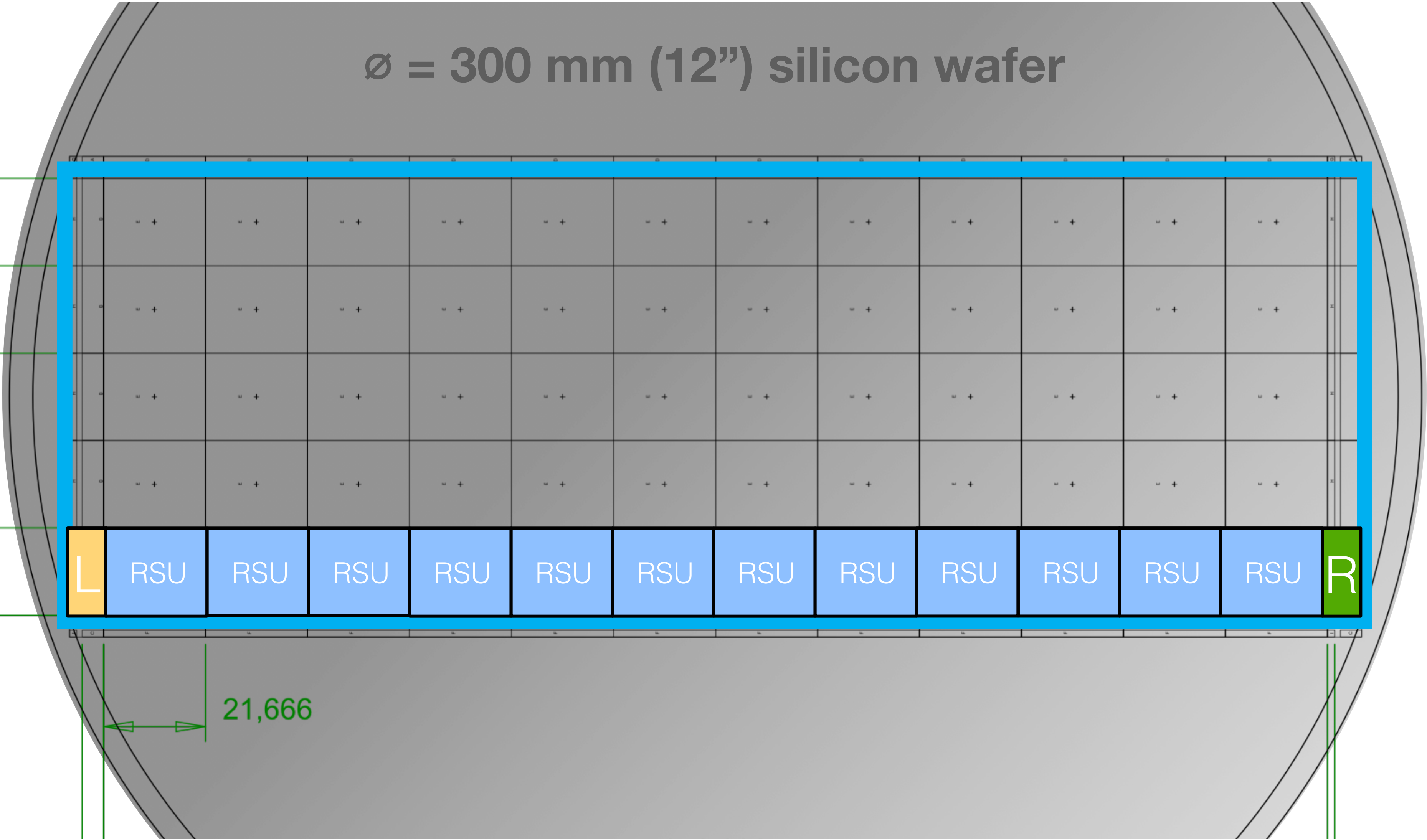
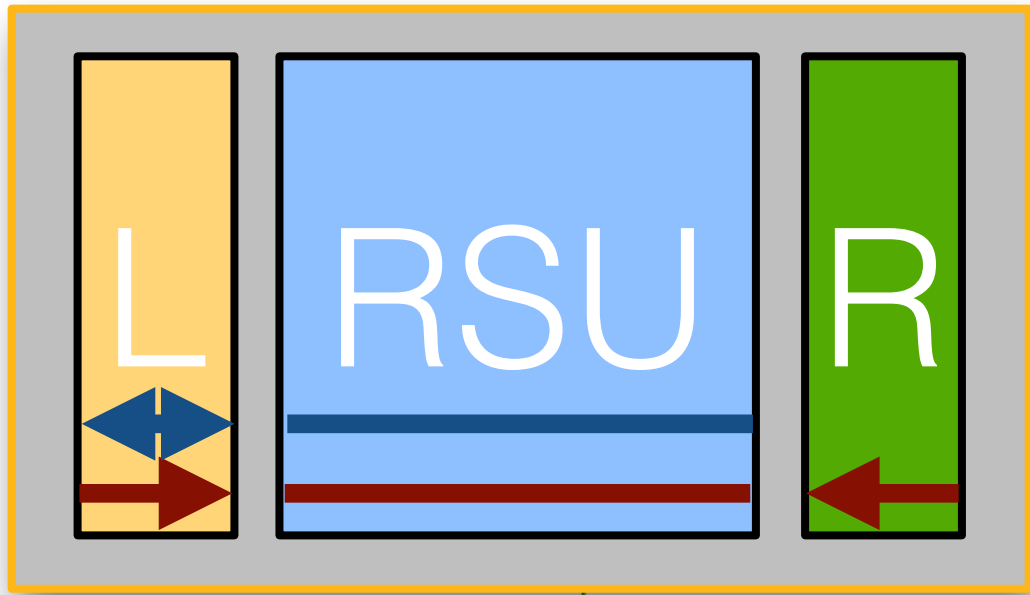
Lithographic mask

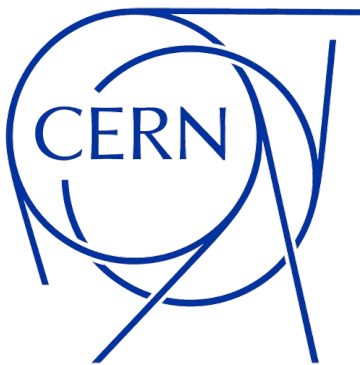




Stitching

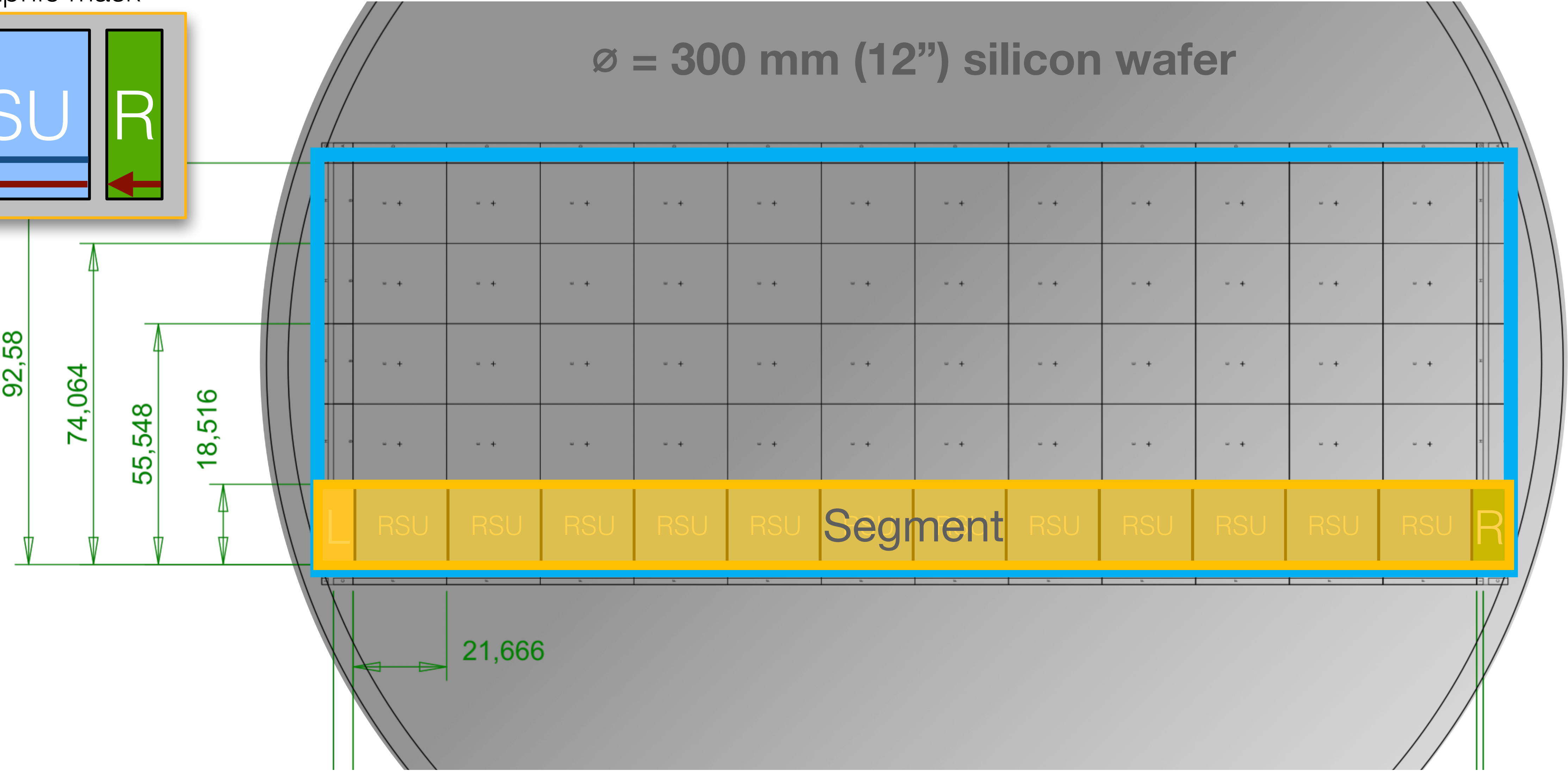
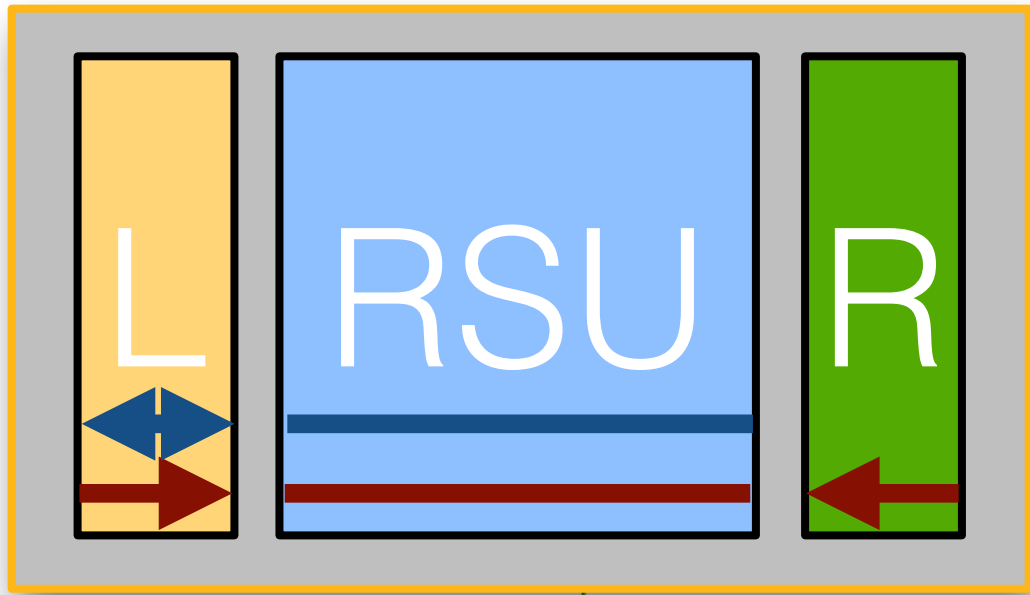
Lithographic mask

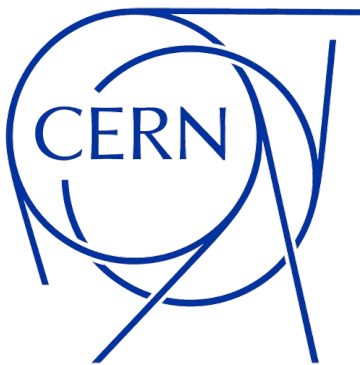




Stitching

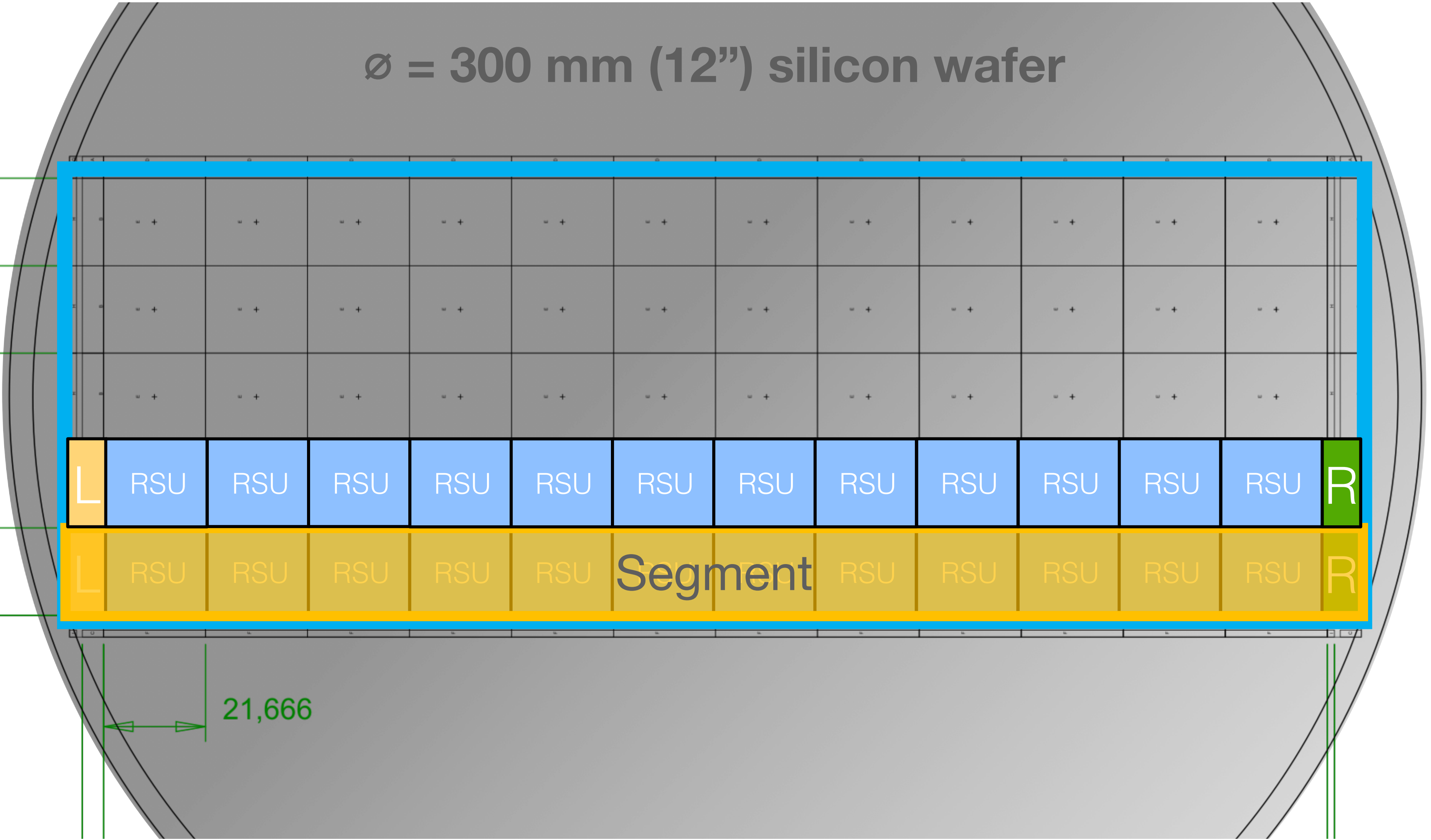
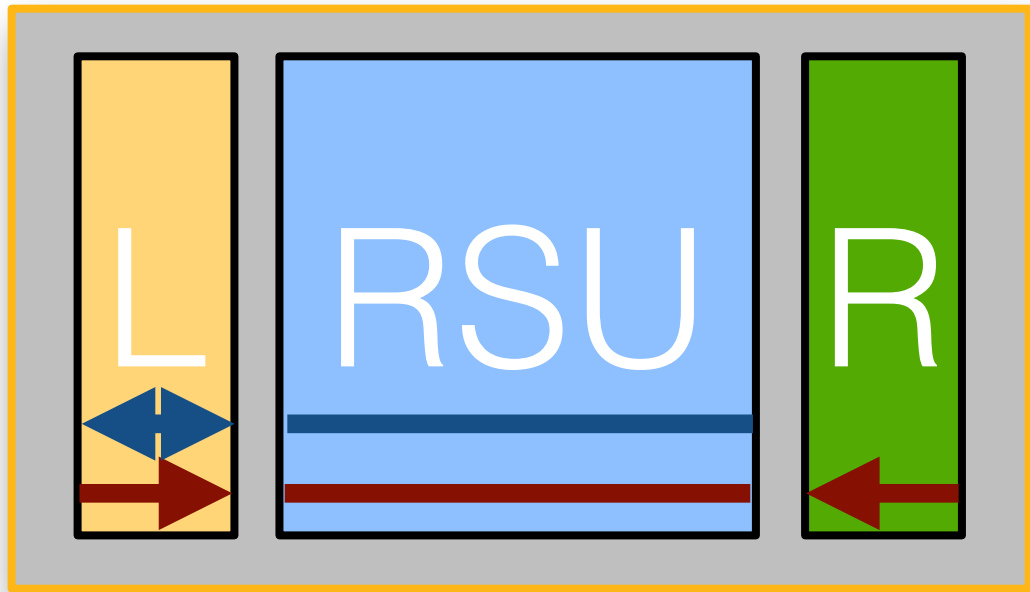
Lithographic mask

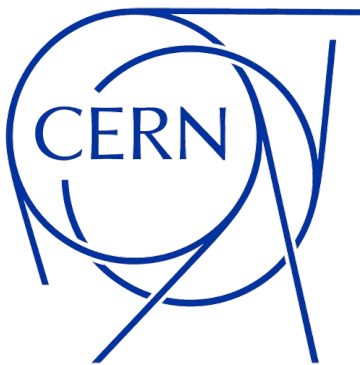




Stitching

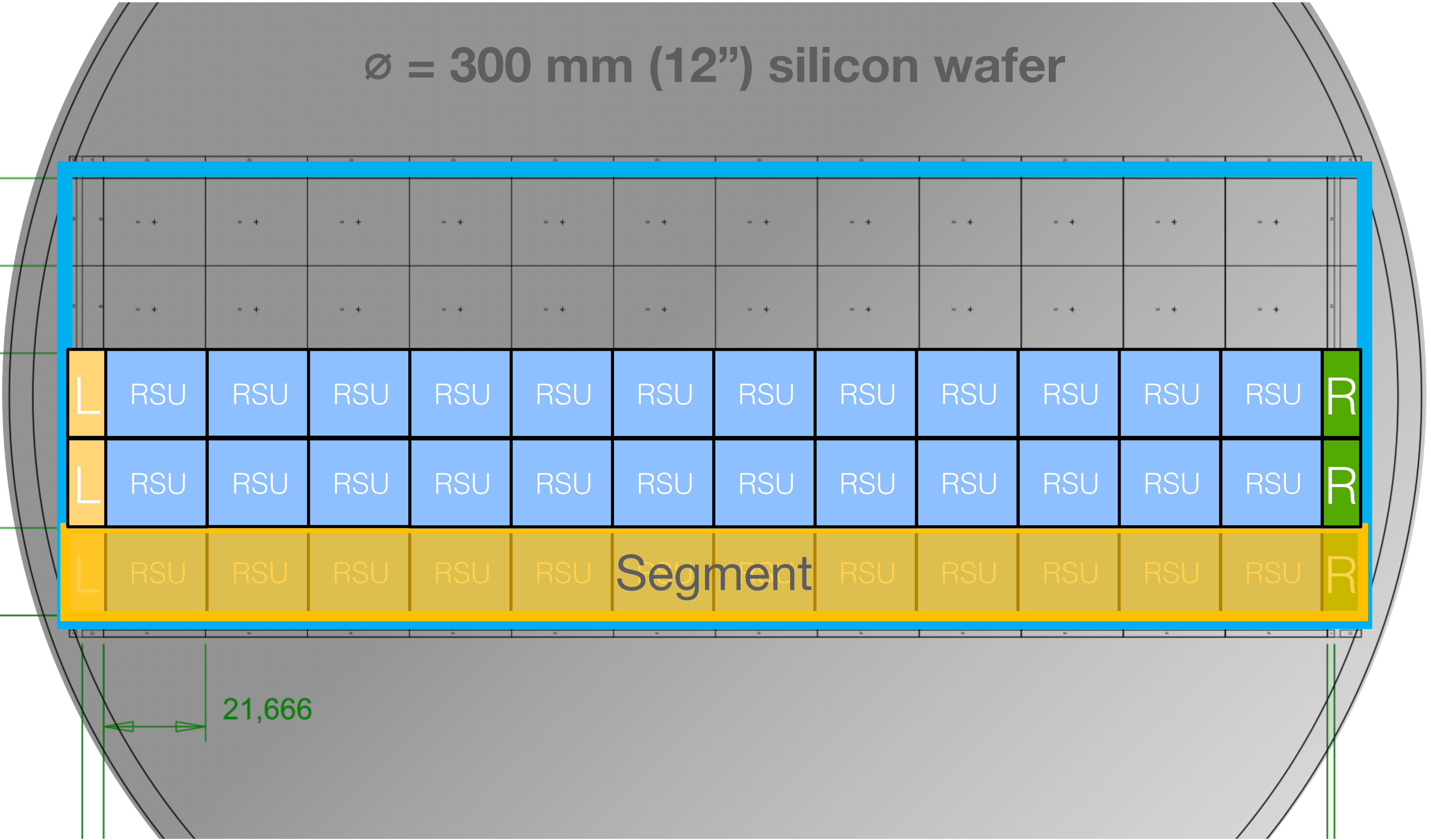
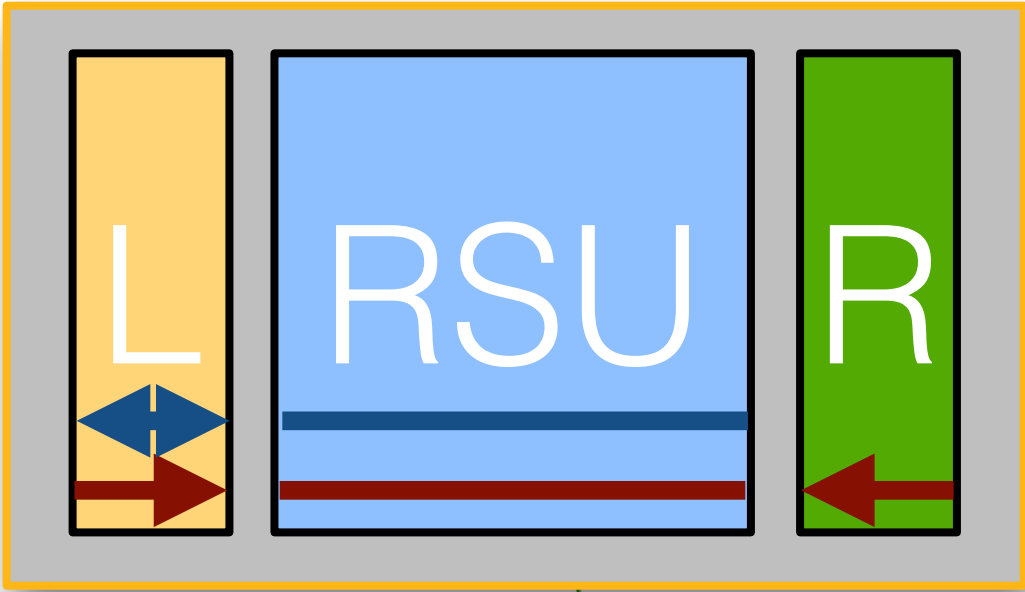
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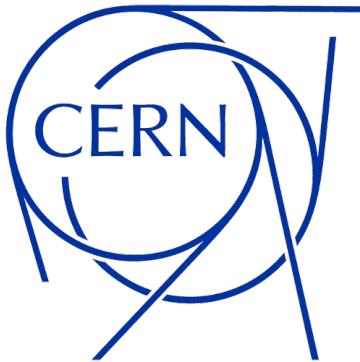




Stitching

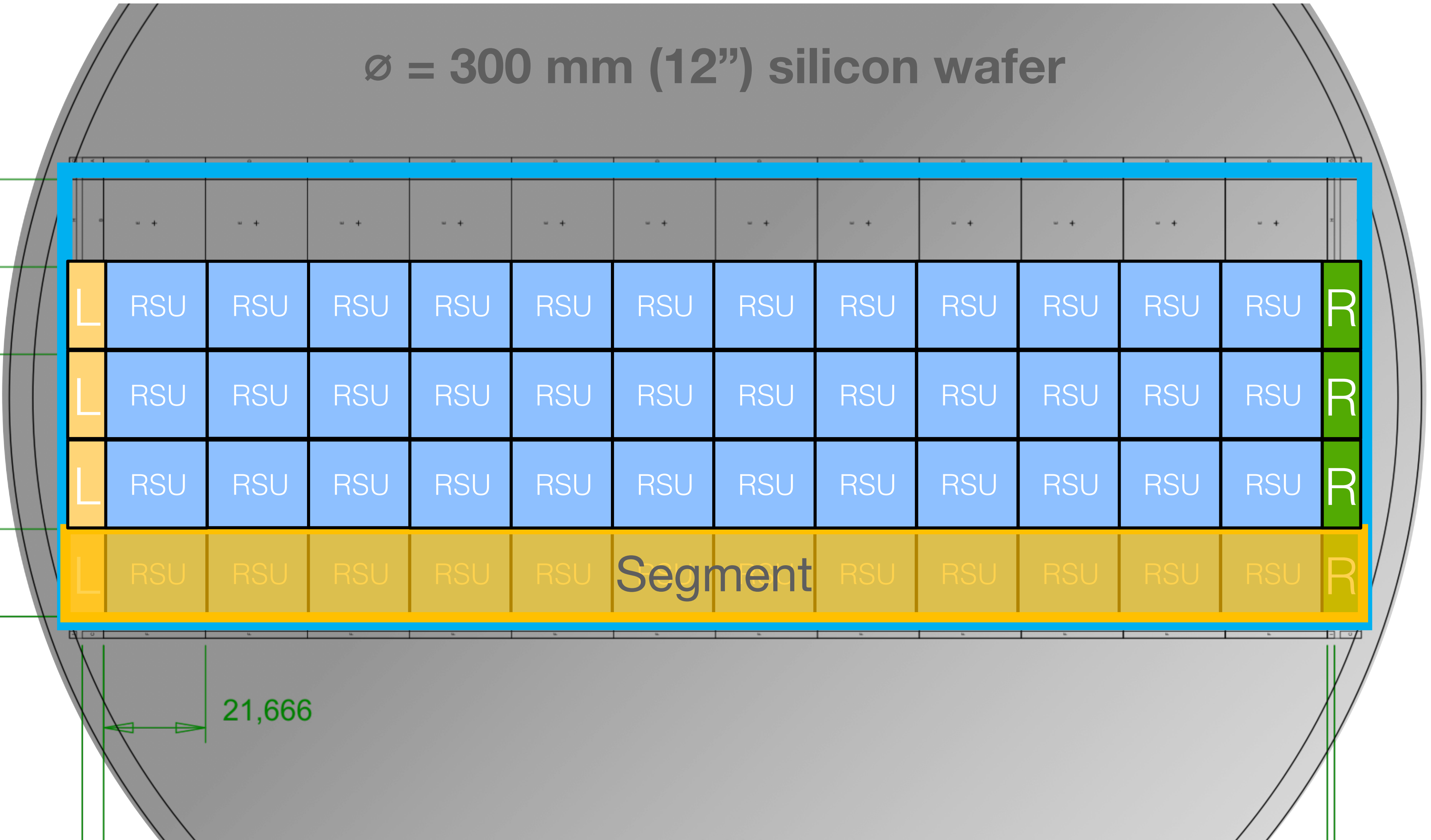
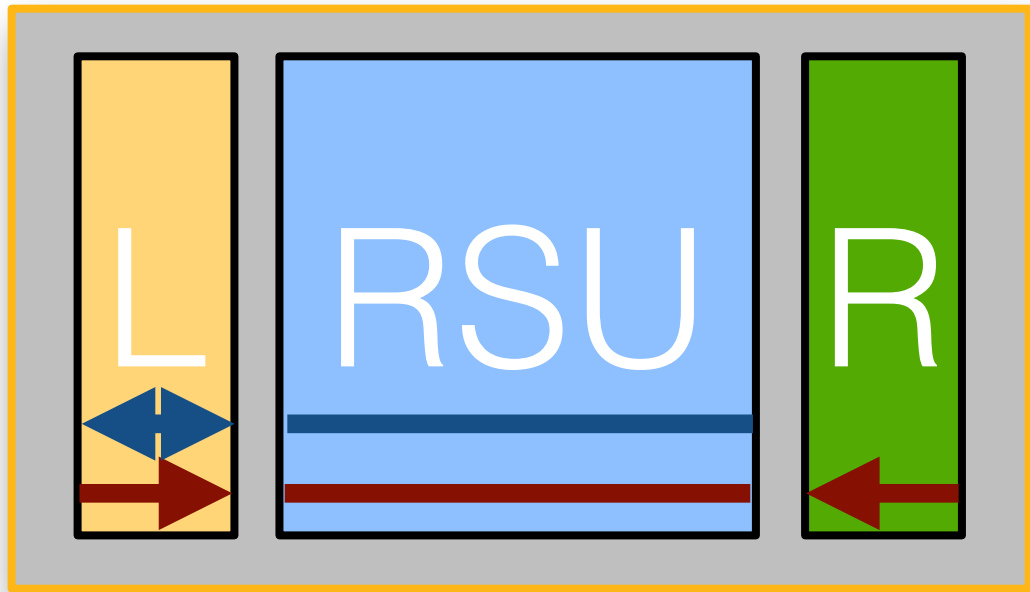
Lithographic mask





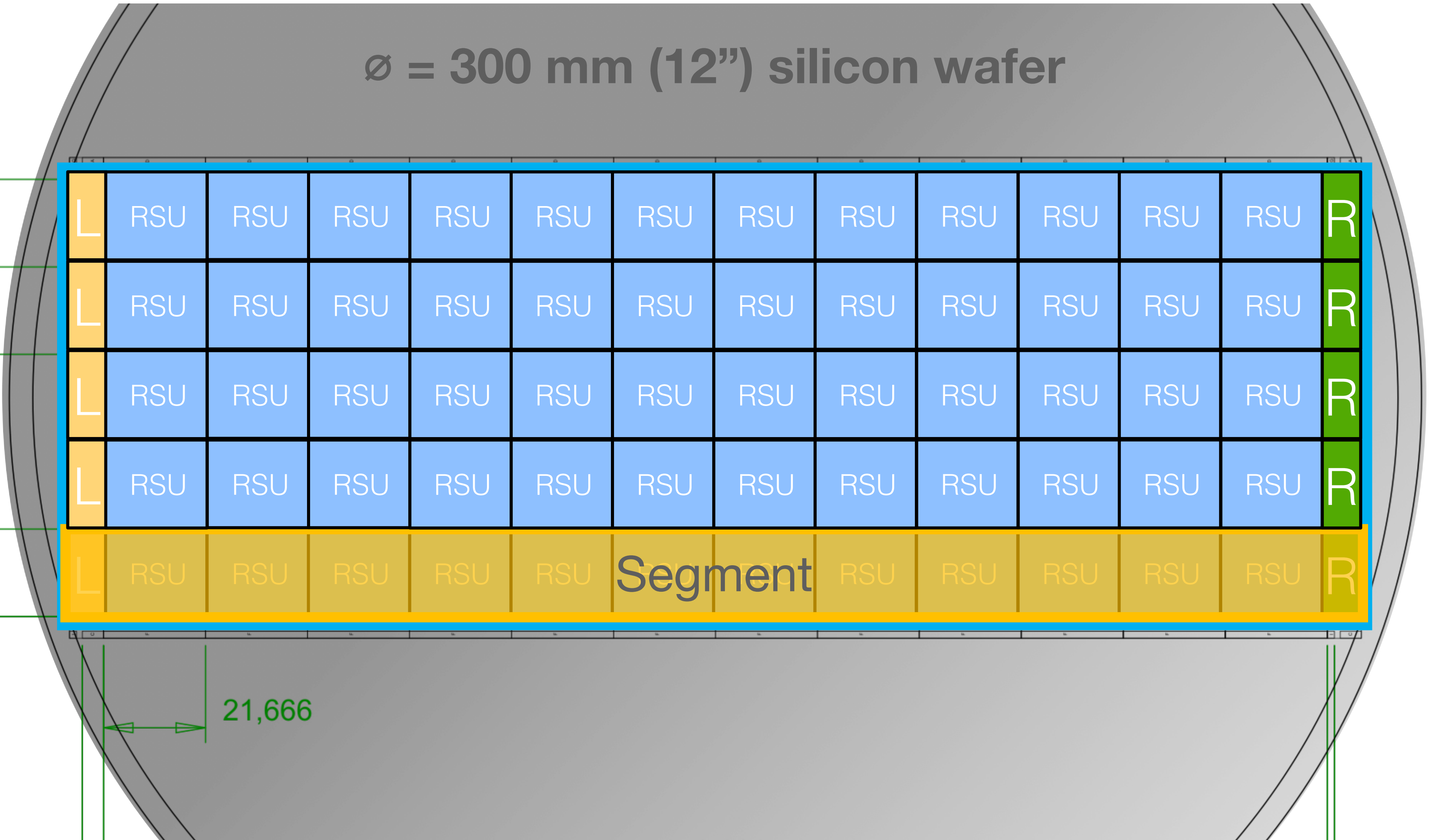
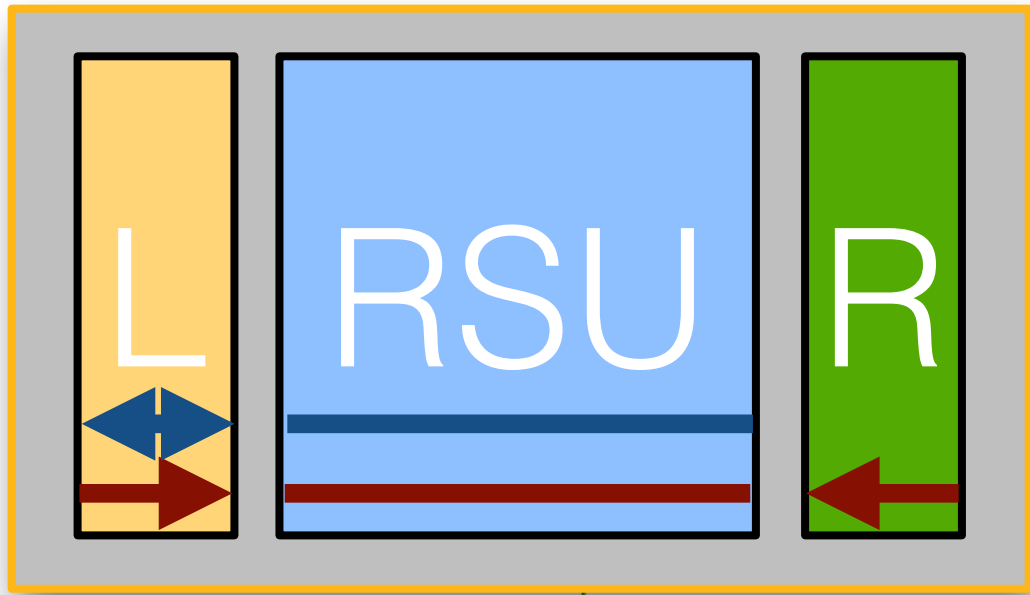
Stitching

Lithographic mask



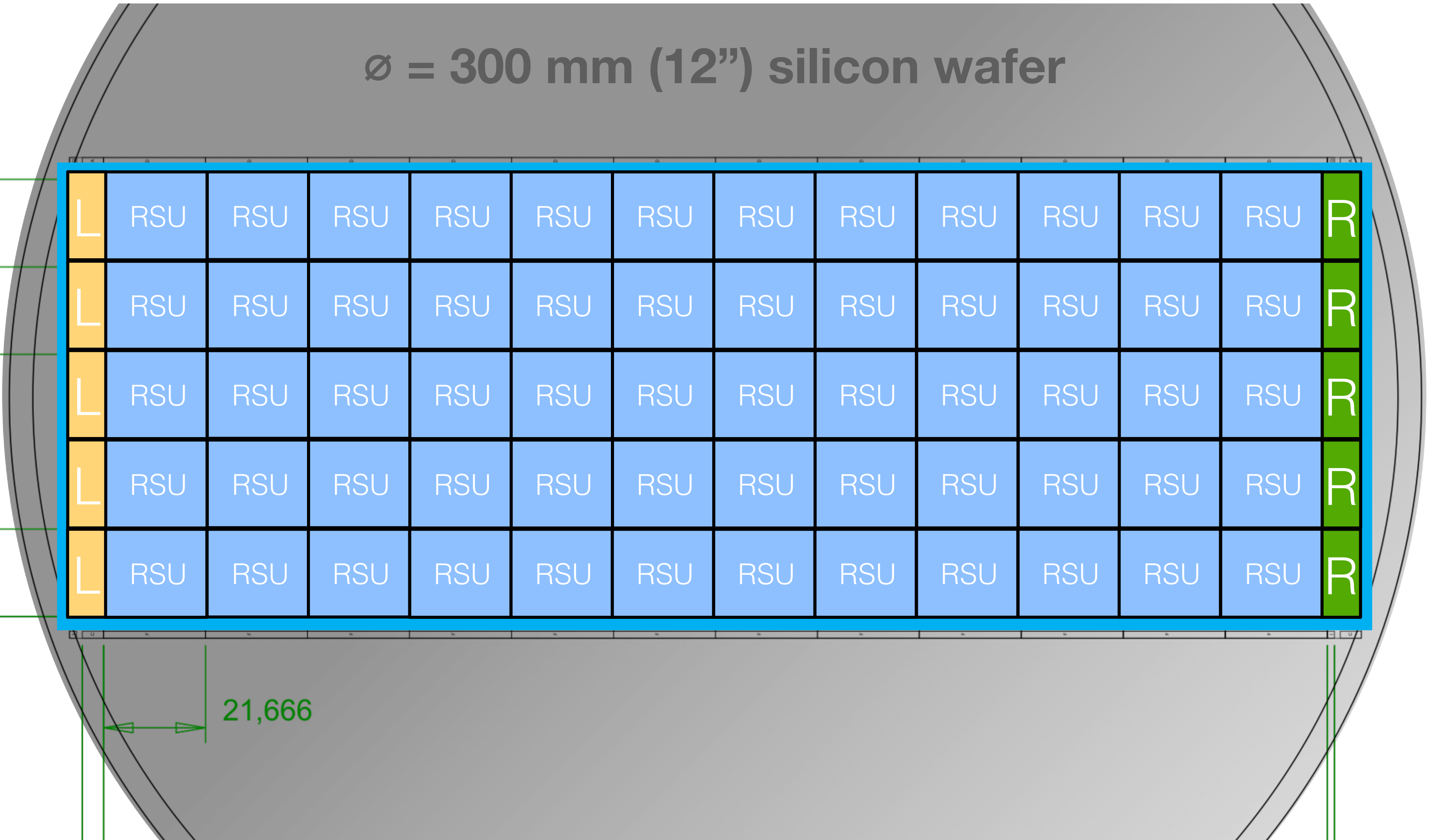
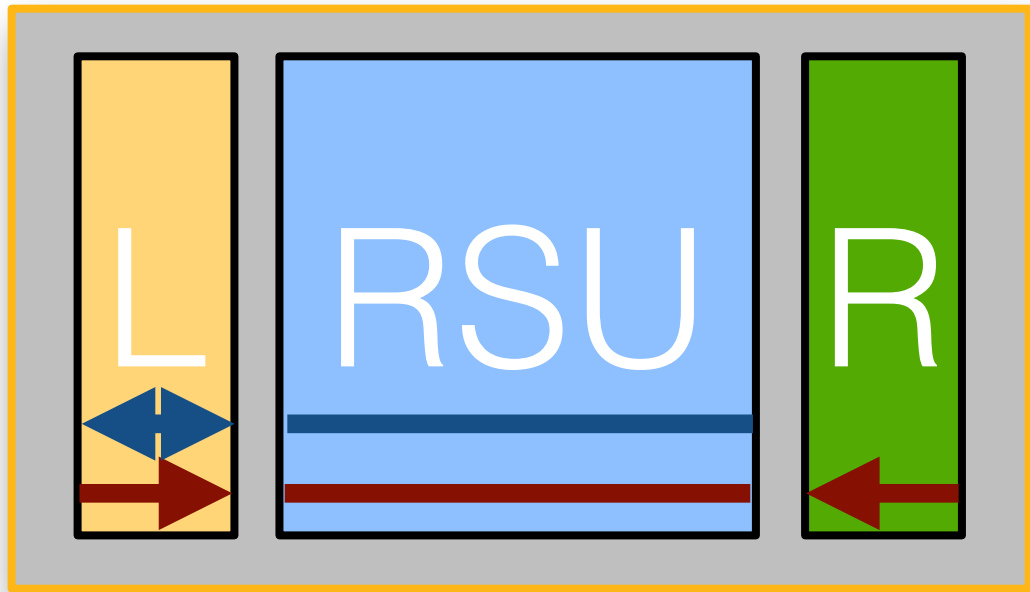
Stitching

Lithographic mask



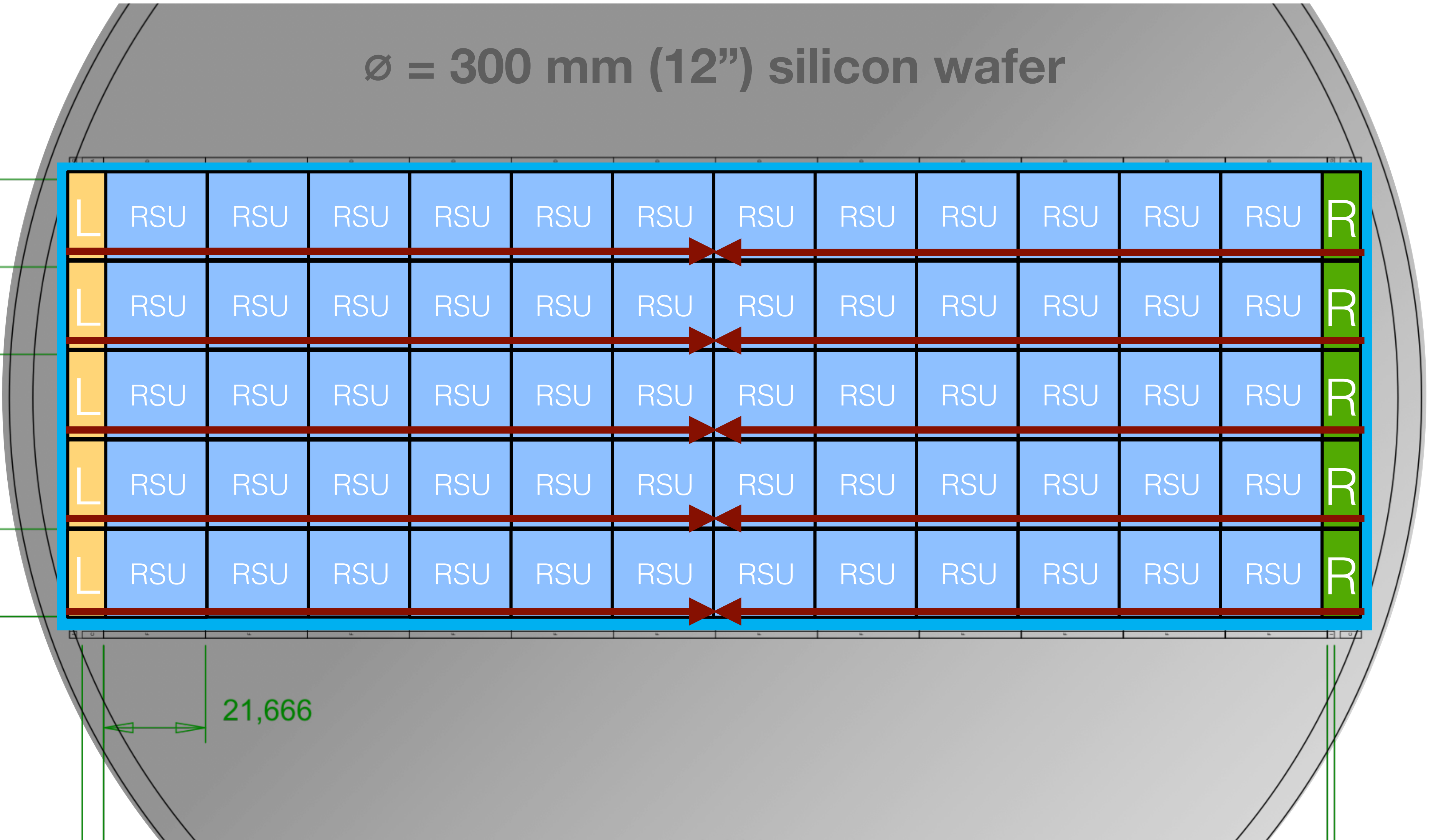
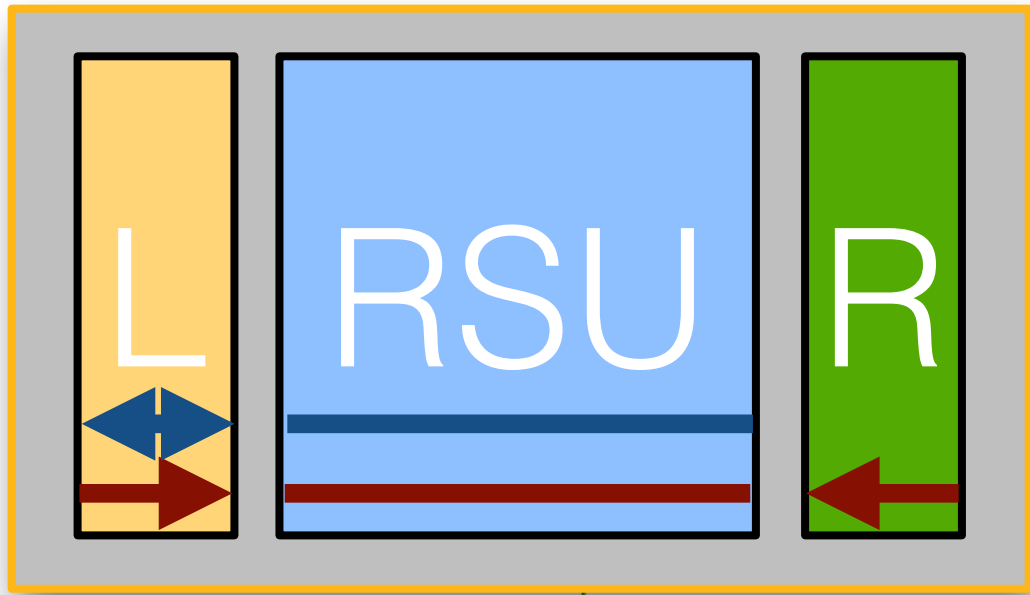
Stitching

Lithographic mask



Stitching

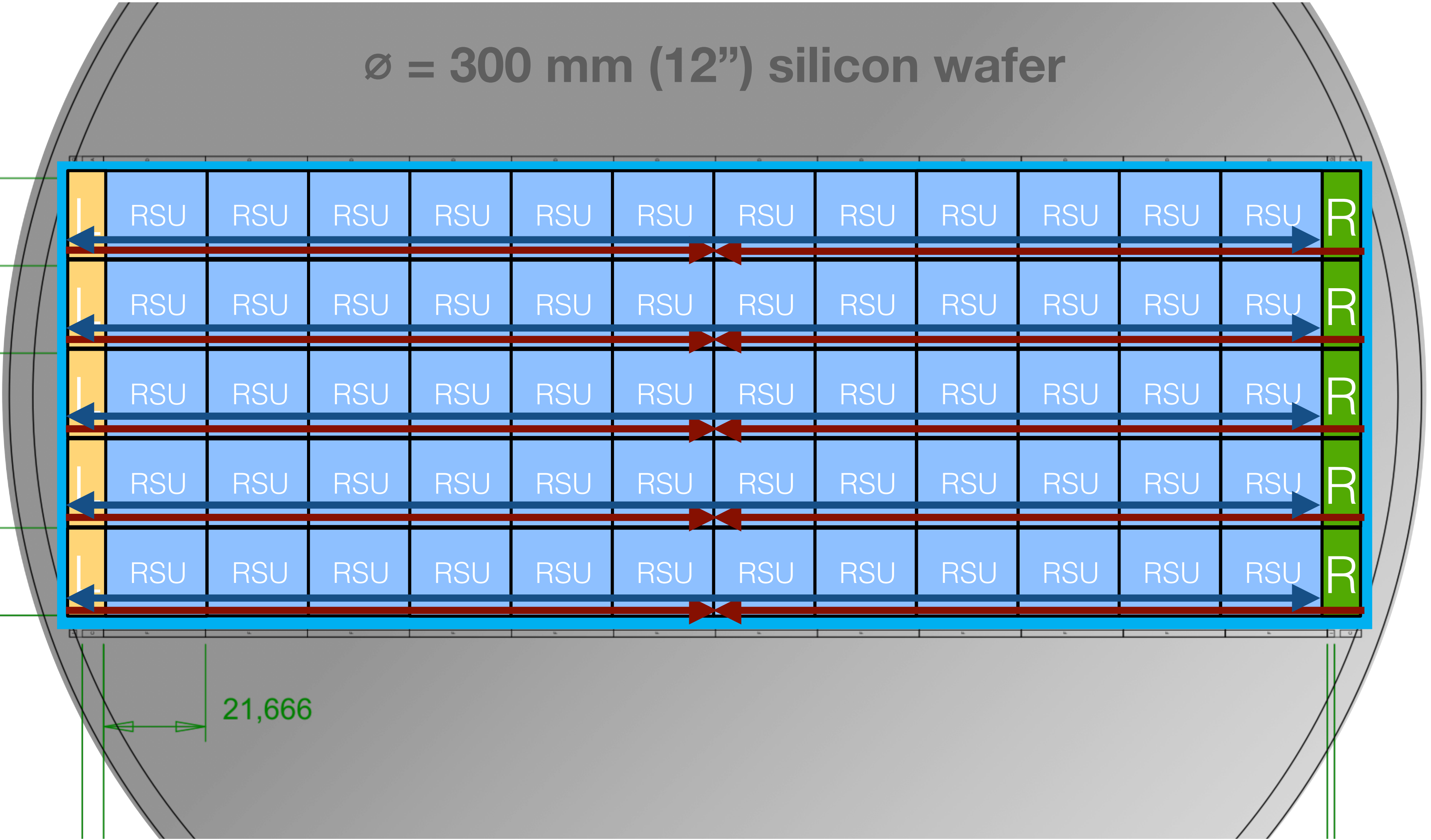
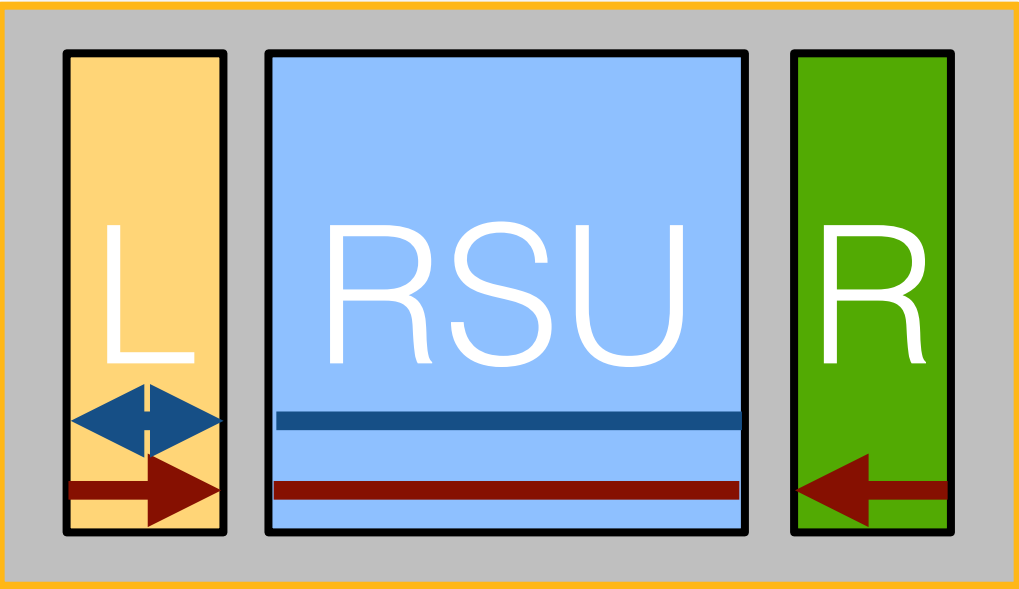
Lithographic mask



➡ Power supply

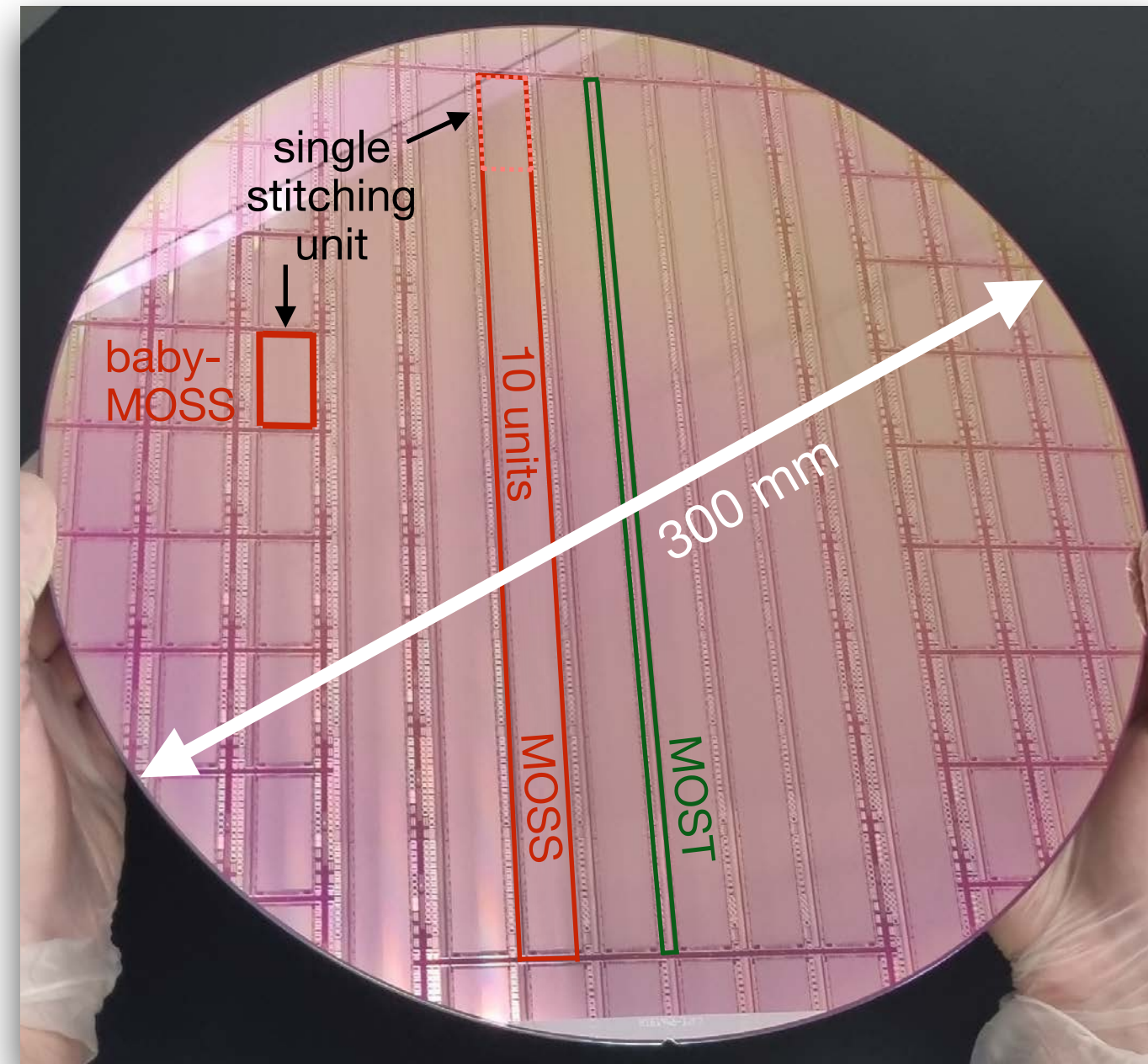
Stitching

Lithographic mask



 Power supply
 Data and control

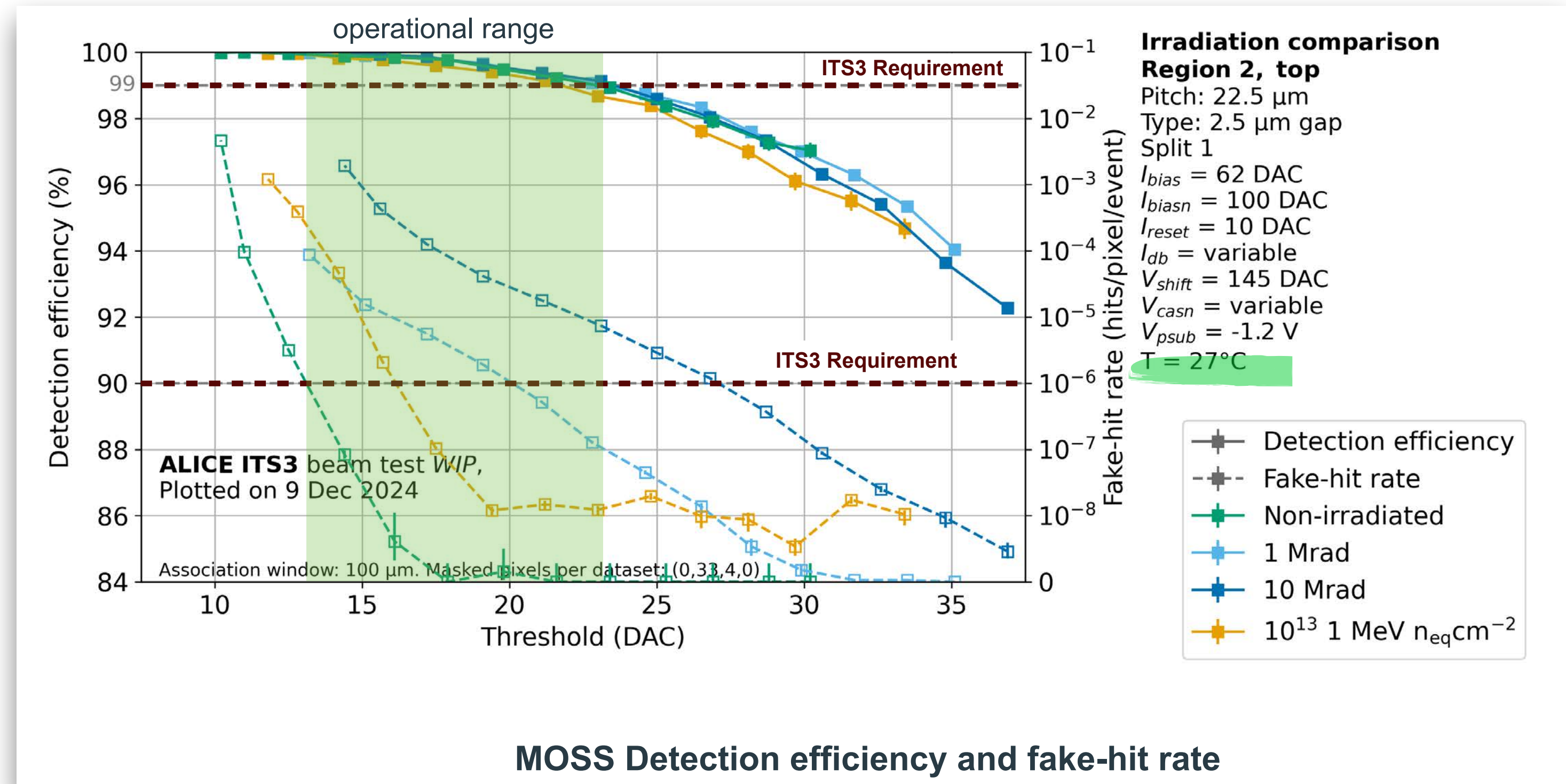
Stitched wafer-scale CMOS pixel sensors — current results



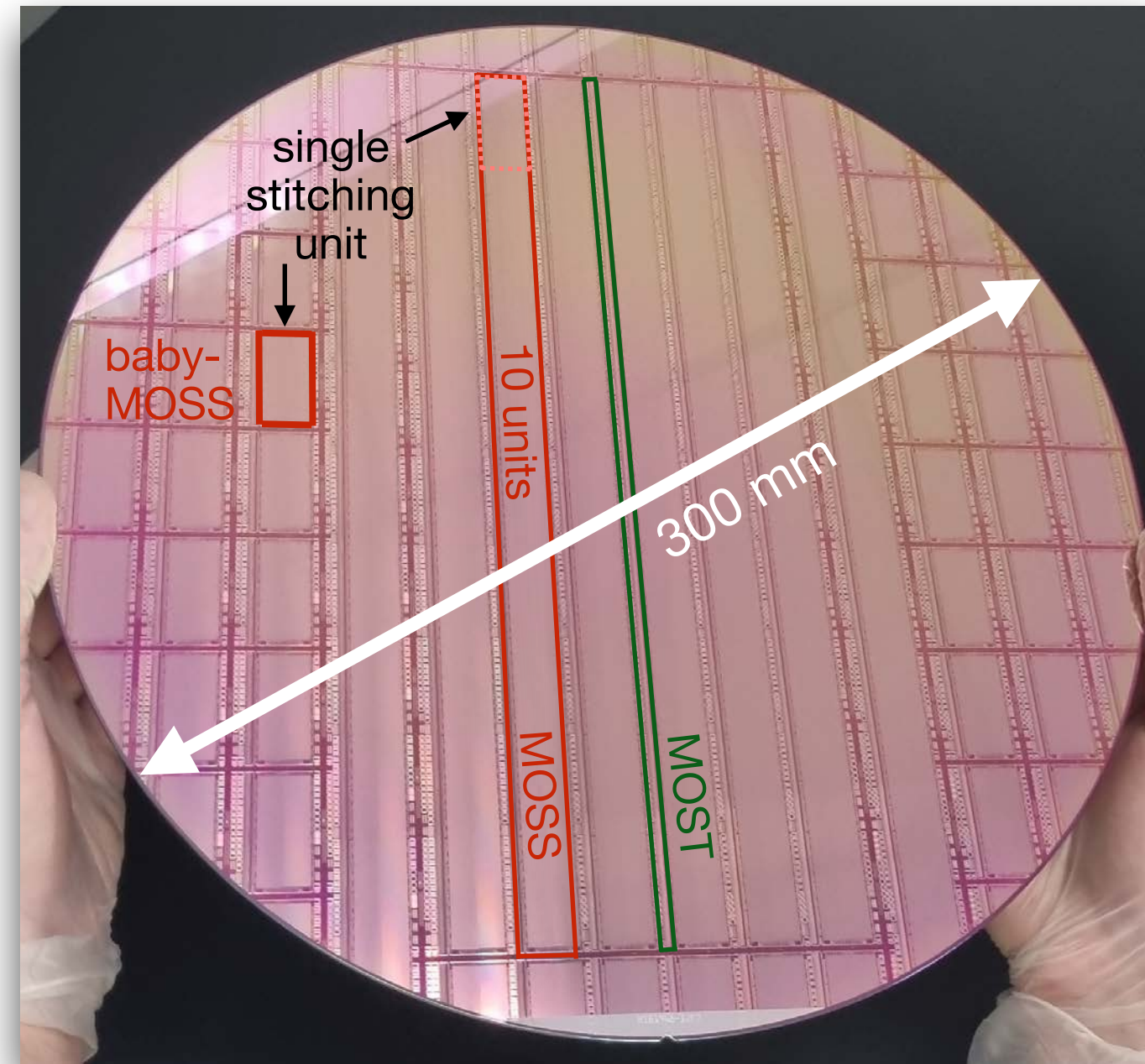
Engineering Run 1 wafer with various dies

Monolithic Stitched Sensor (MOSS)

- First stitched MAPS for high-energy physics
- 10 Repeated Sensor Units (RSUs) stitched together: **259 mm x 14 mm per sensor**
- 2 pixel pitches (18 μm and 22.5 μm) and 5 front-end variants, a total of **6.72 MPixel** per chip
- Chip is **operational** and reaches **full efficiency**
- Yield currently being studied in detail, main failure mechanism expected to be mitigated in the next submission



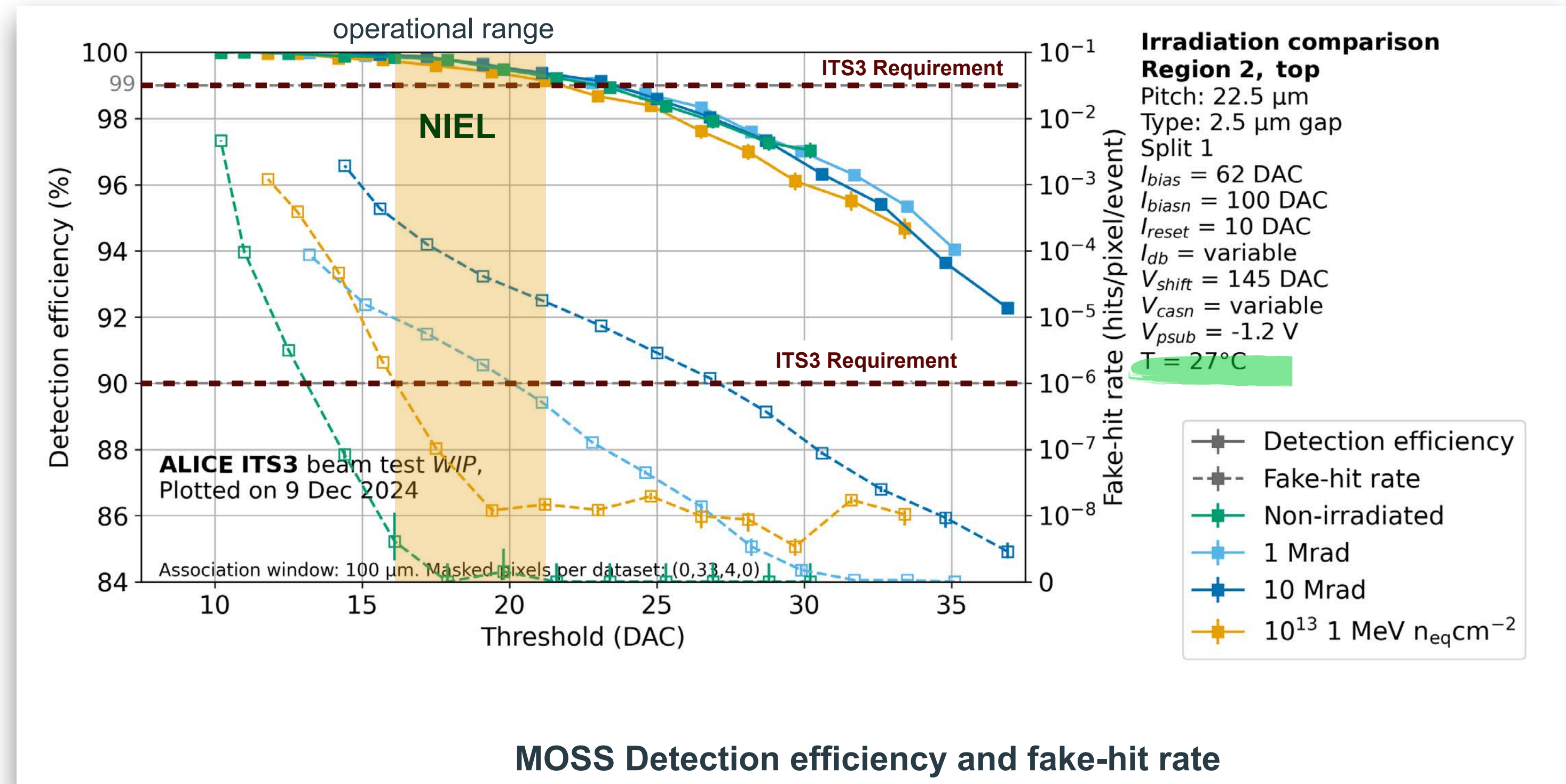
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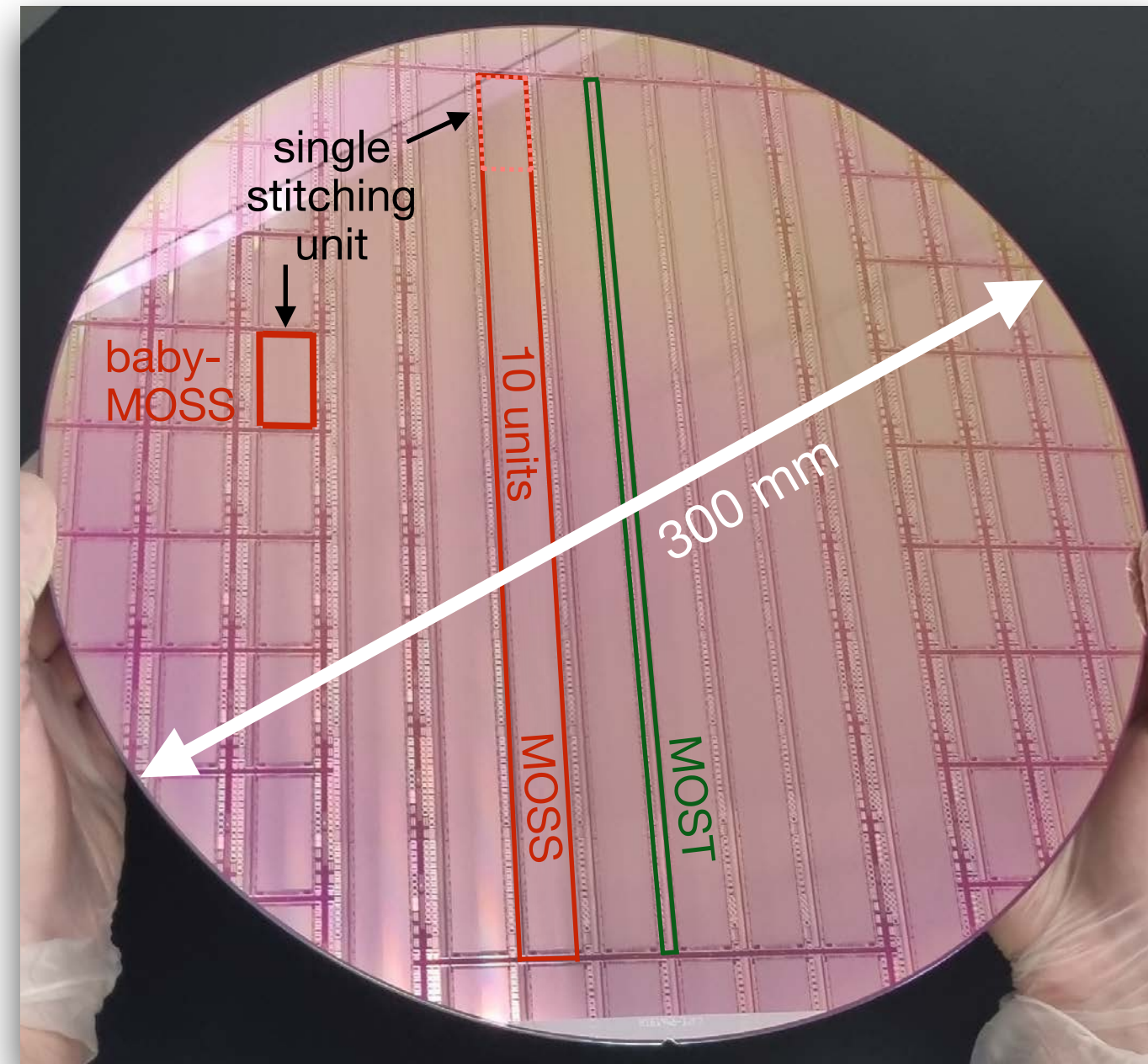
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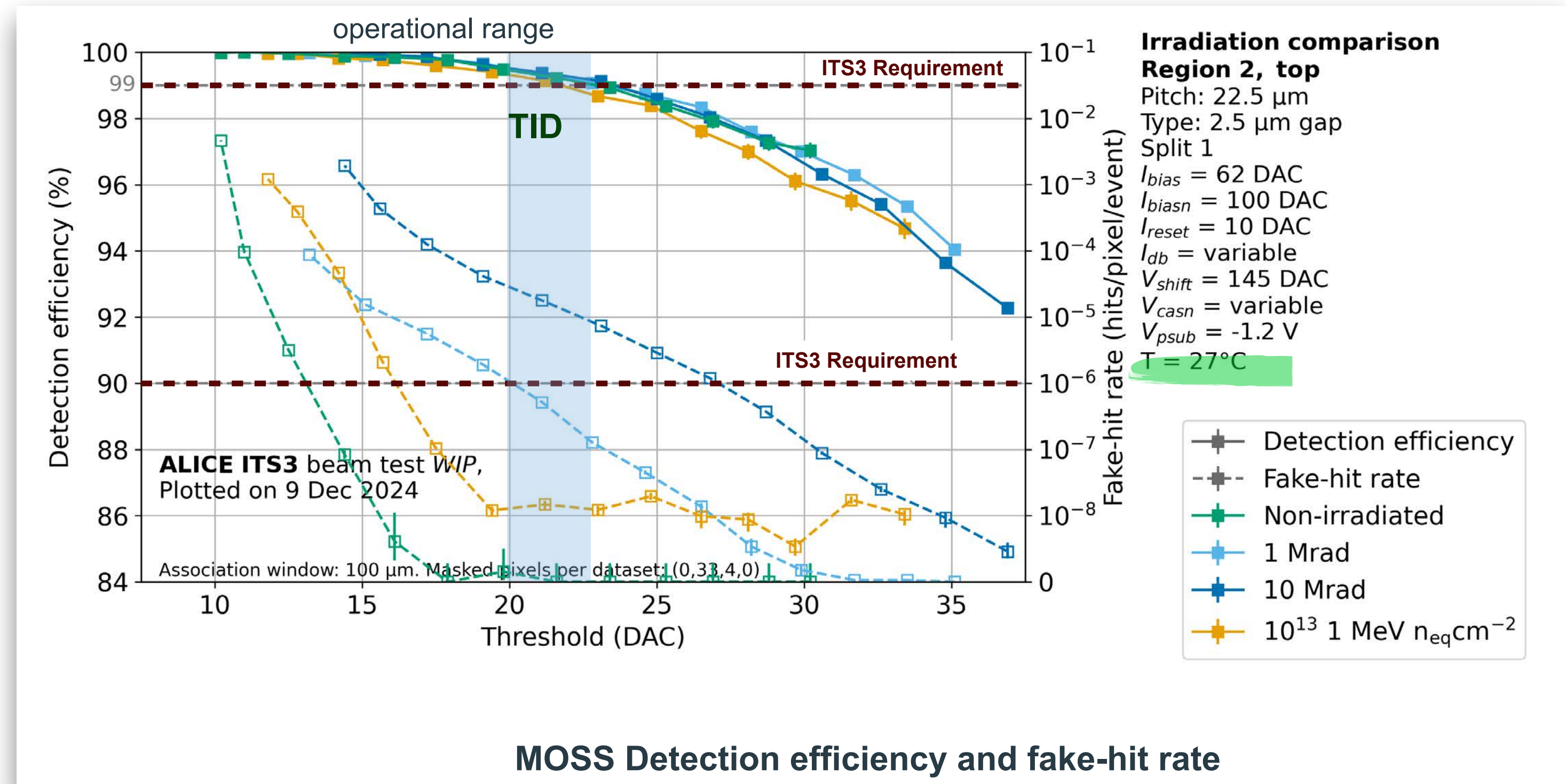
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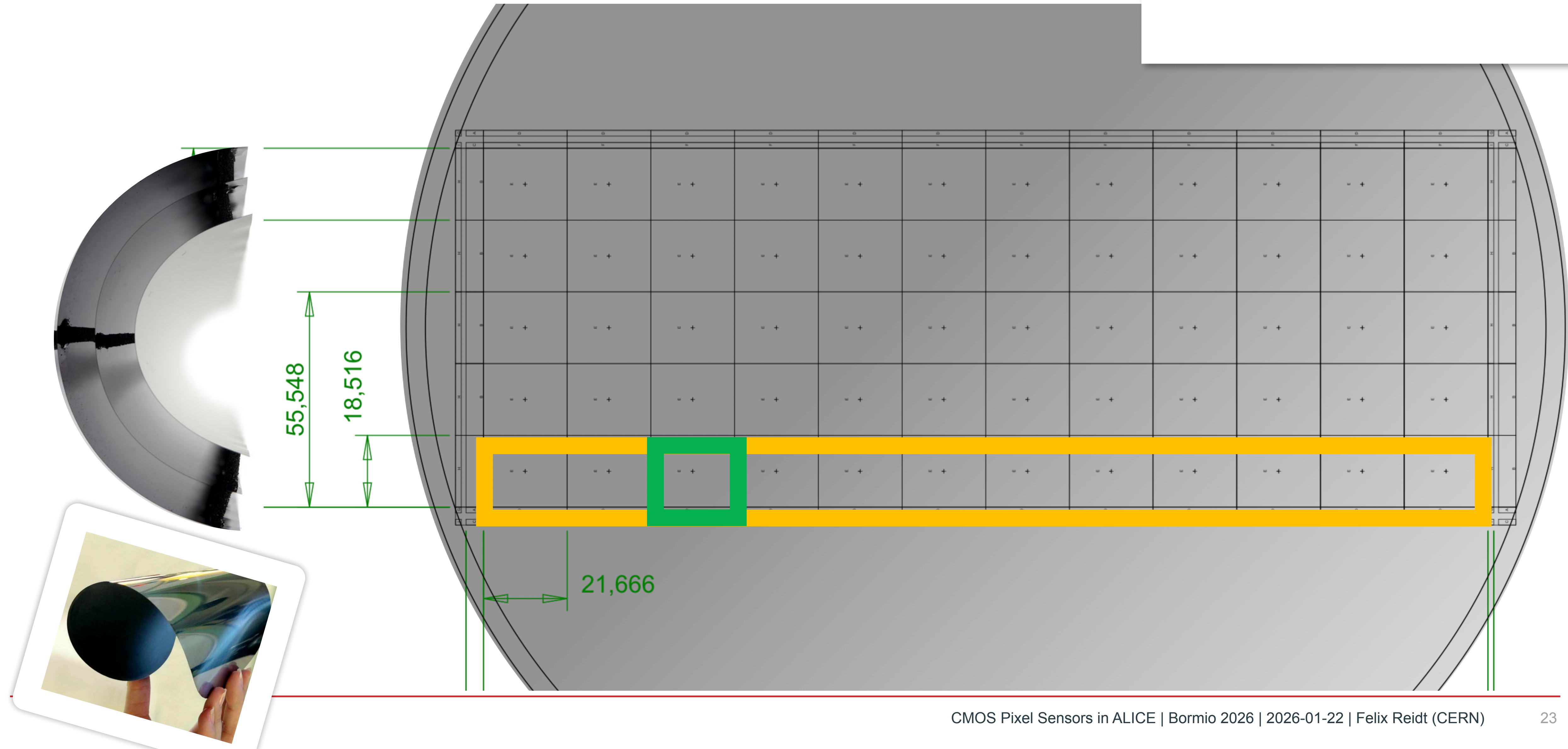
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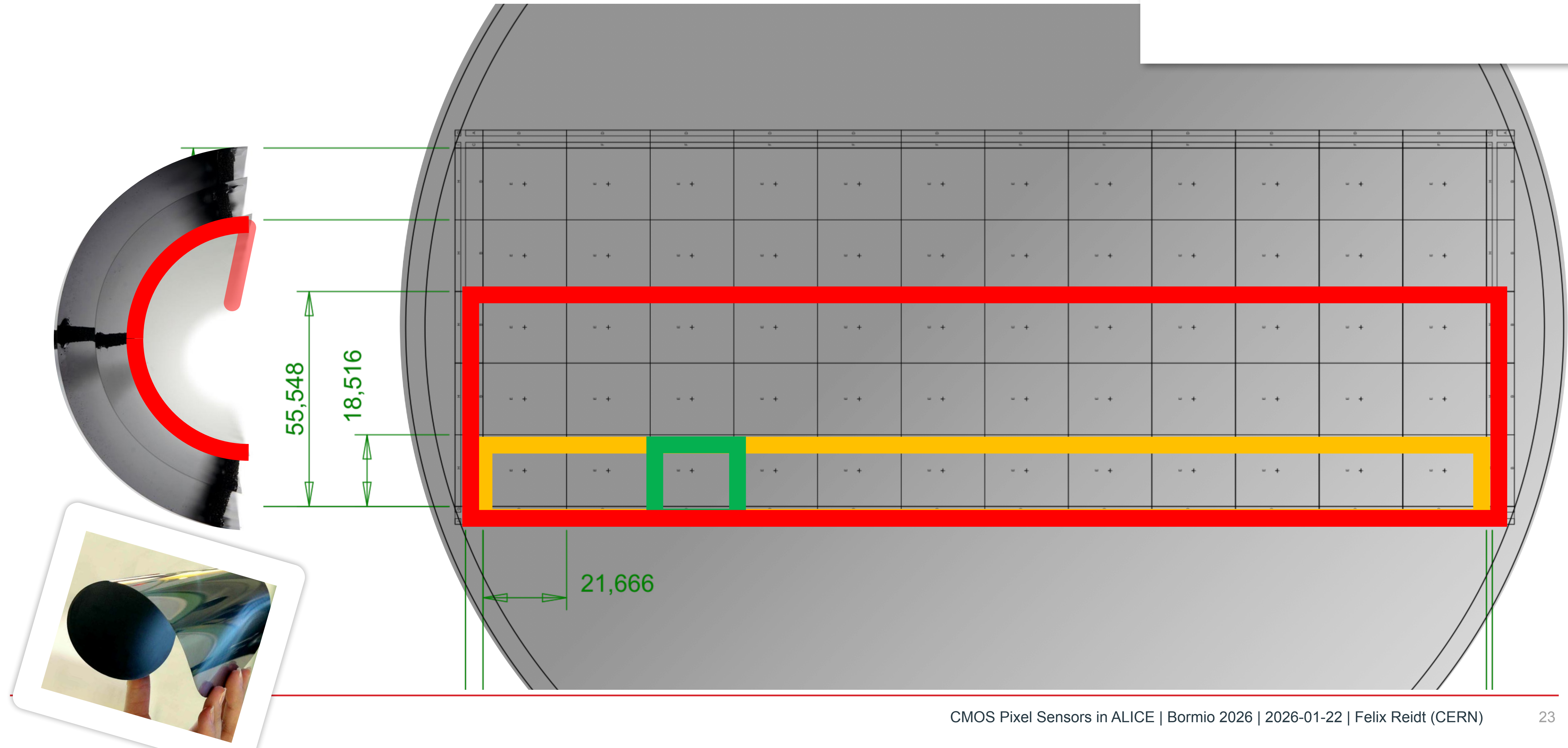
ITS3 Half-Layers

- Segment 12 RSUs + endcaps
- Repeated Sensor Unit



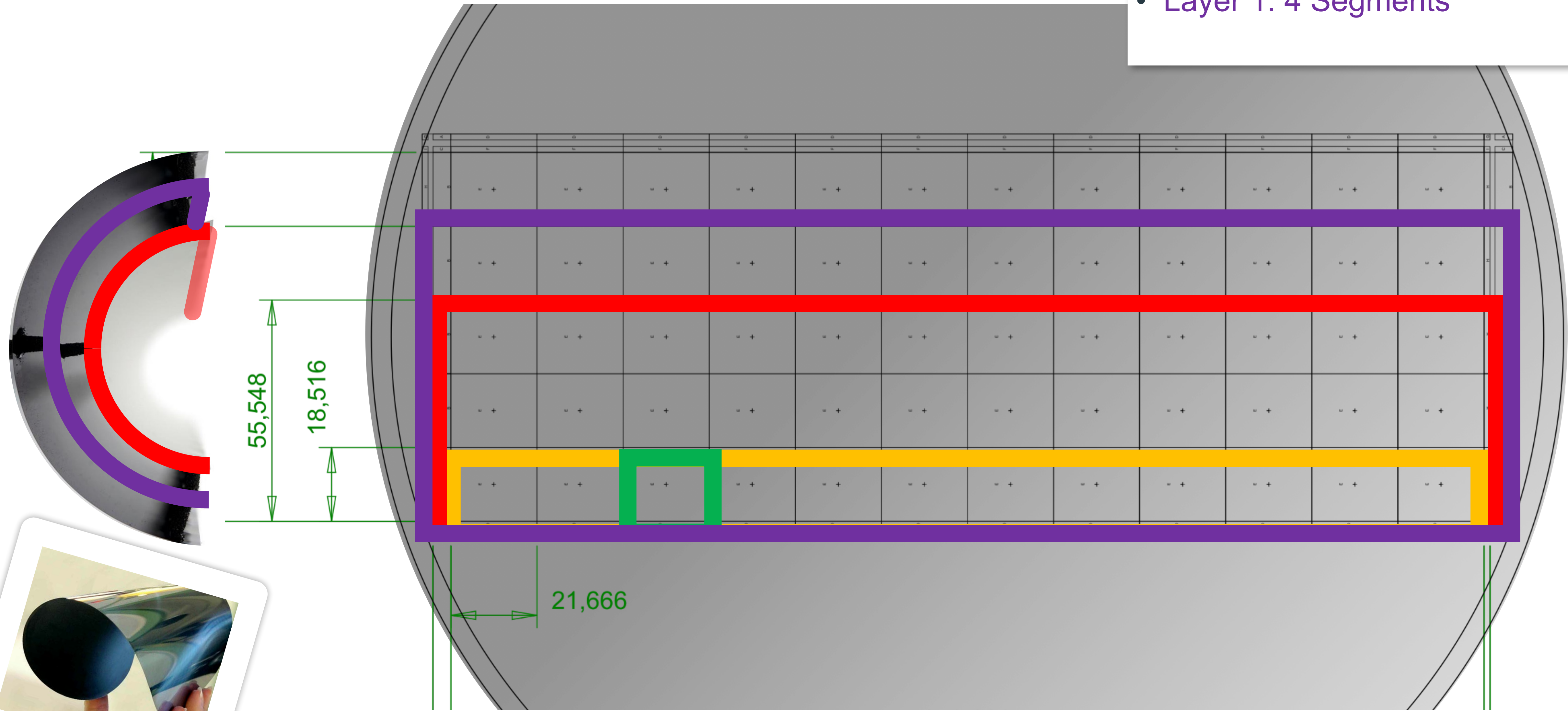
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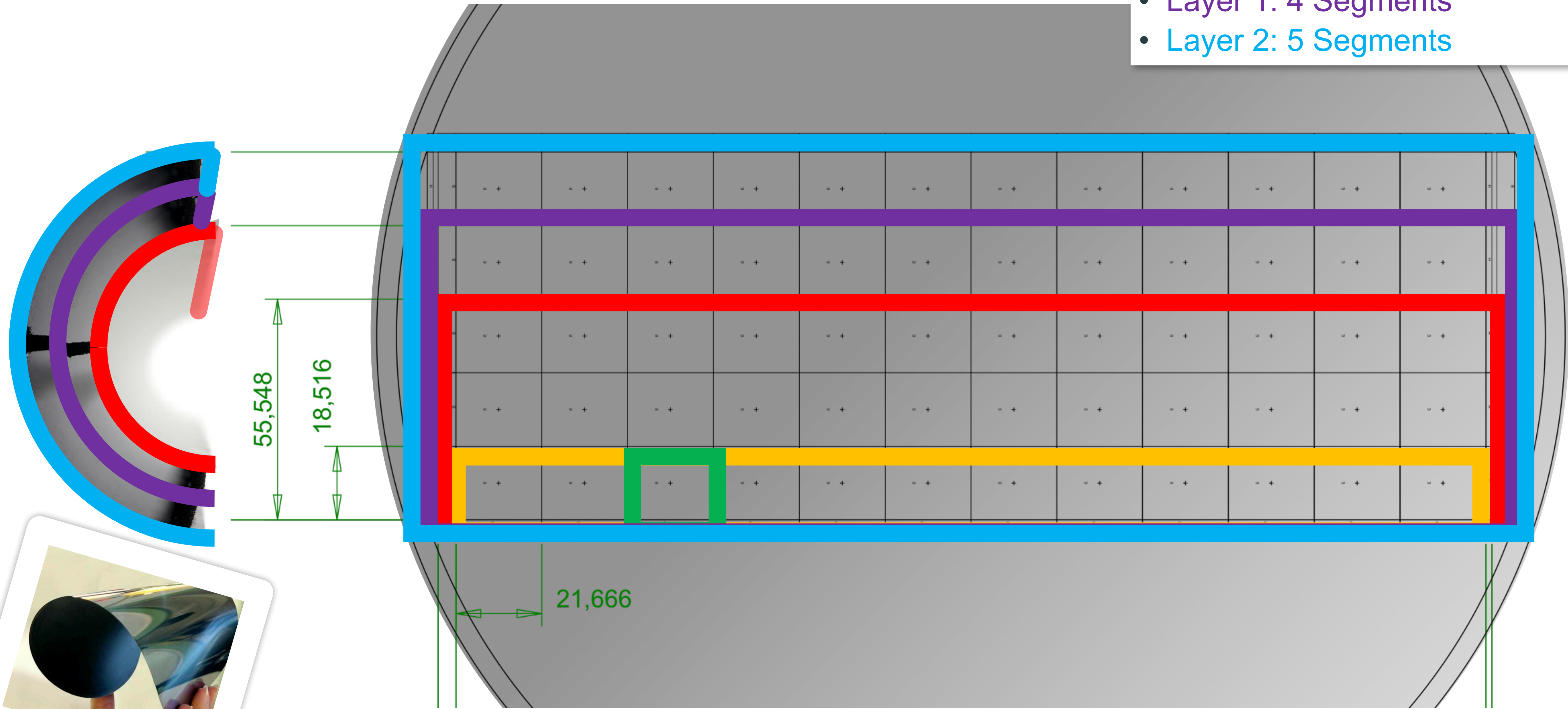
ITS3 Half-Layers

- Segment 12 RSUs + endcaps
- Repeated Sensor Unit
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- Layer 1: 4 Segments

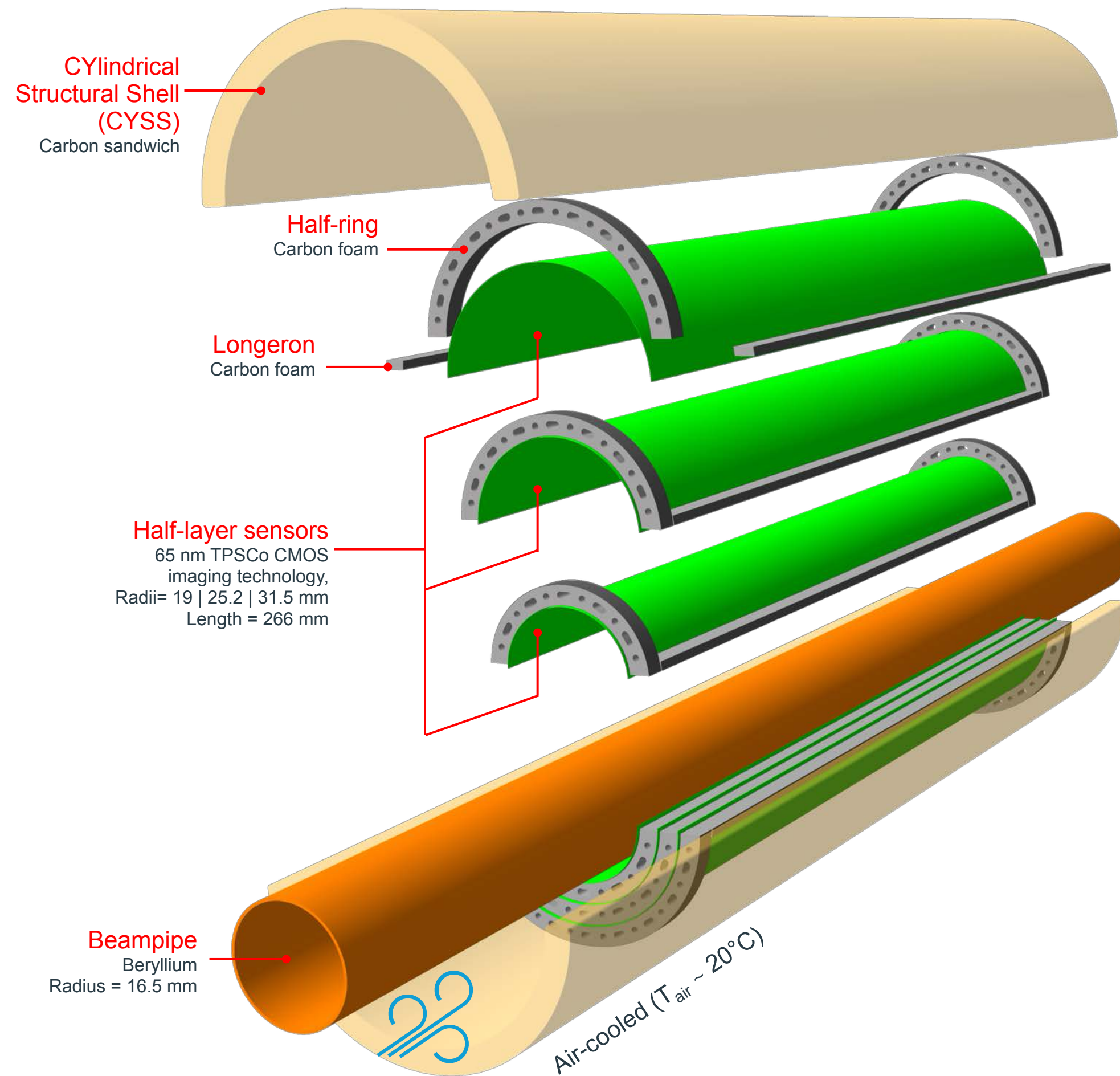


ITS3 Half-Layers

- Segment 12 RSUs + endcaps
- Repeated Sensor Unit
- Layer 0: 3 Segments
- Layer 1: 4 Segments
- Layer 2: 5 Segments



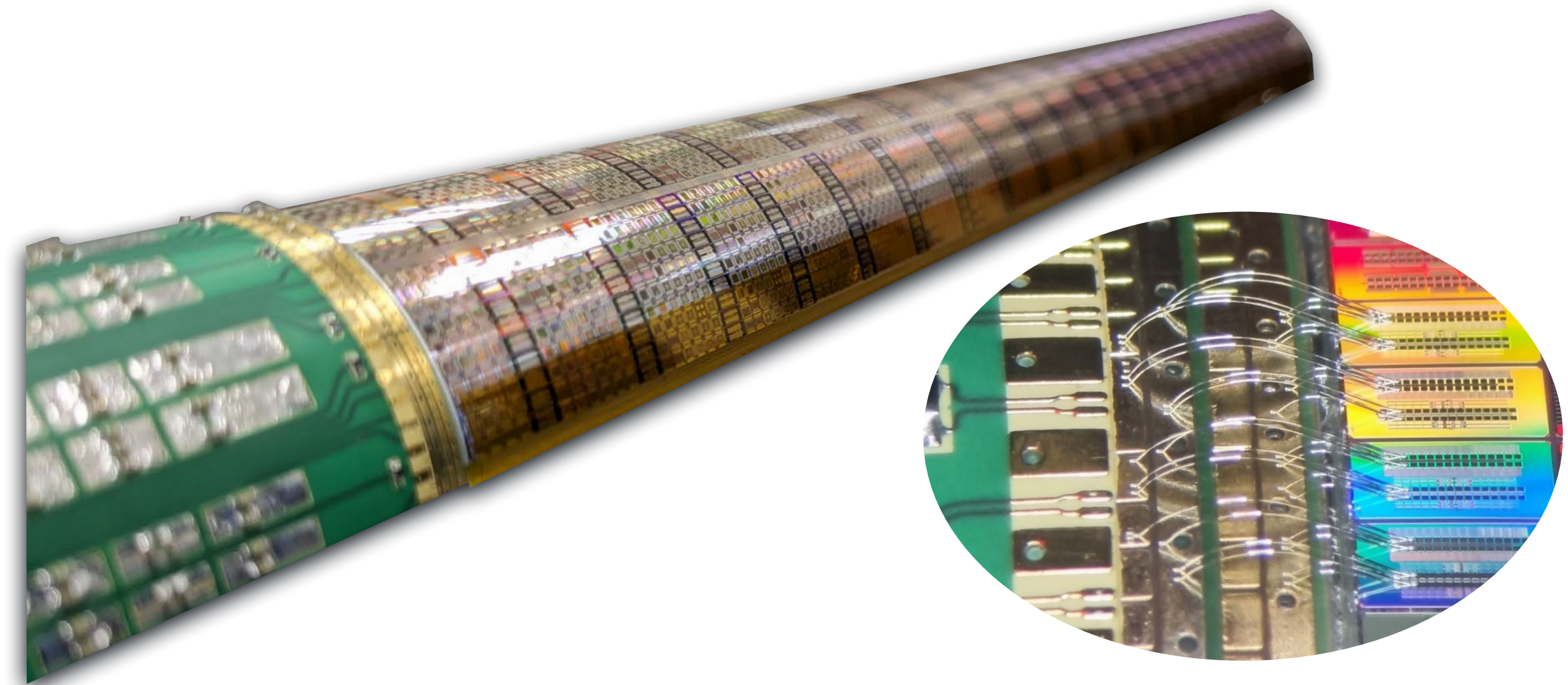
Mechanics and assembly



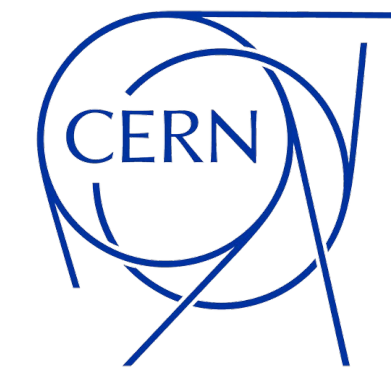
Simplified drawing schematic of the ALICE ITS3



Model for thermal and thermoelastic testing



Wire-bonding tests for integration of bent pixel sensor with FPC

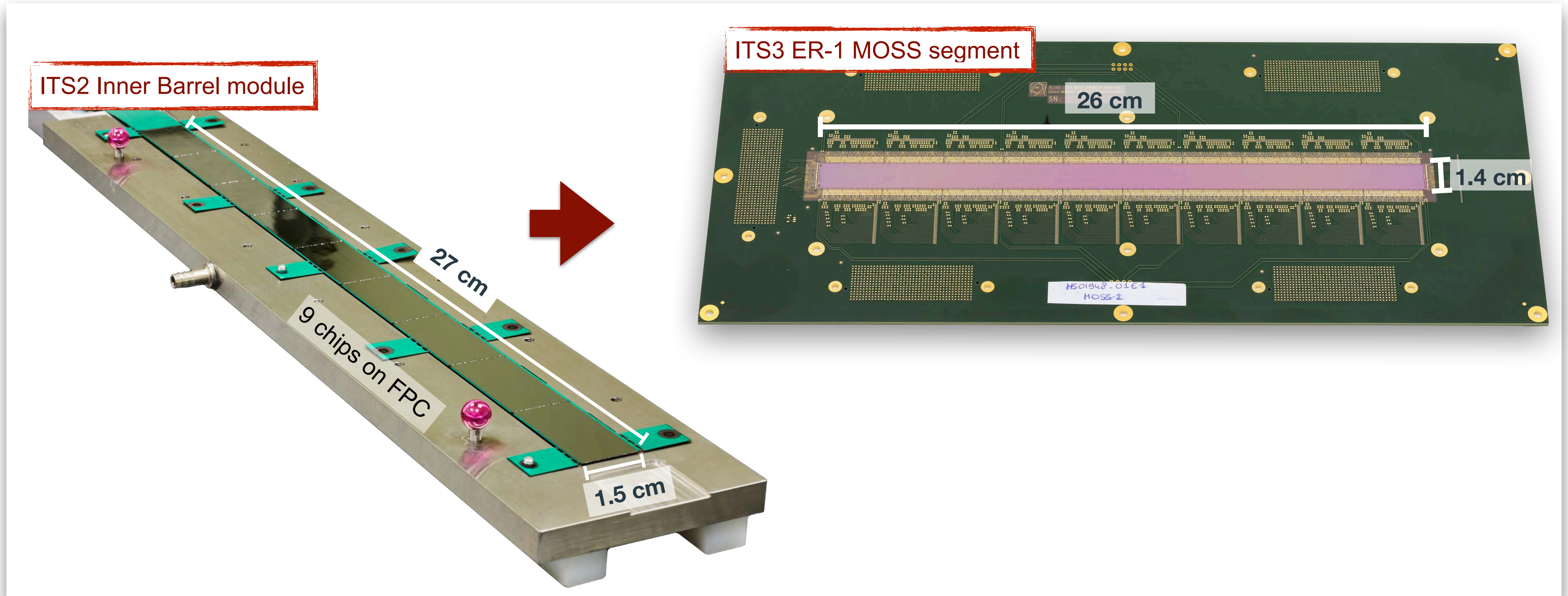


MOSAIX — Final full size, full functionality stitched CMOS pixel sensor

- Modular design:
 - Sensor divided into 5 $r\phi$ -segments for layer assembly
 - 144 tiles corresponding to 0.7% modularity to deactivate broken portions of the sensor
- Fractional sensitive area: 93%
- Interfacing:
 - Powering LEC and REC sides
 - Control and readout from the LEC only
- Pixel:
 - Pitch: $O(20\ \mu\text{m})$ / spatial resolution $\approx 5\ \mu\text{m}$
 - Detection efficiency: $> 99\%$
 - Fake-hit rate: 10^{-6} / pixel / event
- Hit load and readout:
 - 5.75 MHz / cm^2 particle hit rate (Pb-Pb collisions, safety factor 2)
 - Minimum integration window: $2\ \mu\text{s}$
 - Off-chip data transmission: 30.72 Gb/s
 - Multiple 5.12 / 10.24 Gb/s links
- Radiation load*:
 - Non-Ionising Energy Loss (NIEL): $\sim 4 \times 10^{12}\ 1\ \text{MeV}\ n_{\text{eq}}\ \text{cm}^{-2}$
 - Total Ionising Dose (TID): $\sim 4\ \text{kGy} / 400\ \text{krad}$
 - * recent estimates, based on radiation dose absorbed by ITS2*
- Power dissipation (active area): $< 40\ \text{mW} / \text{cm}^2$
- Delivery from foundry expected in February

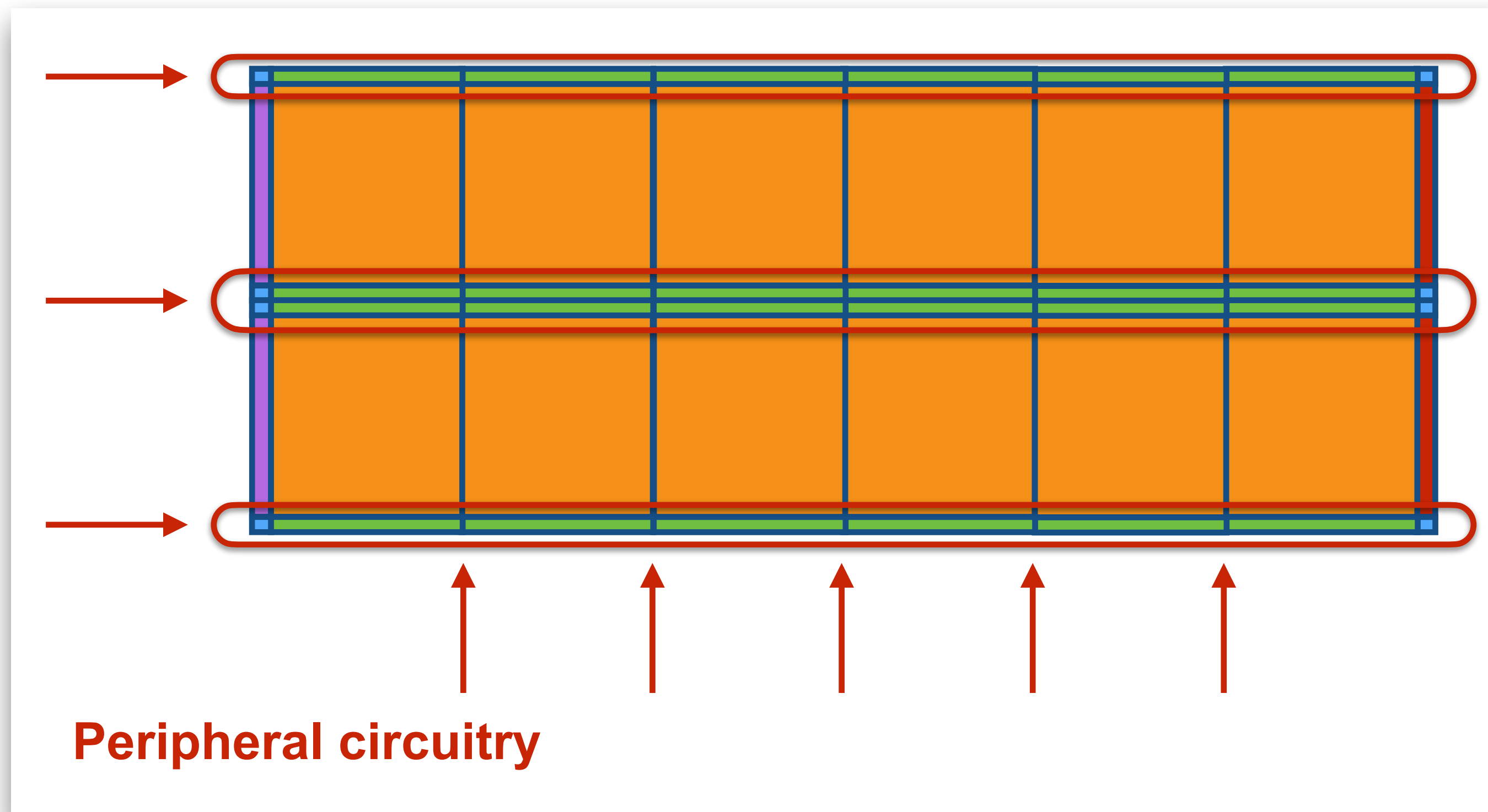
Stitched Wafer-Scale MAPS — MOSAIX — challenges

- Interdependencies and integration: ‘module on a chip’



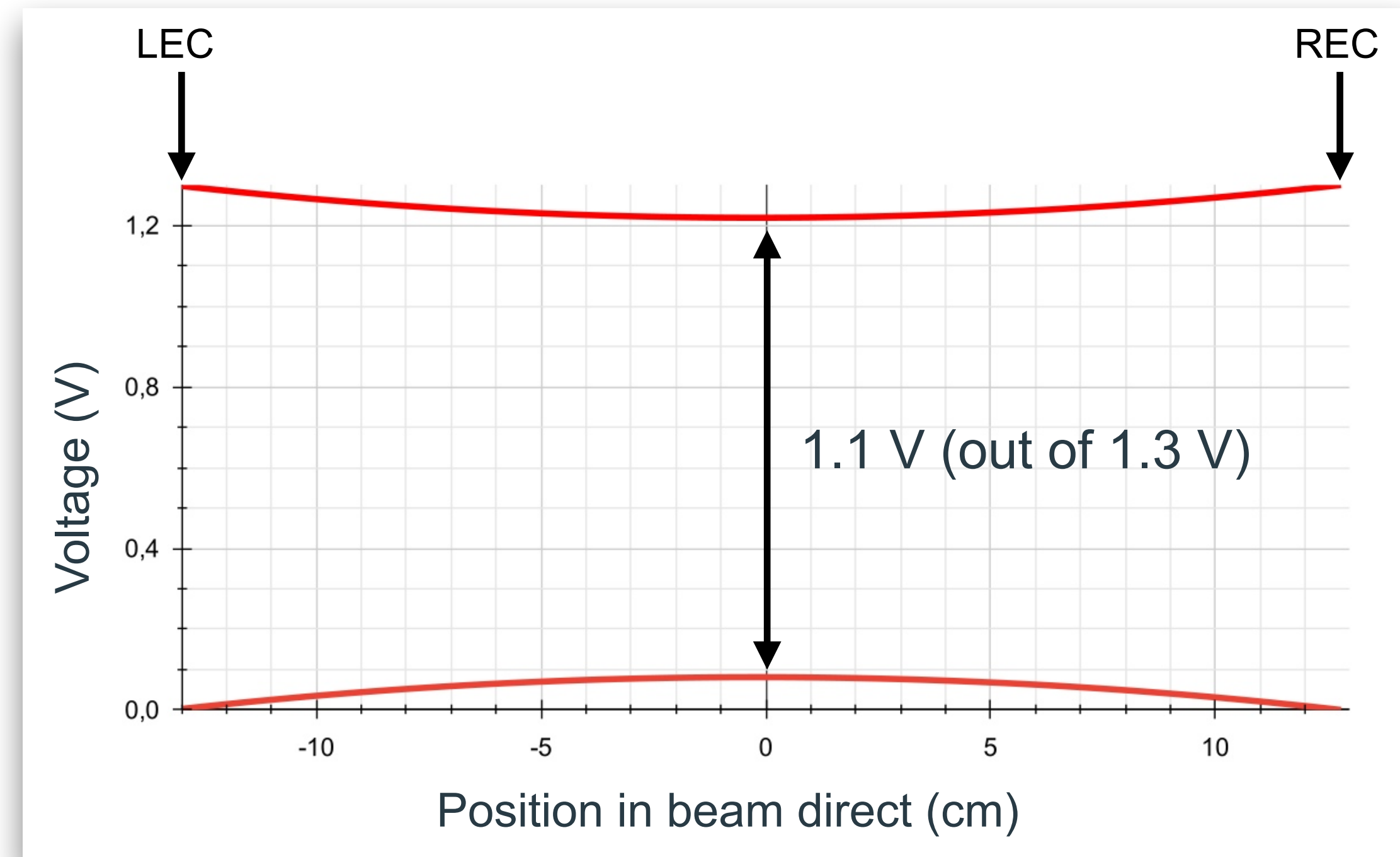
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 - Readout and biasing need peripheral circuits



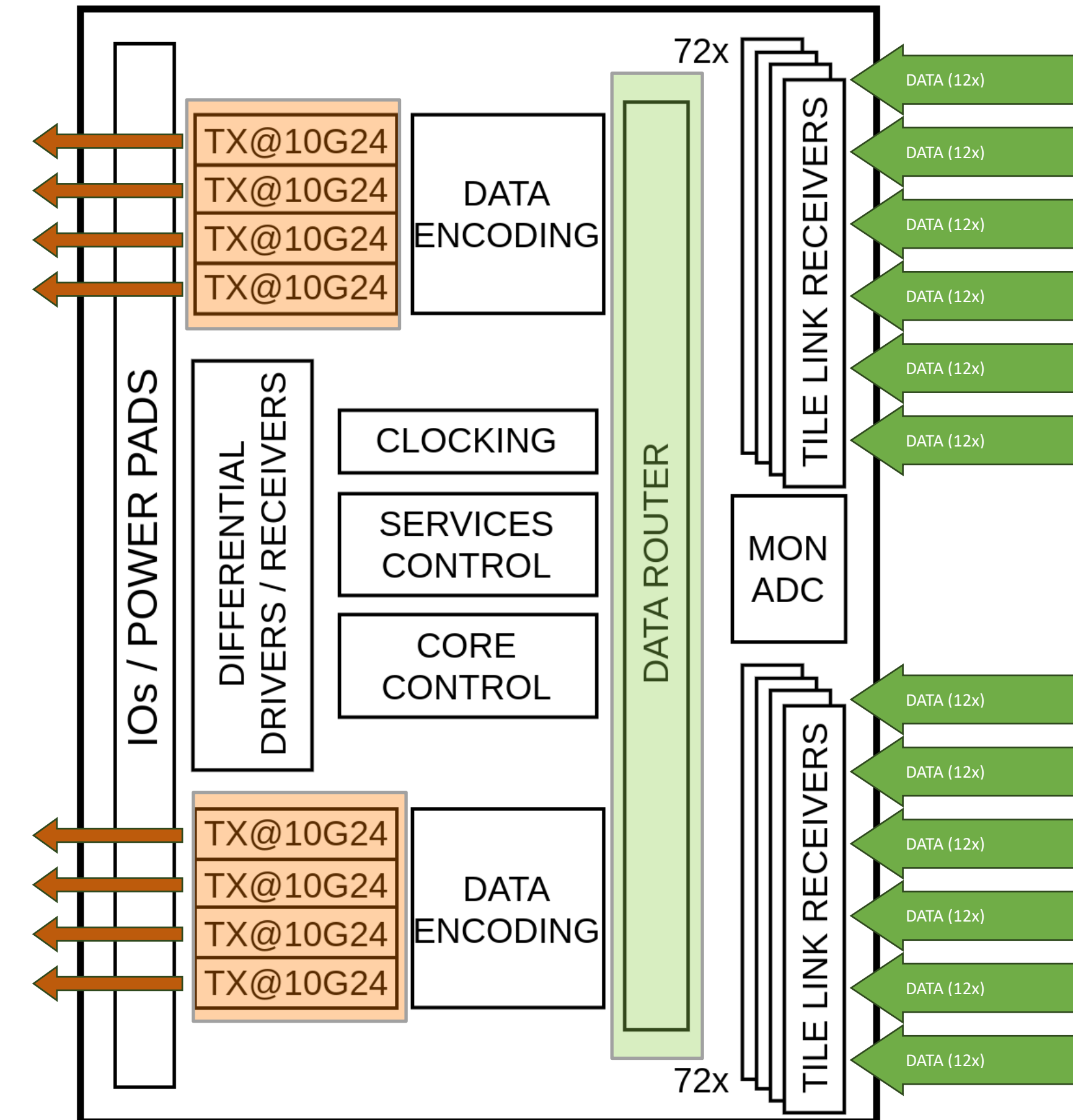
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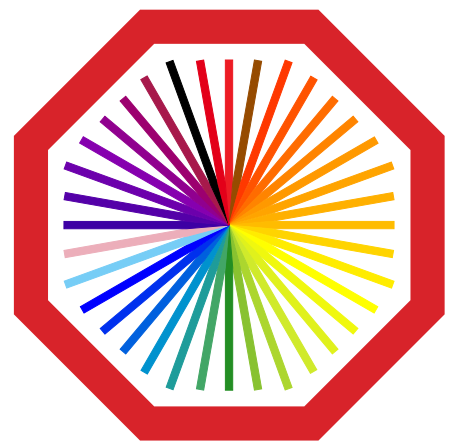
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 - Complex segmentation in many independent domains (tiles)
 - Switches and cross-domain signaling and protections



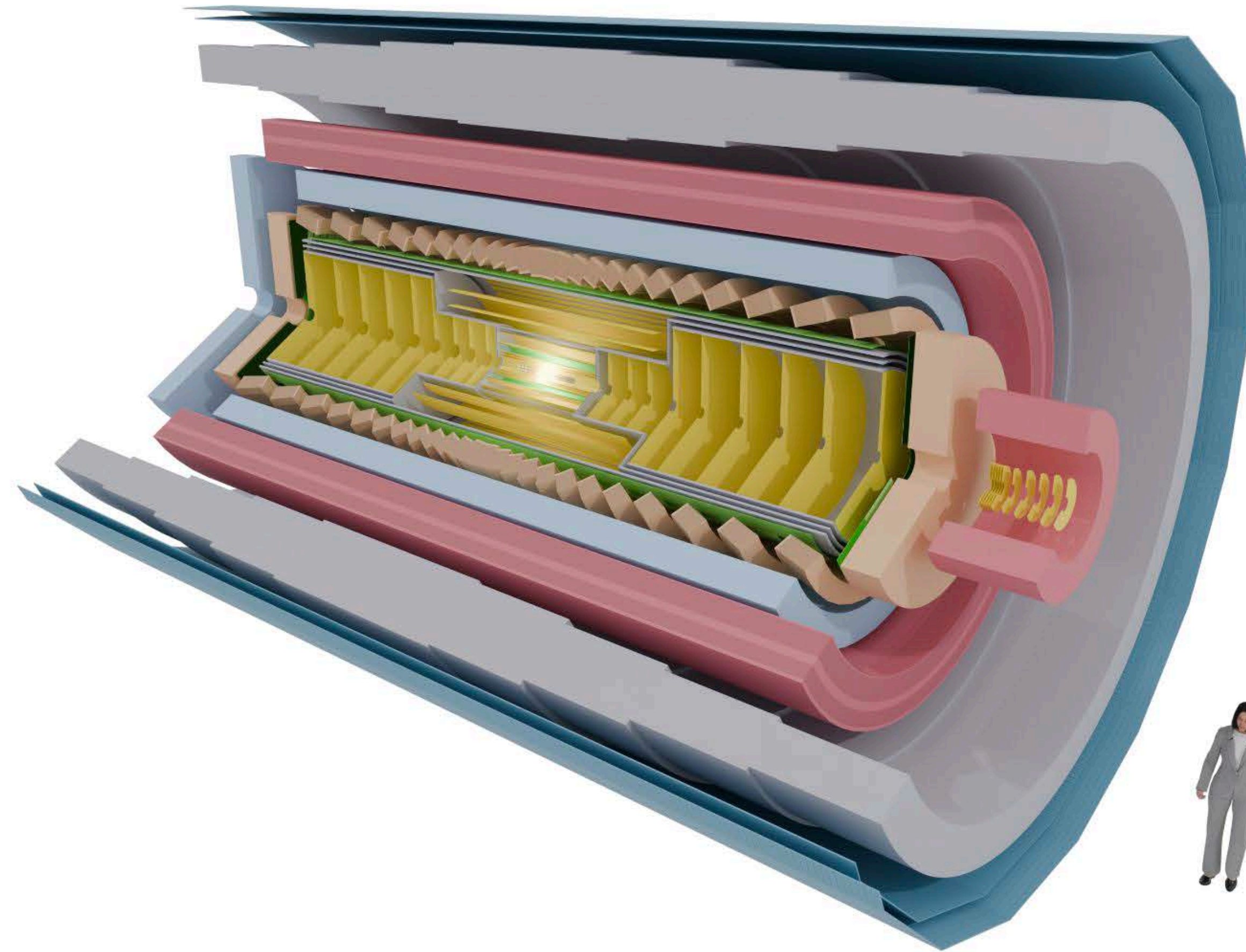
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- Power distribution
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 - Complex segmentation in many independent domains (tiles)
 - Switches and cross-domain signaling and protections
- Data transmission
 - Integrate **144 on-chip transmission lines** of 25 cm working at 160 Mb/s
 - High speed (10.24 Gb/s) **wireline drivers** for off-chip transmission

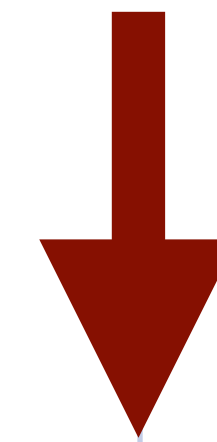




ALICE



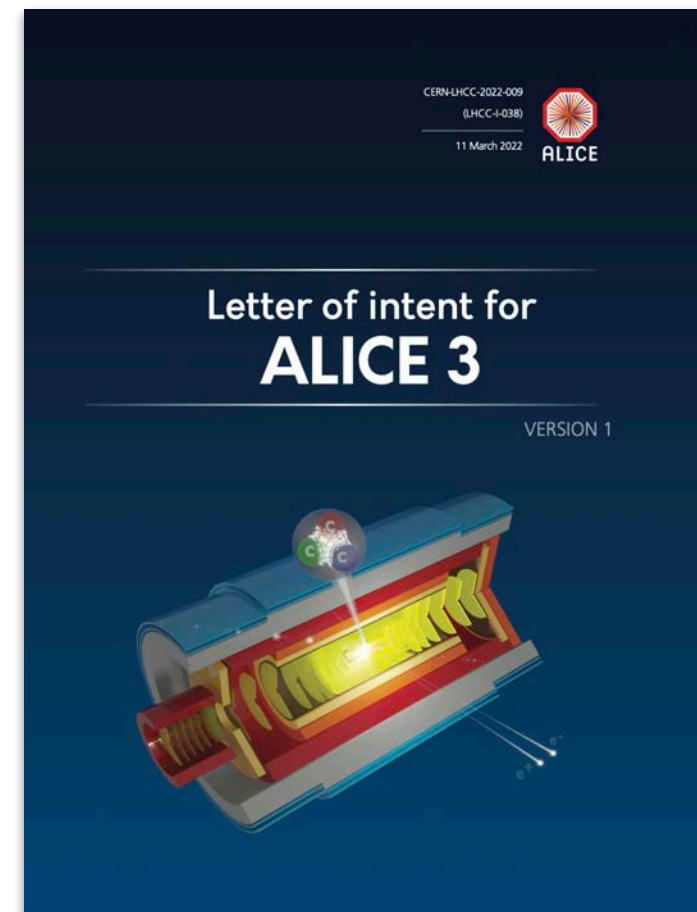
ALICE 3 Vertex Detector and Trackers



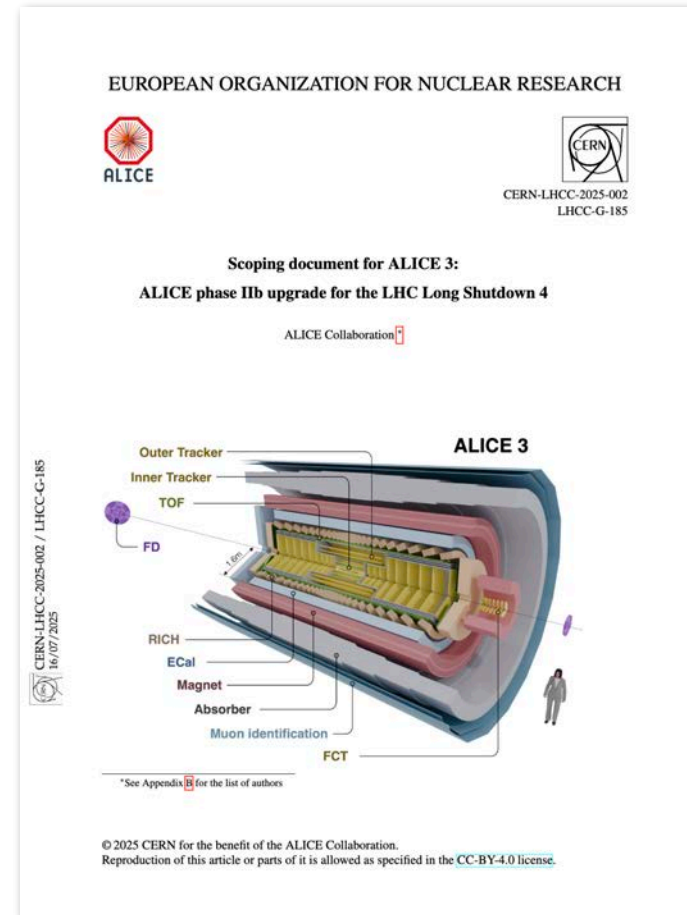
ALICE 3 — Concept

Novel and innovative detector concept

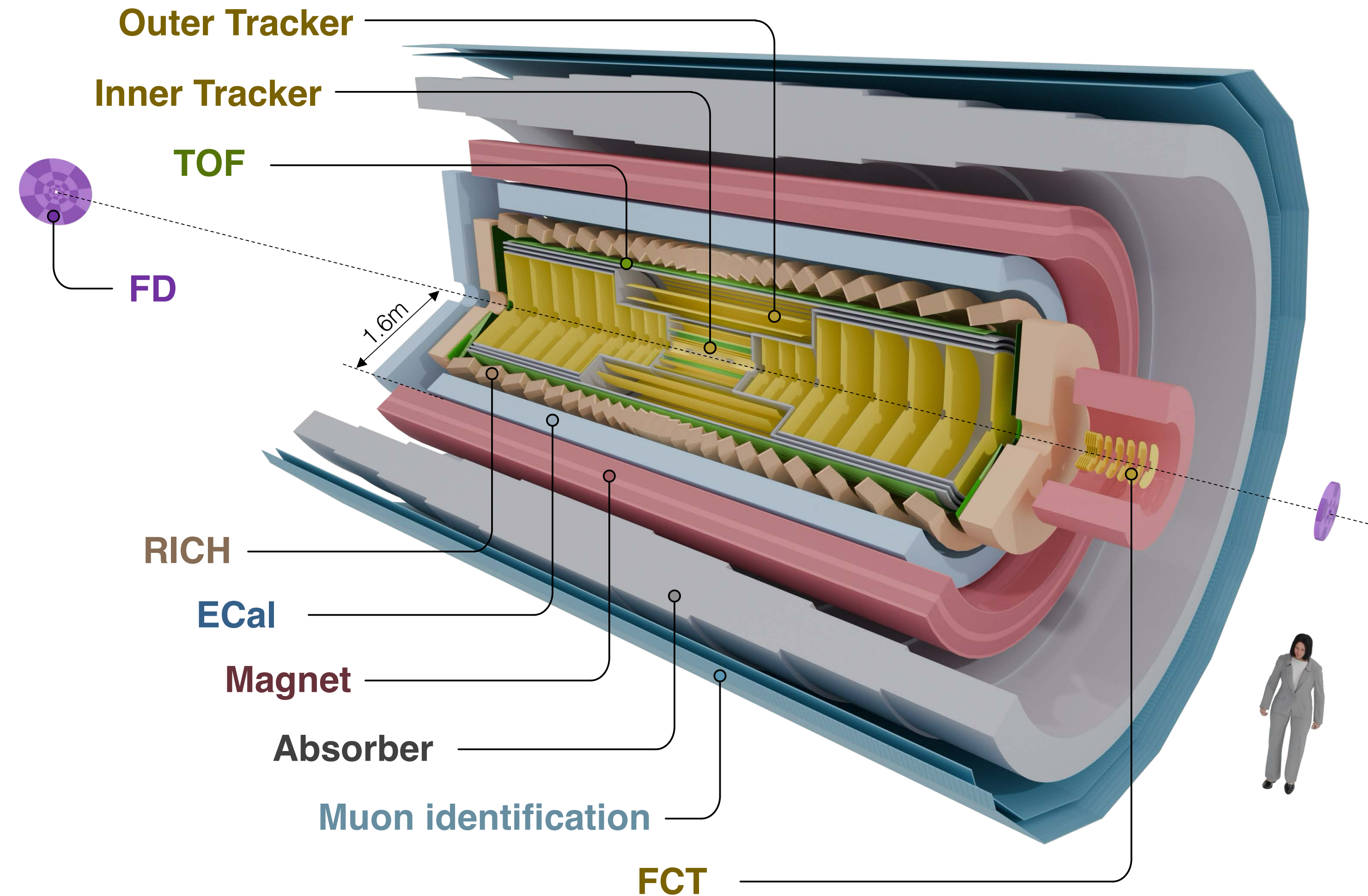
- Compact, low-mass **all-silicon** tracker
- Retractable **vertex** detector
- Excellent **vertex reconstruction** and **PID** capabilities
- **Large acceptance**
- Super conduction magnet system
- Continuous read-out and online processing



CERN-LHCC-2022-009

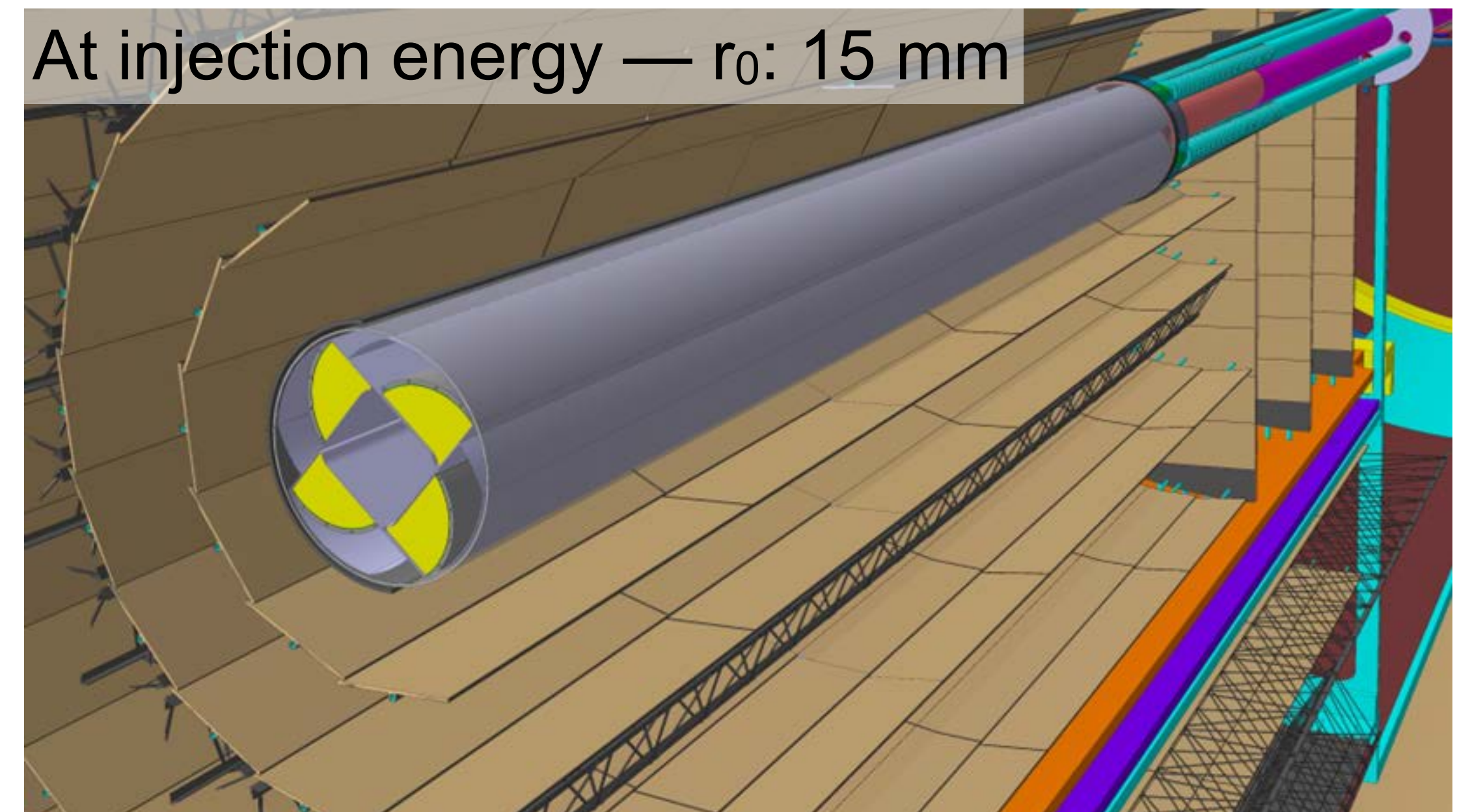
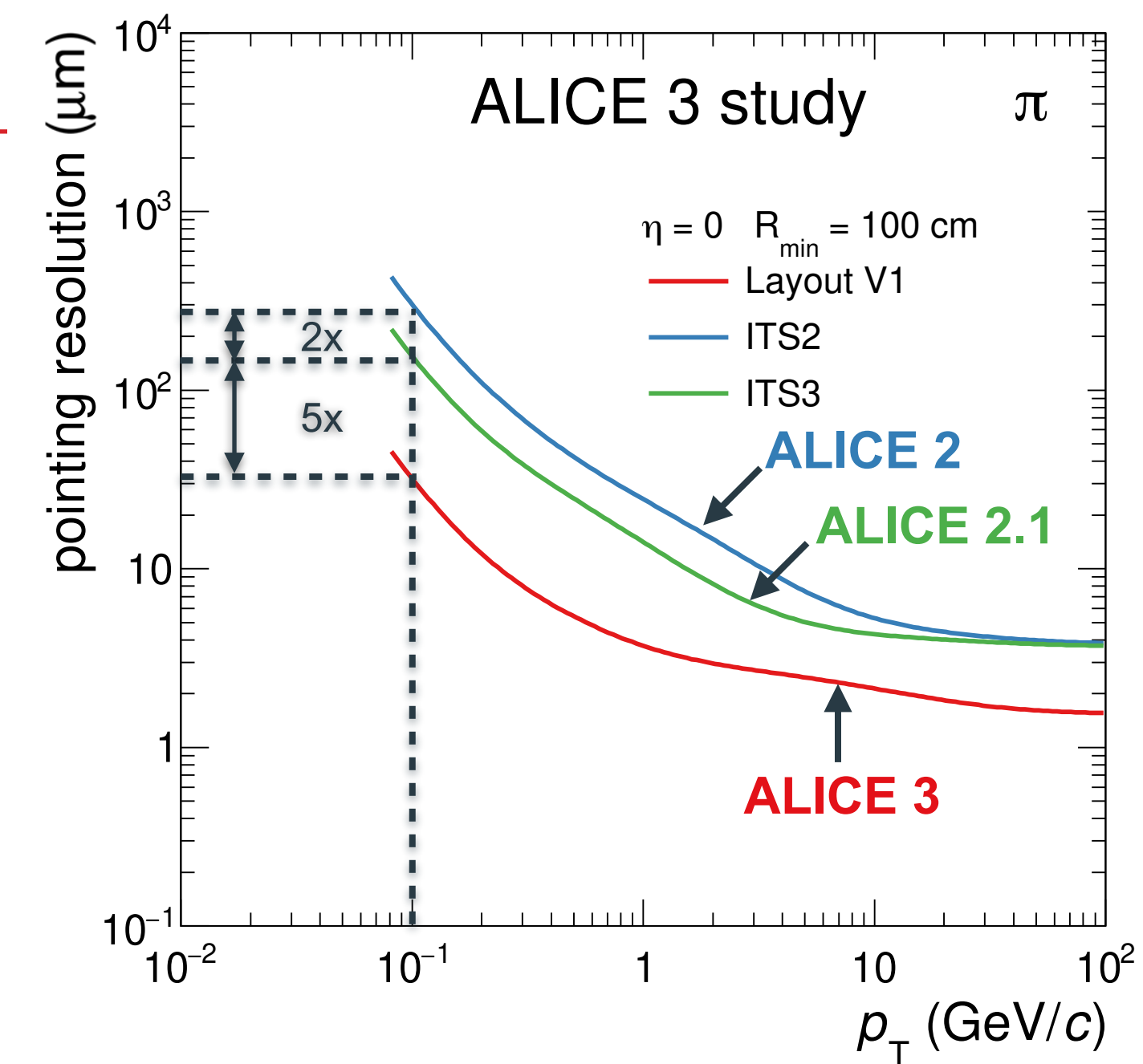


CERN-LHCC-2025-002



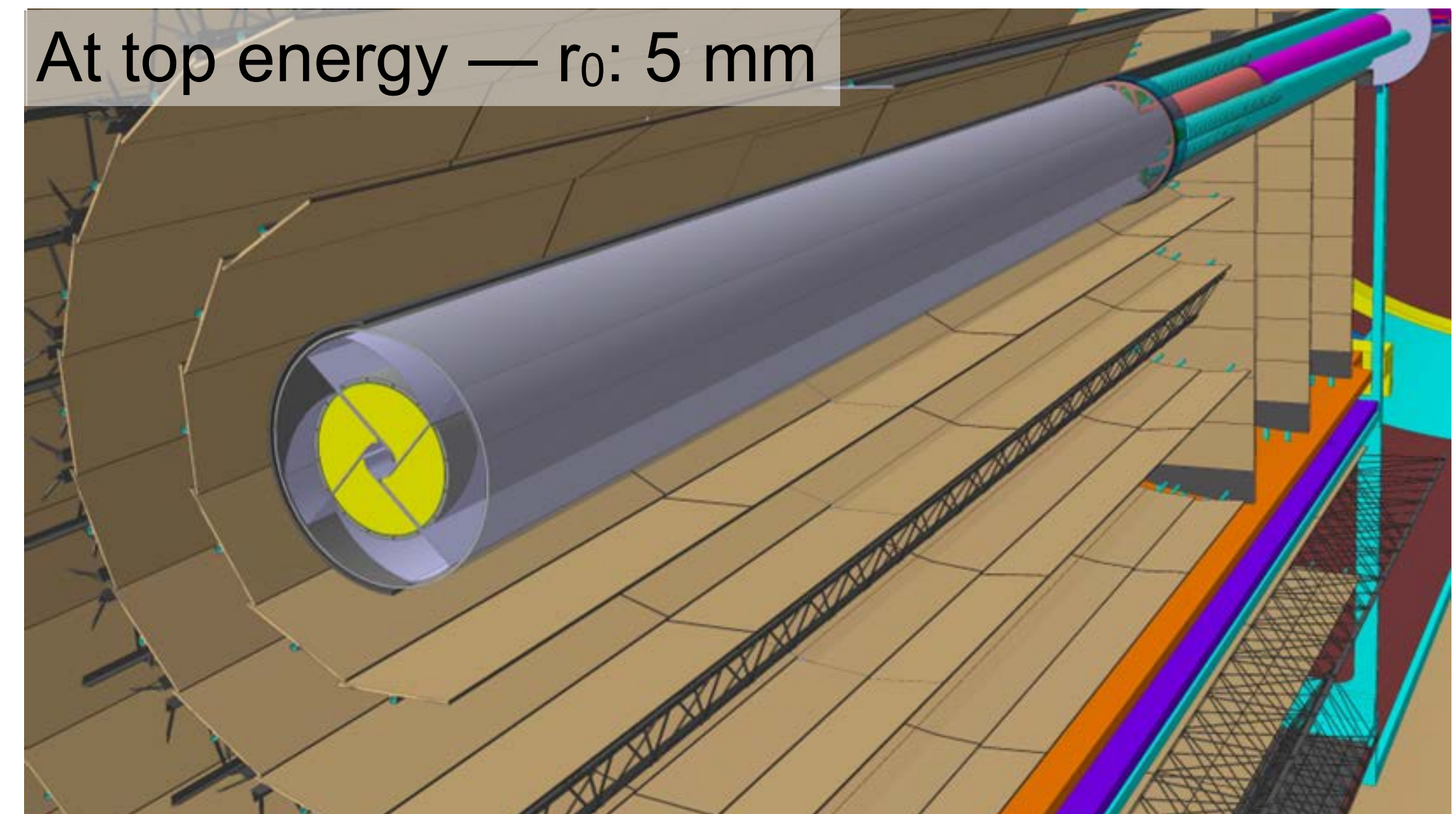
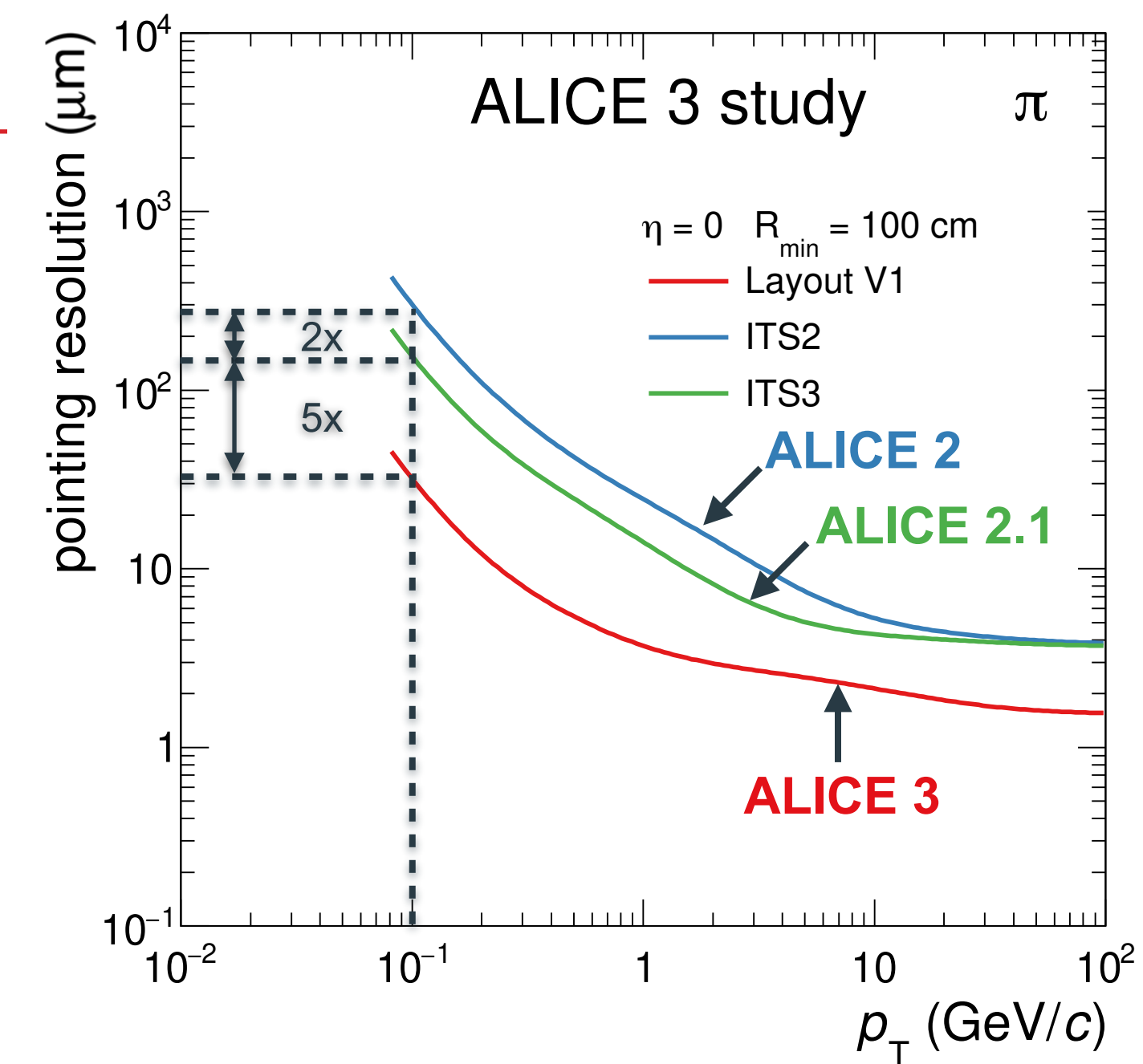
ALICE 3 — Vertex Detector (VD)

- **Pointing resolution** $\propto r_0 \cdot \sqrt{x/X_0}$ (multiple scattering regime)
 - Radius and material of first layer crucial
 - Minimal radius given by required aperture:
 $R \approx 5$ mm at top energy,
 $R \approx 15$ mm at injection energy
→ retractable vertex detector
- **Key detector characteristics**
 - 3 detection layers (barrel + disks)
 - Retractable: **$r_0 = 5$ mm**
 - Material budget: **0.1% X_0 / layer**
 - Unprecedented spatial resolution: **$2.5 \mu\text{m}$**
- **Main R&D challenges**
 - Light-weight in-vacuum mechanics and cooling
 - Radiation hardness ($>10^{15}$ 1 MeV $n_{\text{eq}}/\text{cm}^2$ + 300 Mrad)
 - Pixel pitch of $10 \mu\text{m}$
 - Particle load of ~ 100 MHz / cm^2



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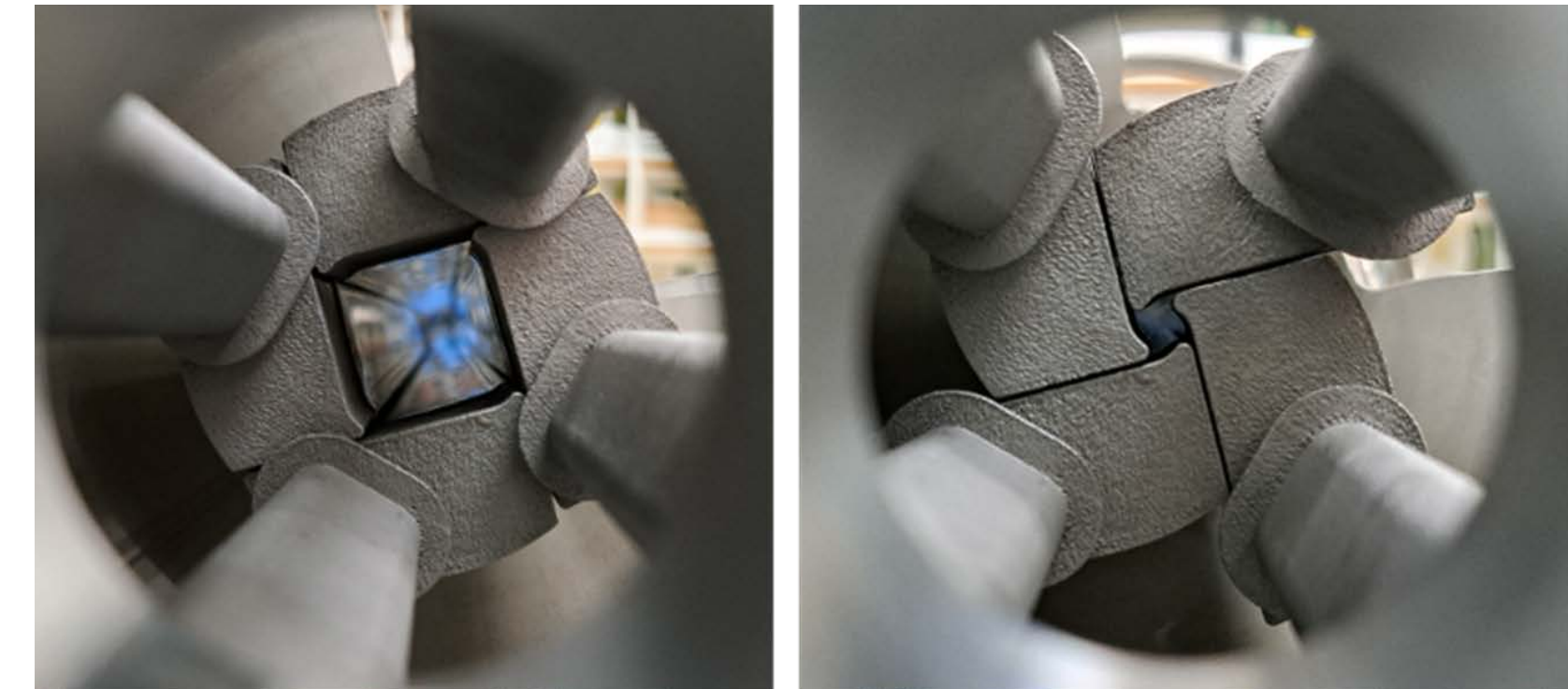
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- **Main R&D challenges**
 - Light-weight in-vacuum mechanics and cooling
 - Radiation hardness ($>10^{15}$ 1 MeV $n_{\text{eq}}/\text{cm}^2$ + 300 Mrad)
 - Pixel pitch of 10 μm
 - Particle load of ~ 100 MHz / cm^2



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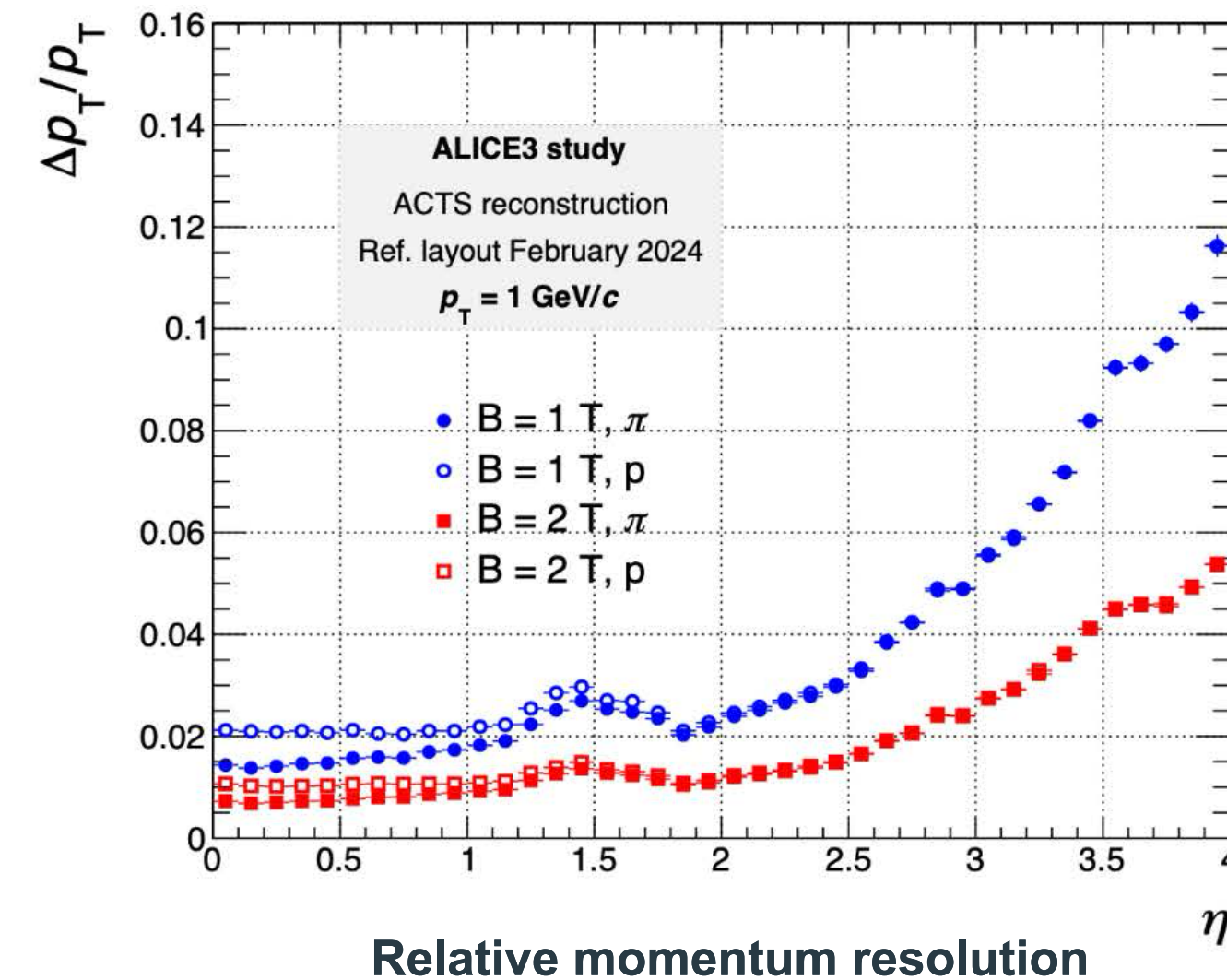
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Latest mechanical prototype

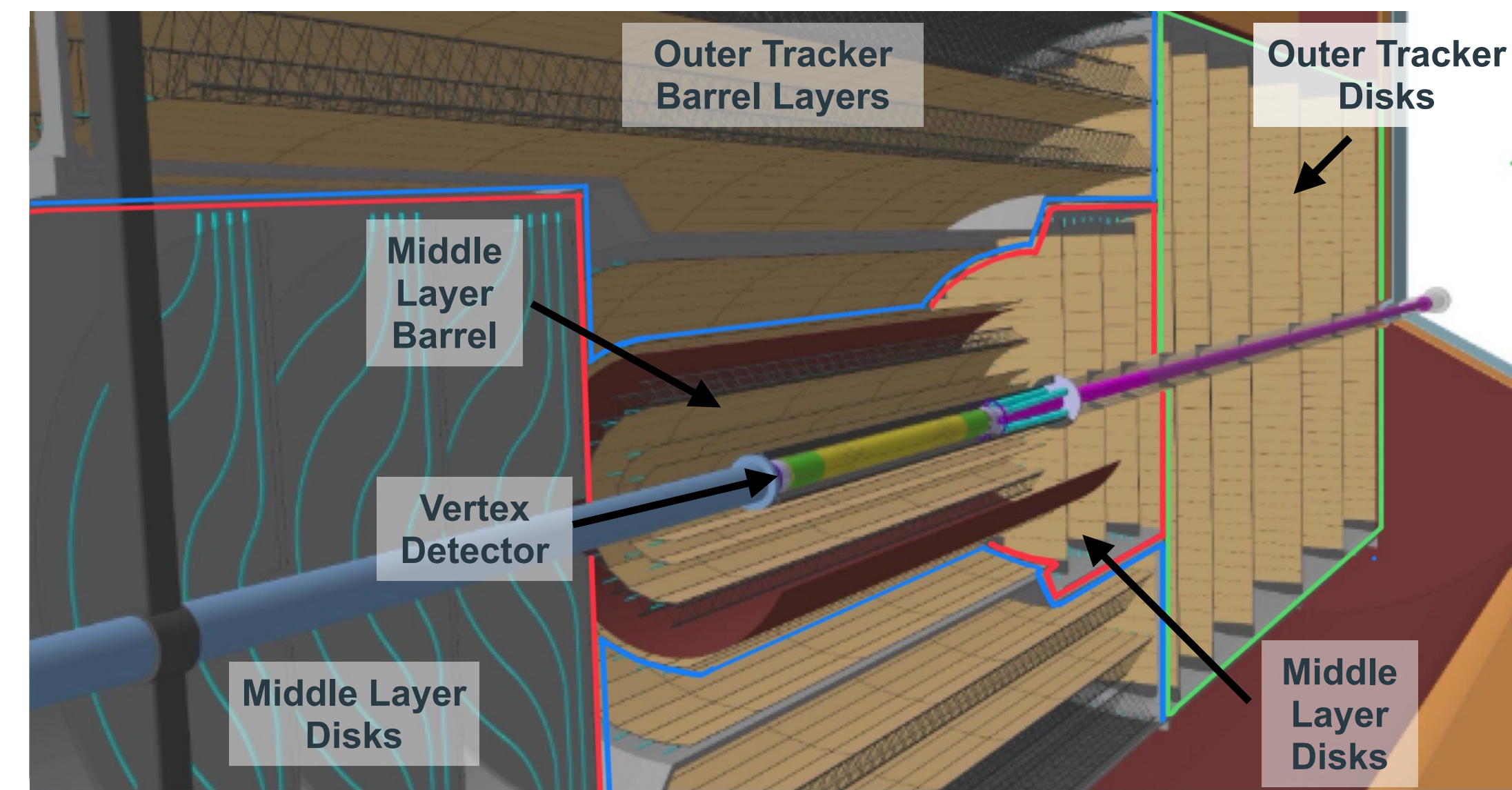


ALICE 3 — Tracking detectors (Middle Layers and Outer Tracker)

- **Relative p_T resolution** $\propto \frac{\sqrt{x/X_0}}{B \cdot L}$
(limited by multiple scattering)
 - Integrated magnetic field crucial
 - Overall material budget critical
- **Key detector characteristics**
 - Barrel layers ($7 \text{ cm} < R < 80 \text{ cm}$) + forward disks
 - Total surface: $\sim 60 \text{ m}^2$
 - Material budget: $1\% X_0 / \text{layer}$
 - Spatial resolution: $10 \text{ } \mu\text{m} / \sim 50 \text{ } \mu\text{m}$ pixel pitch
 - Low power consumption: 20 mW/cm^2
 - $O(100 \text{ ns})$ time resolution
- **Main R&D challenges**
 - Module design for high yield industrial mass production
 - Low power consumption while maintaining timing performance
 - Power distribution (serial powering)

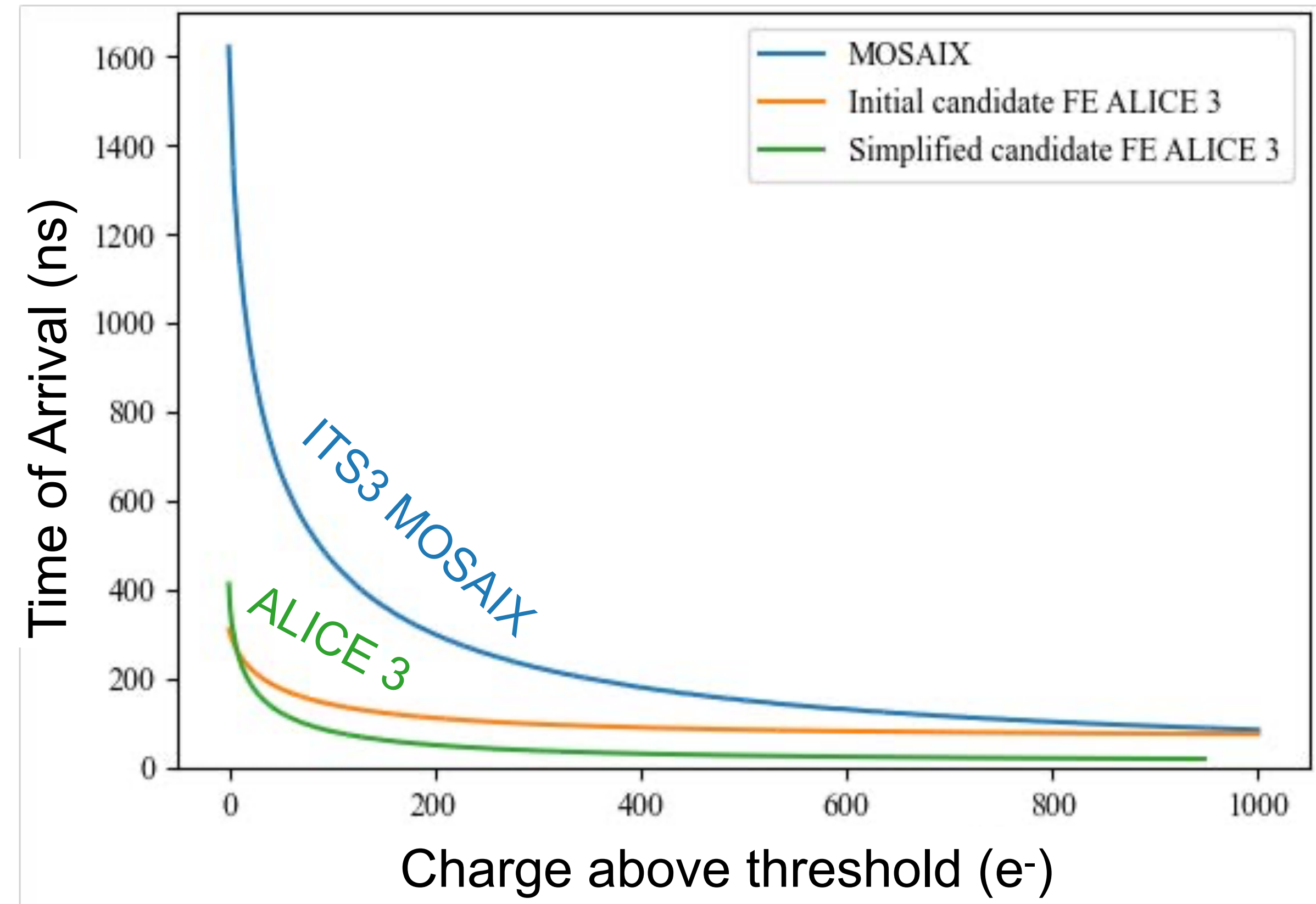


Automated module
assembly tests

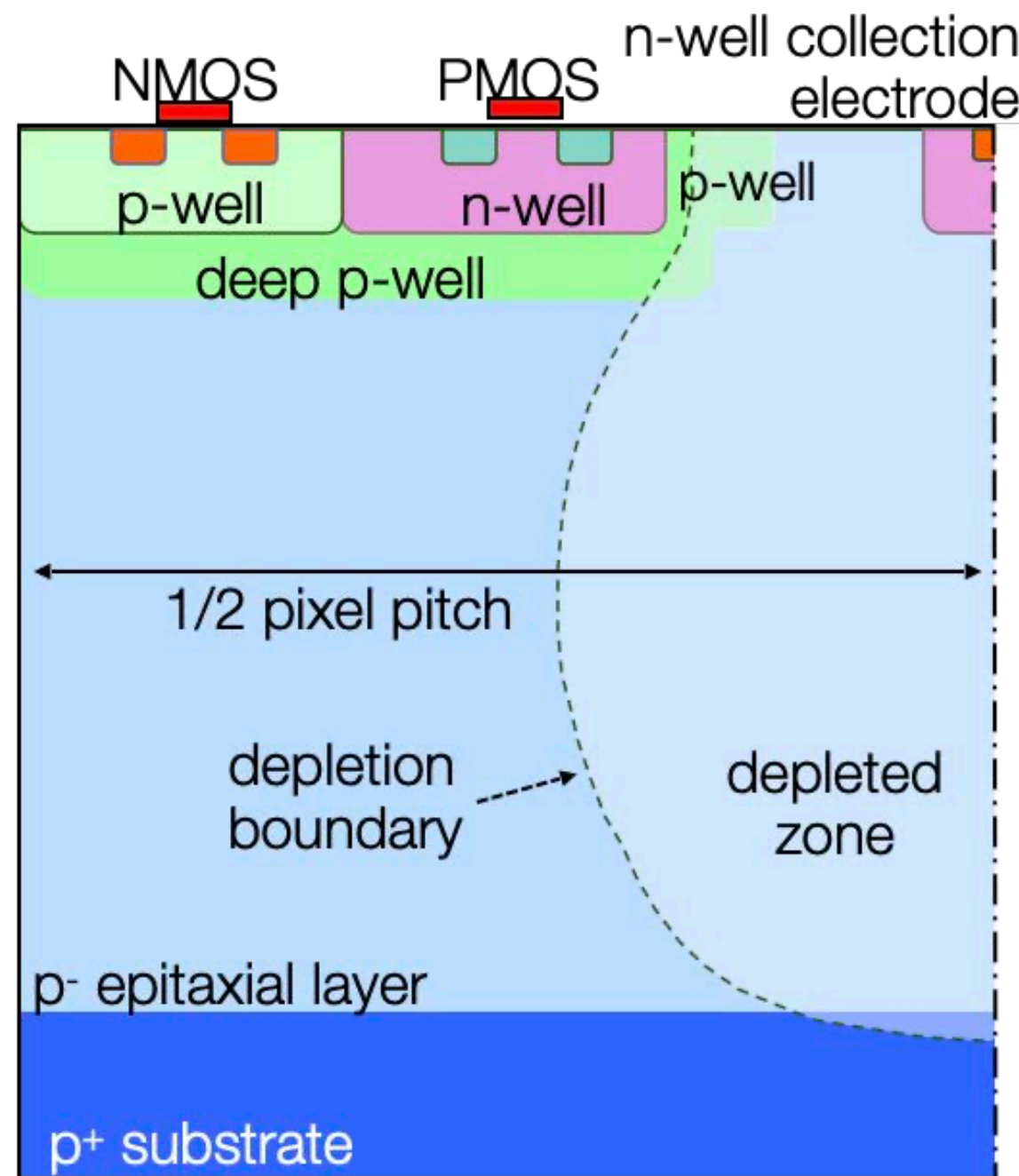


Towards an ALICE 3 pixel sensor — new compact analog front-end circuit

- Layout fitting an area of $5\ \mu\text{m} \times 10\ \mu\text{m}$ including collection electrode (significantly smaller than previous circuits)
⇒ rendering $10\ \mu\text{m}$ pixel pitch possible
- Perspective for lower thresholds ($\sim 75\ e^-$ instead of $\sim 150\ e^-$)
⇒ larger portion of the signal above threshold
- Improved current utilization, yielding:
 - Faster Time-of-Arrival (ToA)
 - Improved time resolution (ToA spread)
- Test chips to be submitted in the next submission



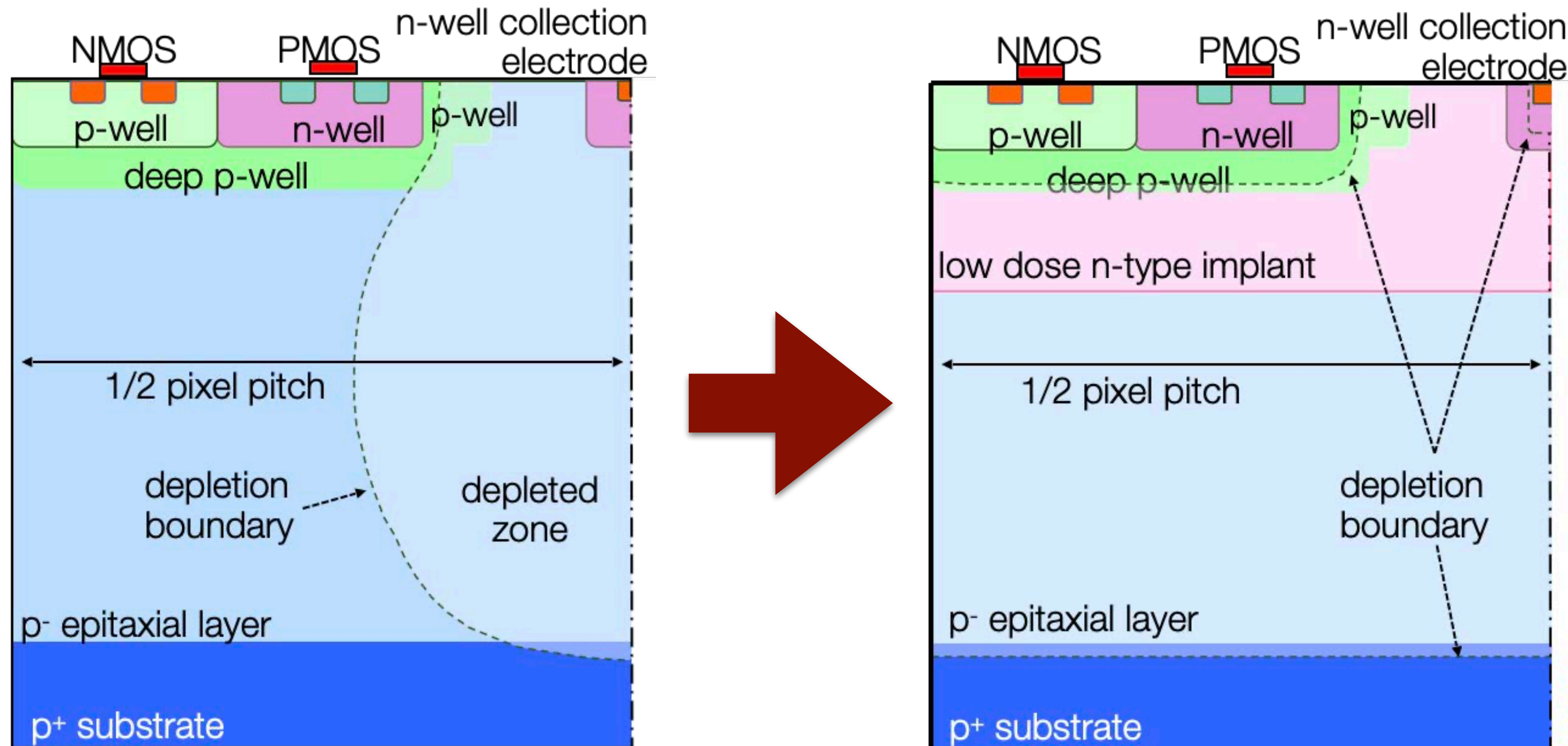
Towards a ALICE 3 pixel sensor — improving charge collection



Standard process

- Used in ALPIDE
- Charge collection by drift and diffusion
- Charge sharing between pixels
⇒ improved position resolution

Towards a ALICE 3 pixel sensor — improving charge collection



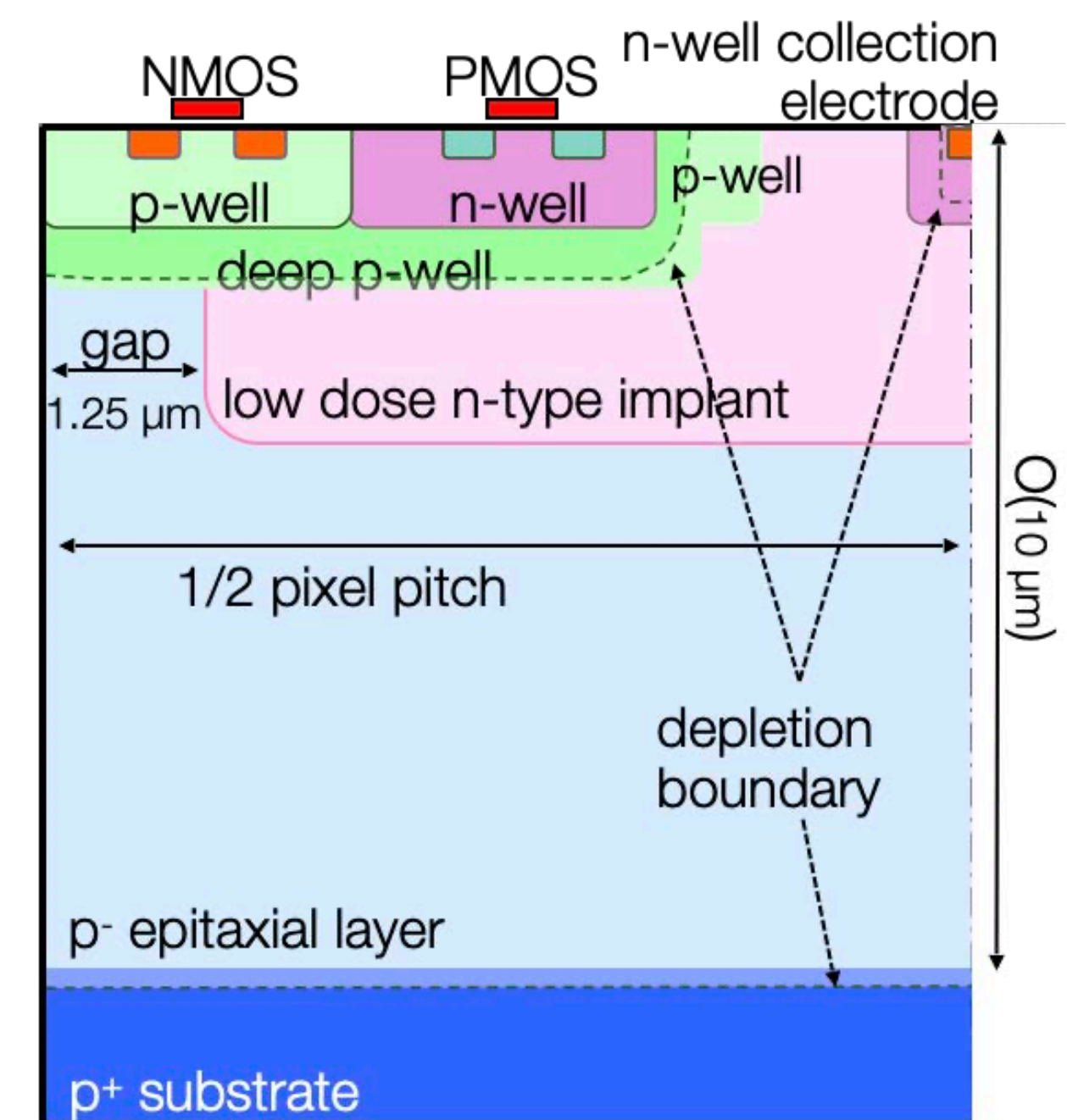
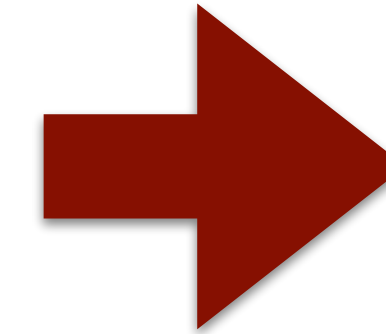
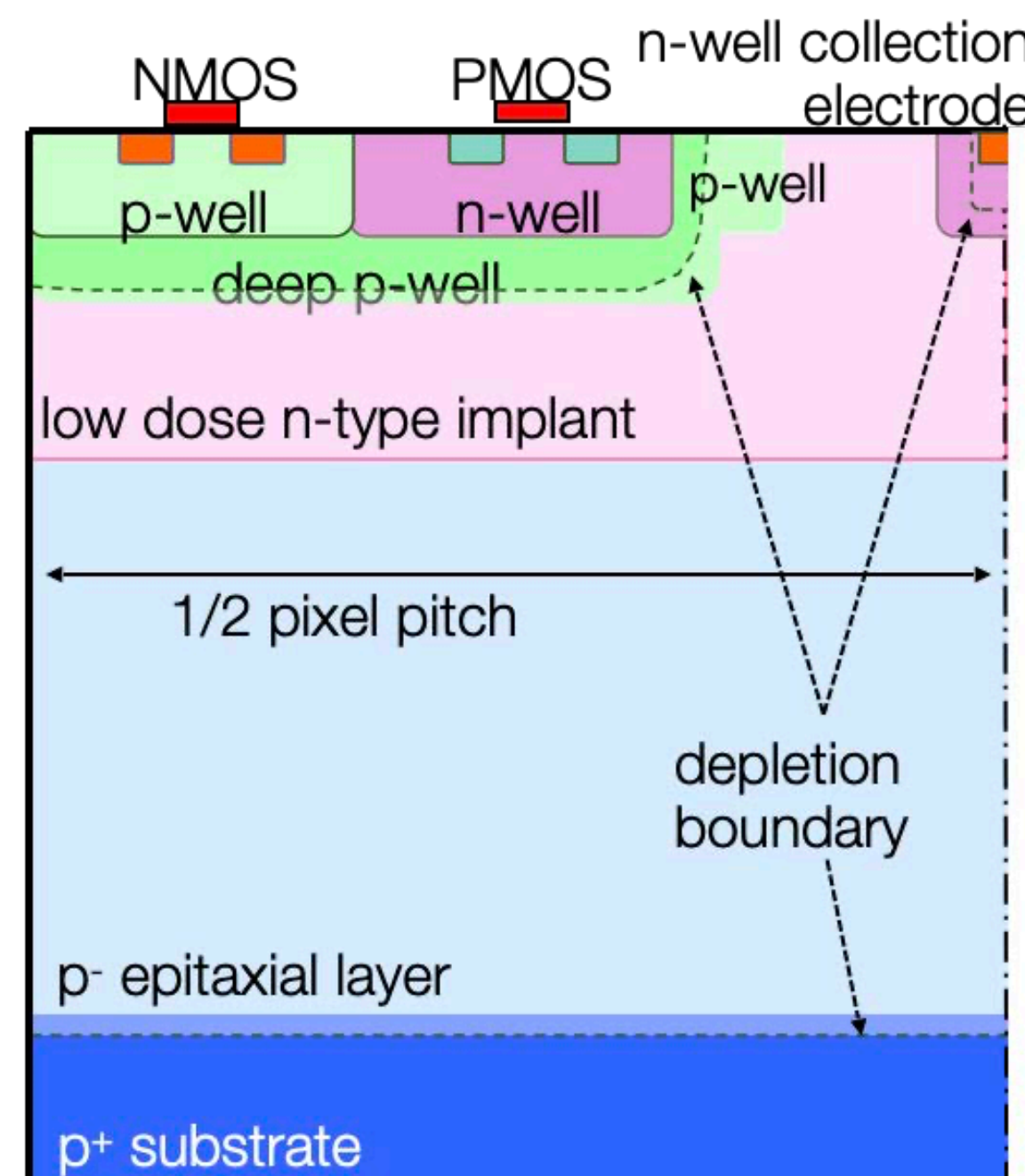
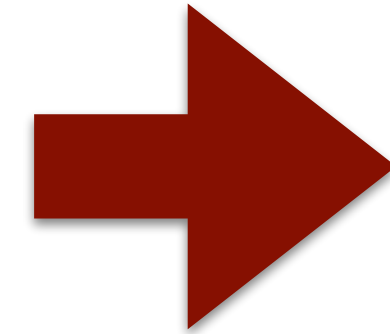
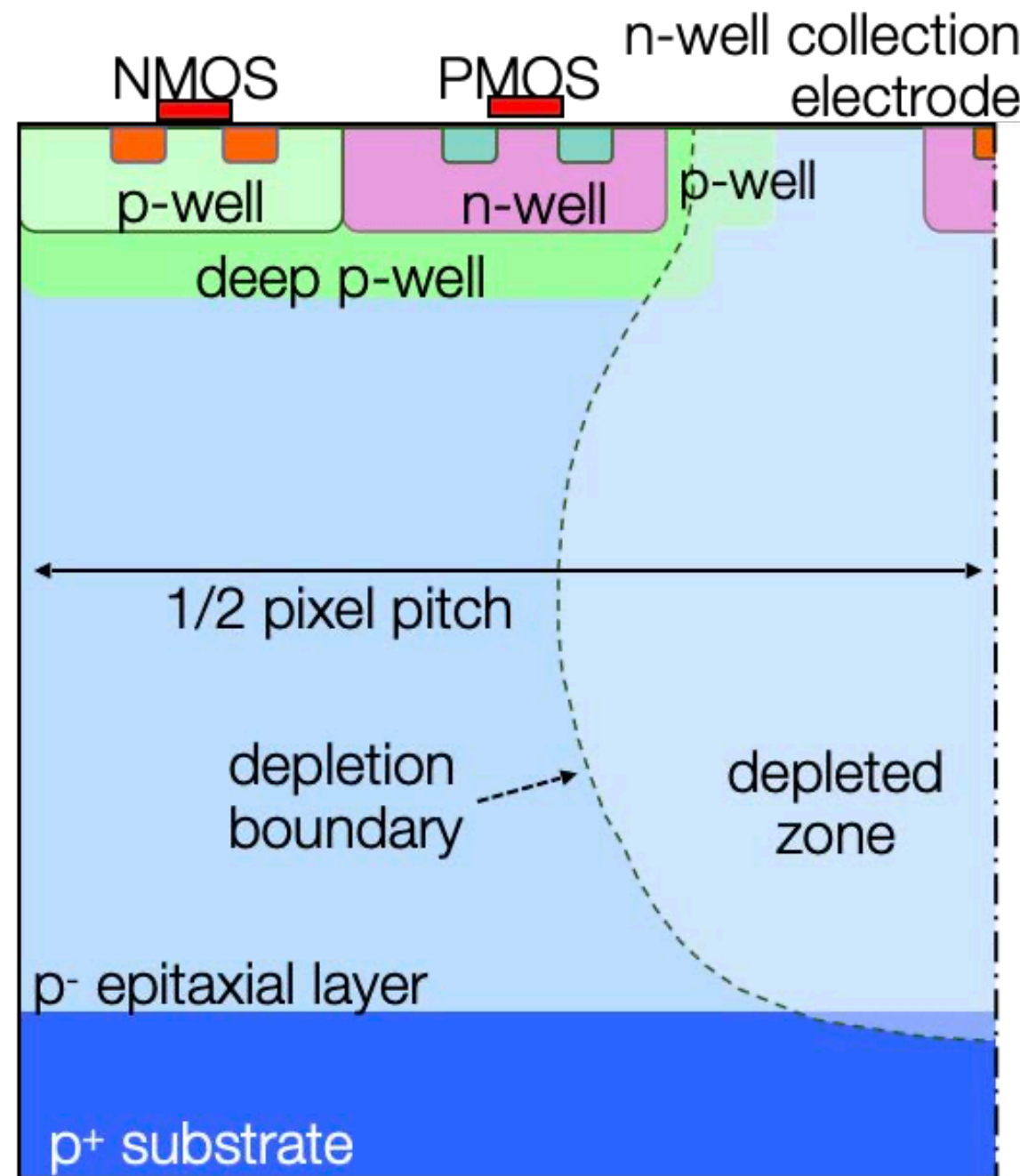
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Modified process

- Developed within ALICE ITS2
- Significantly increase depletion
- Faster charge collection
- Slow horizontal charge transport from the pixel edges and corners

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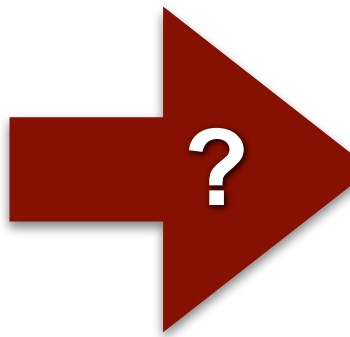
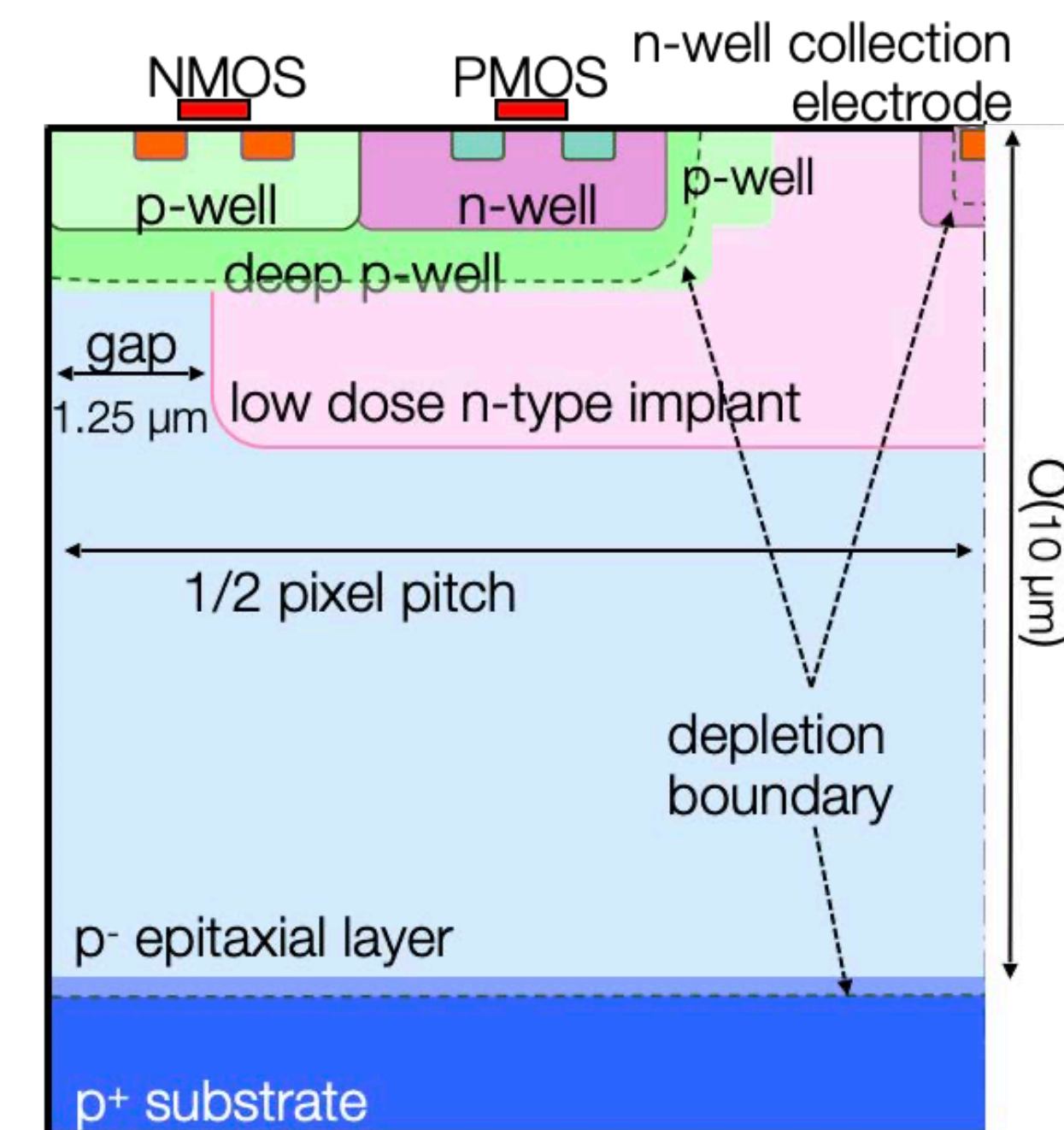
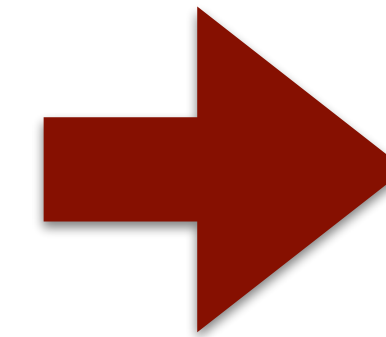
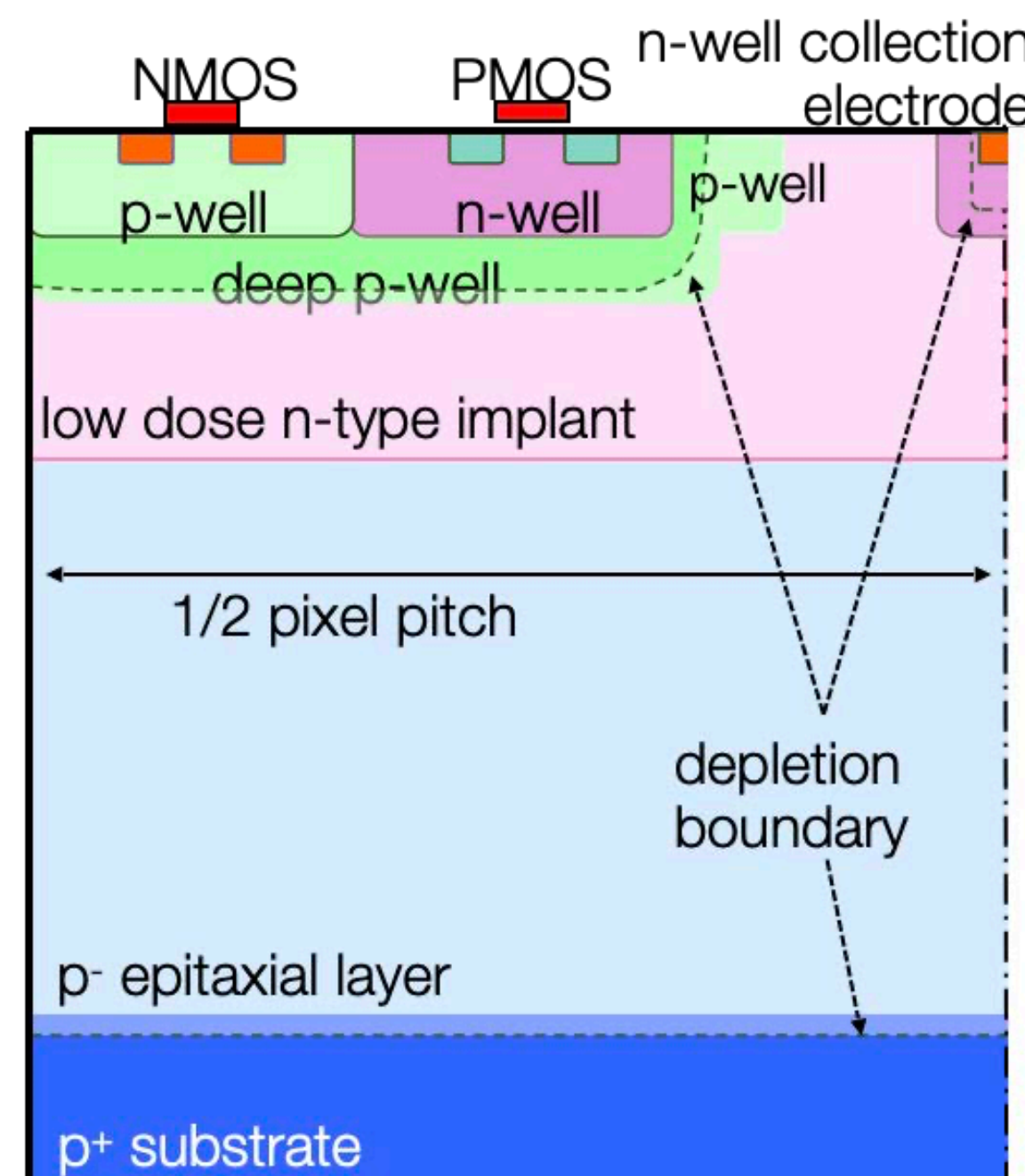
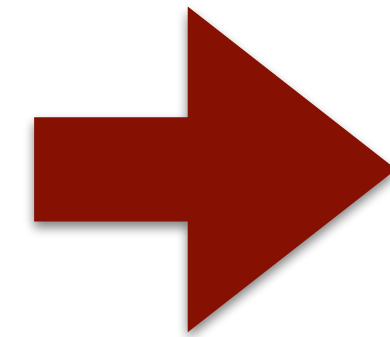
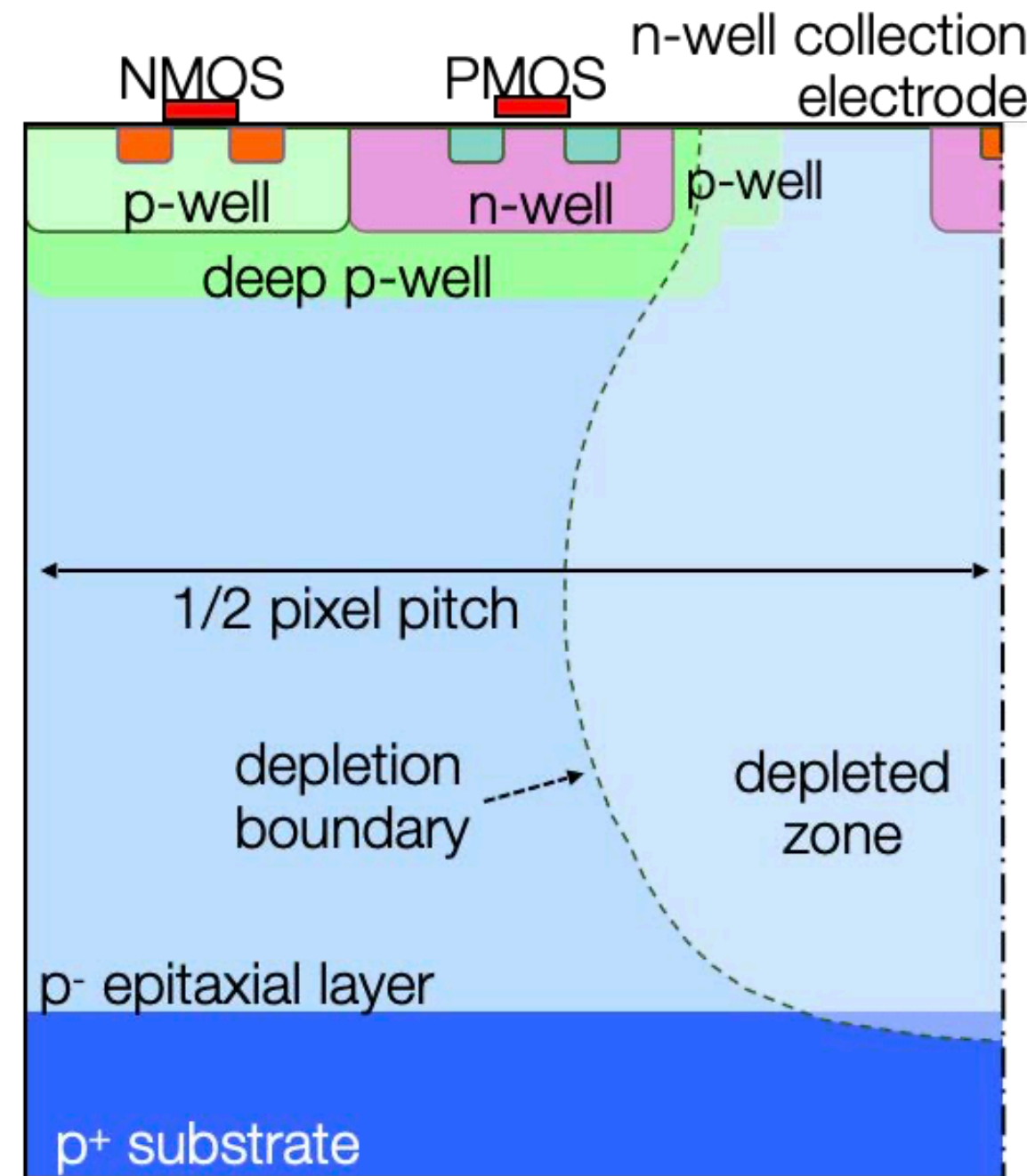
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Modified process with gap

- Further optimization in the MALTA context
- Improved charge collection from the edges

Towards a ALICE 3 pixel sensor — improving charge collection



Standard process

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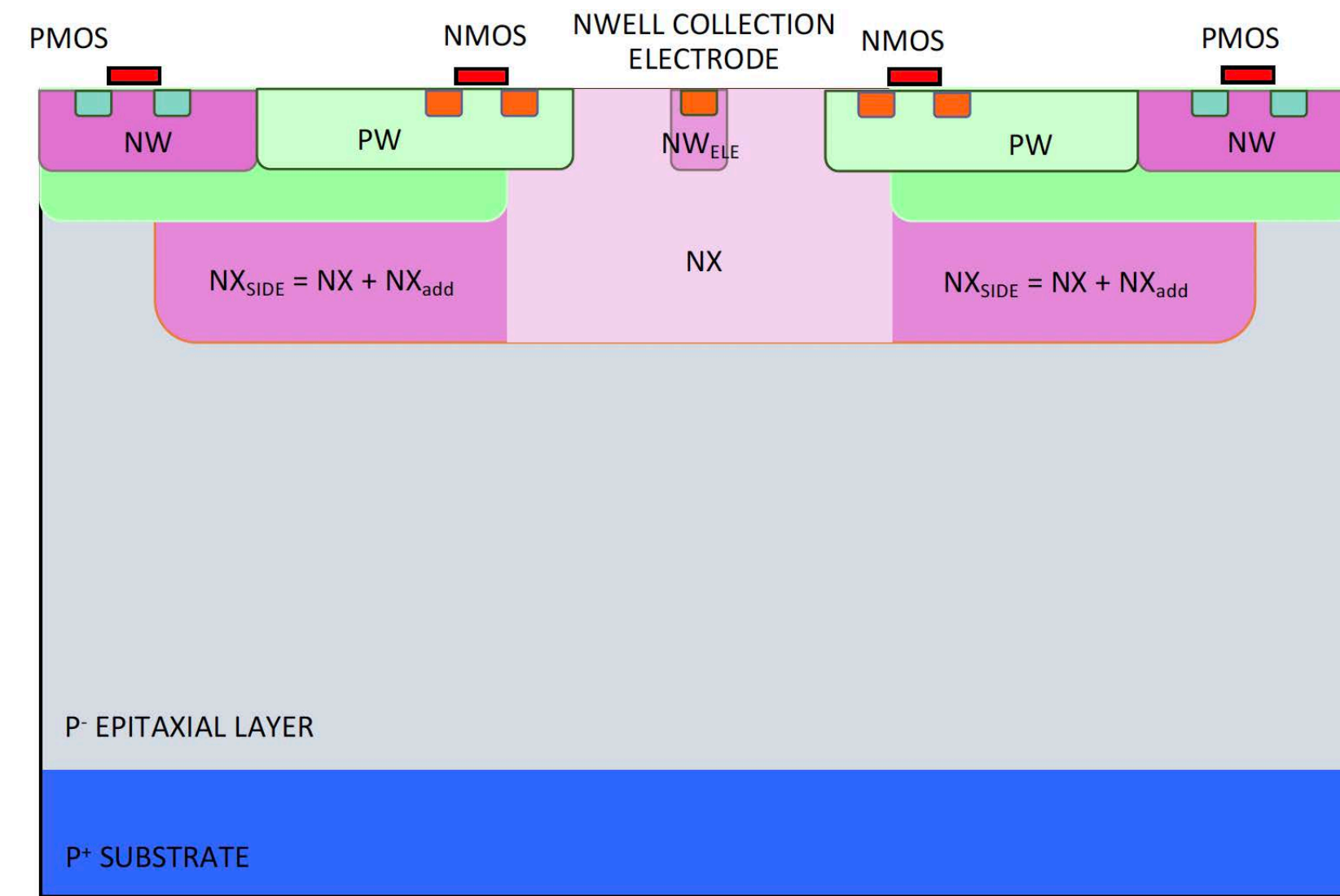
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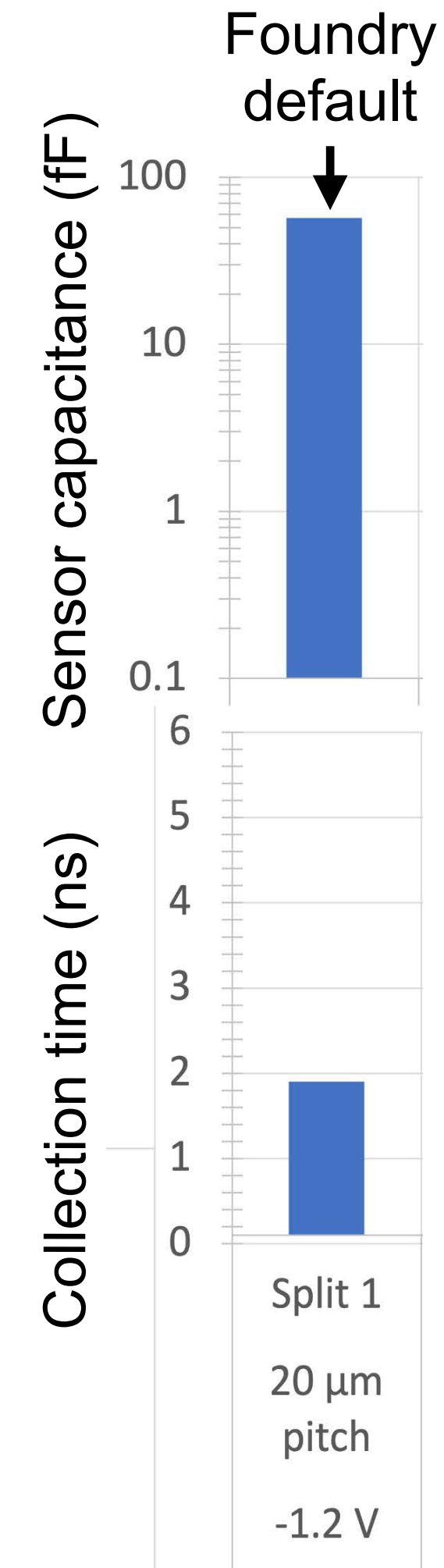
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Towards an ALICE 3 pixel sensor — improving charge collection (2)

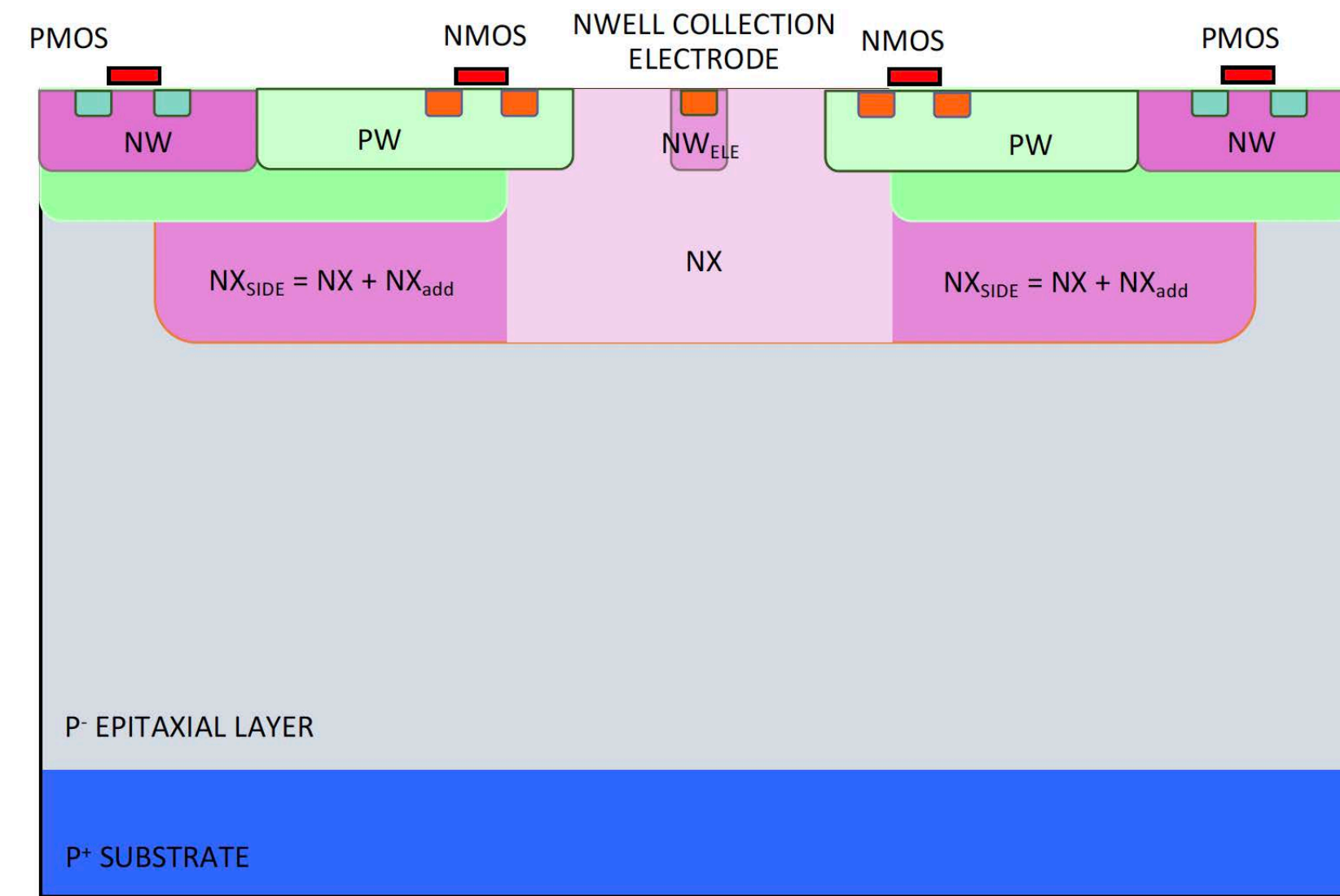


- Further improvement of the collection electrode

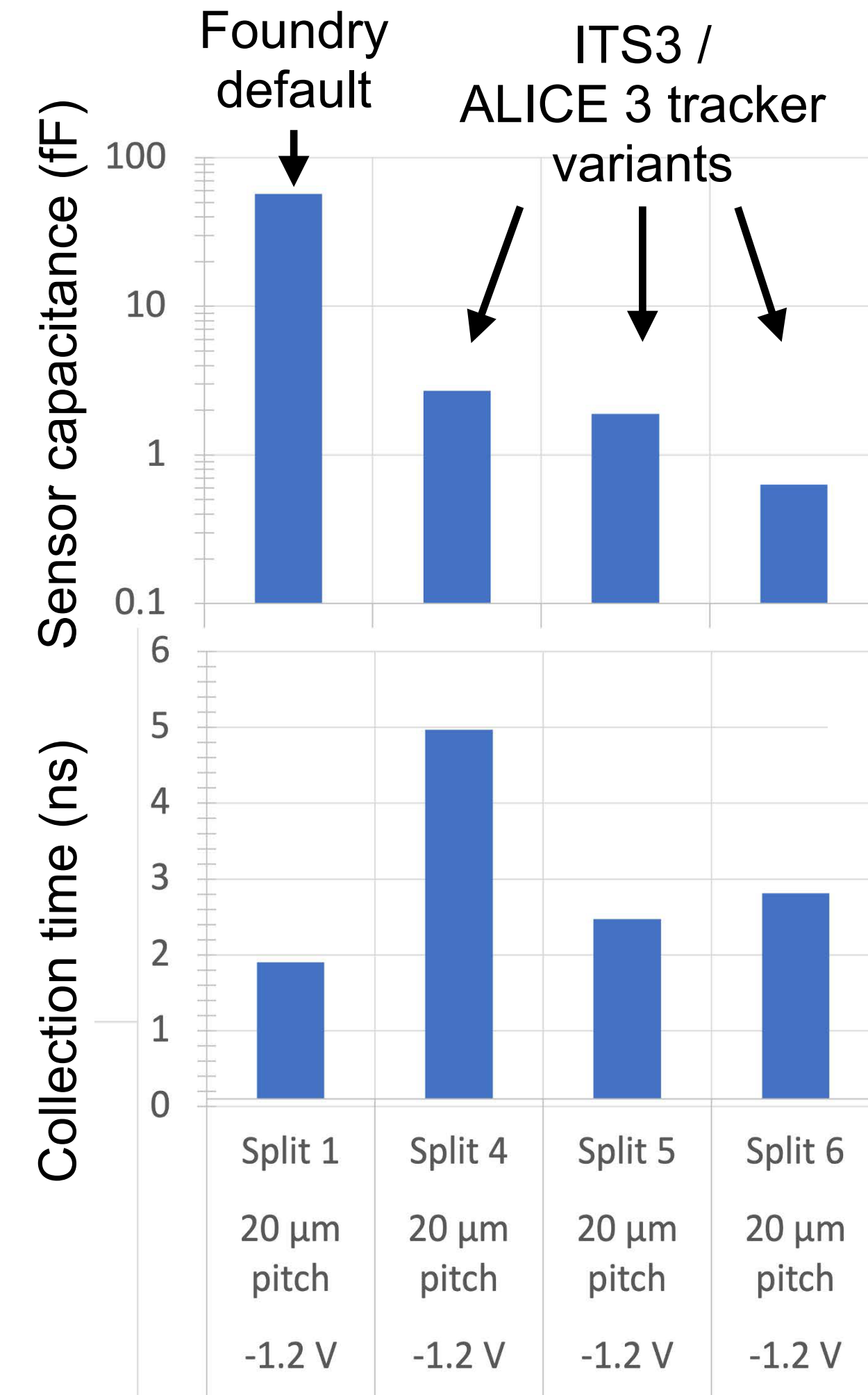


Simulations of different pixel optimisations (“splits”)

Towards an ALICE 3 pixel sensor — improving charge collection (2)

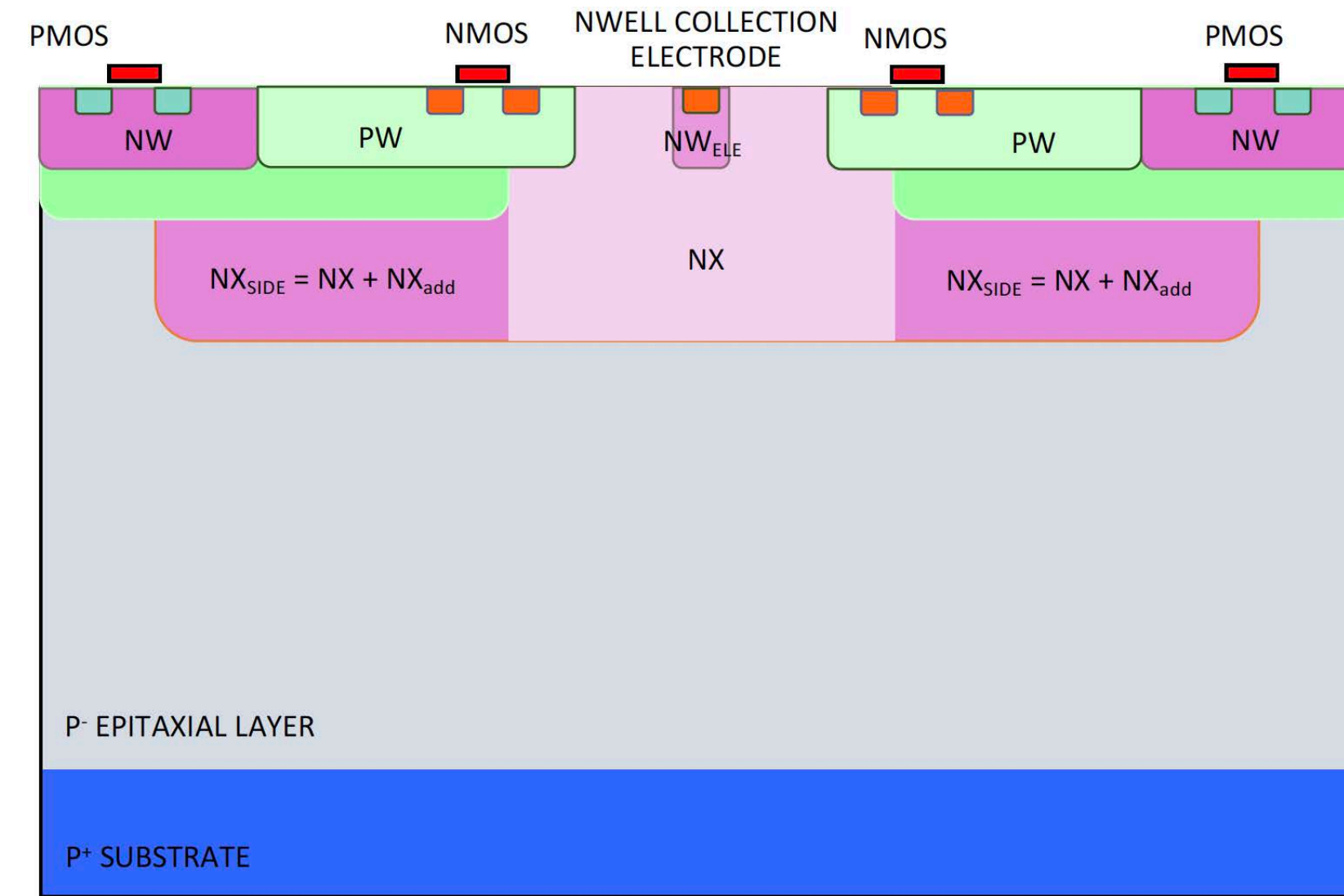


- Further improvement of the collection electrode
- Lower capacitance $\Rightarrow$ improved signal-to-noise ratio

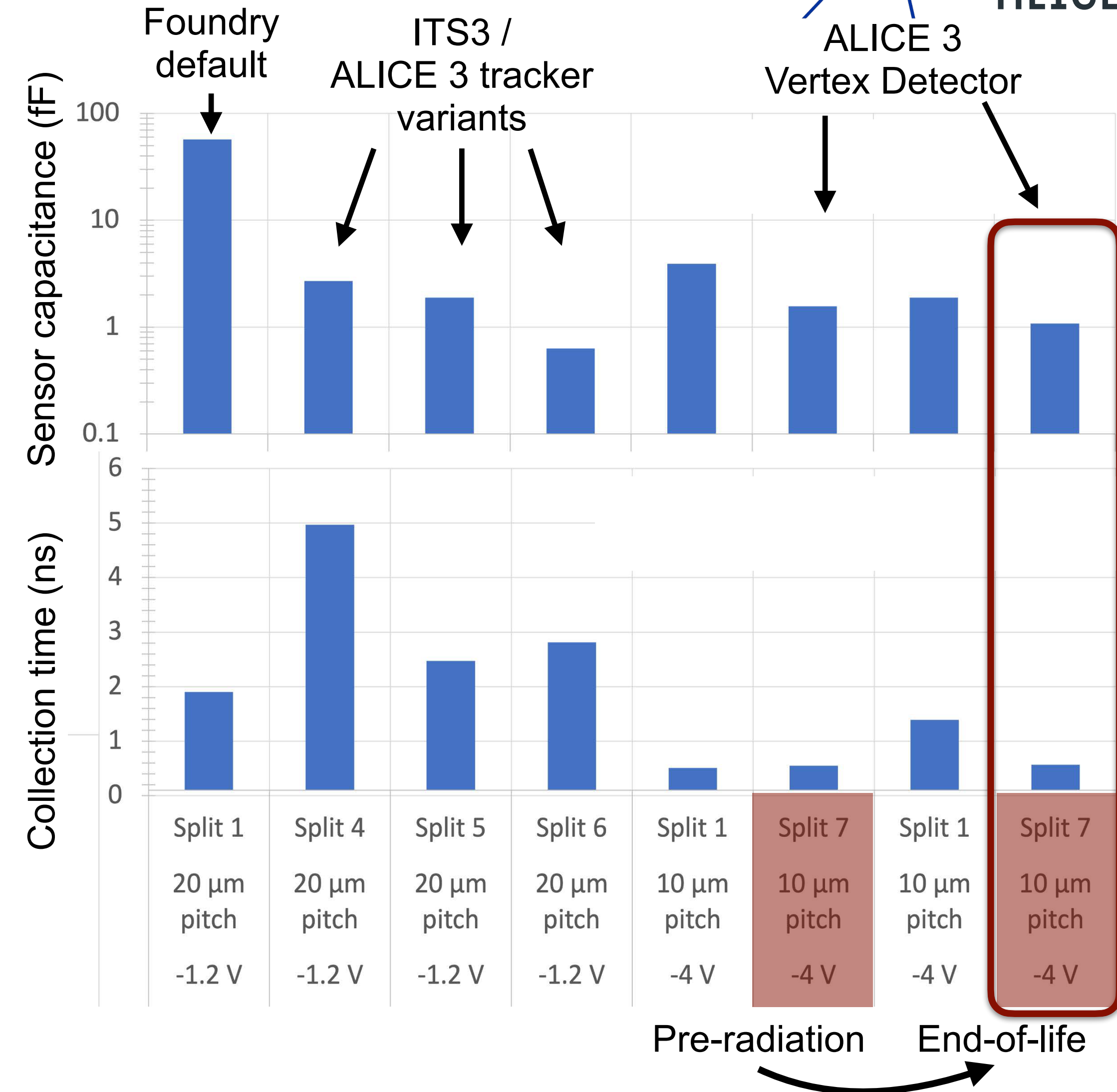


Simulations of different pixel optimisations (“splits”)

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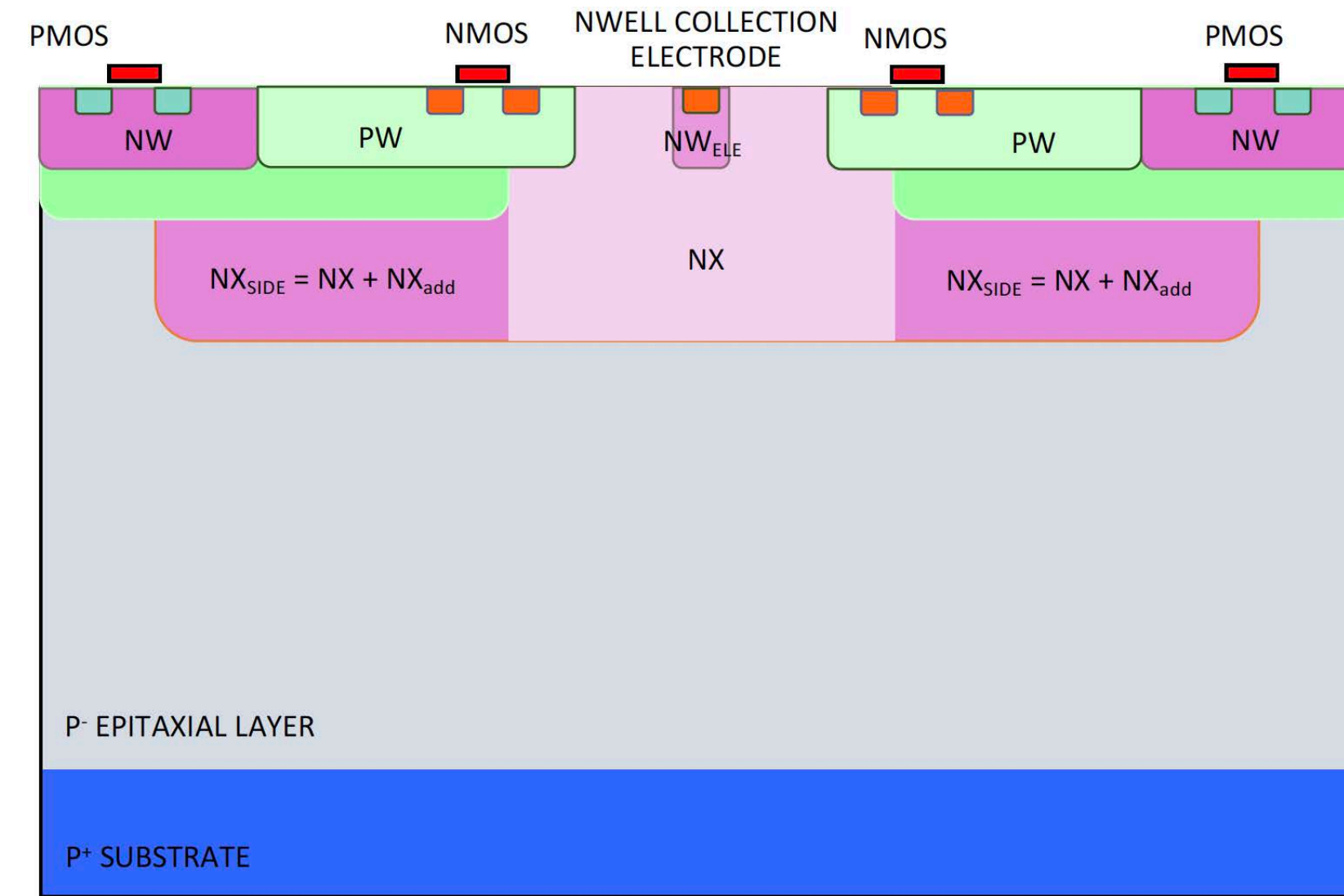


- Further improvement of the collection electrode
- Lower capacitance $\Rightarrow$ improved signal-to-noise ratio
- Faster, efficient charge collection, utilizing larger reverse substrate bias (-4 V instead of -1.2V) $\Rightarrow$ improved radiation tolerance

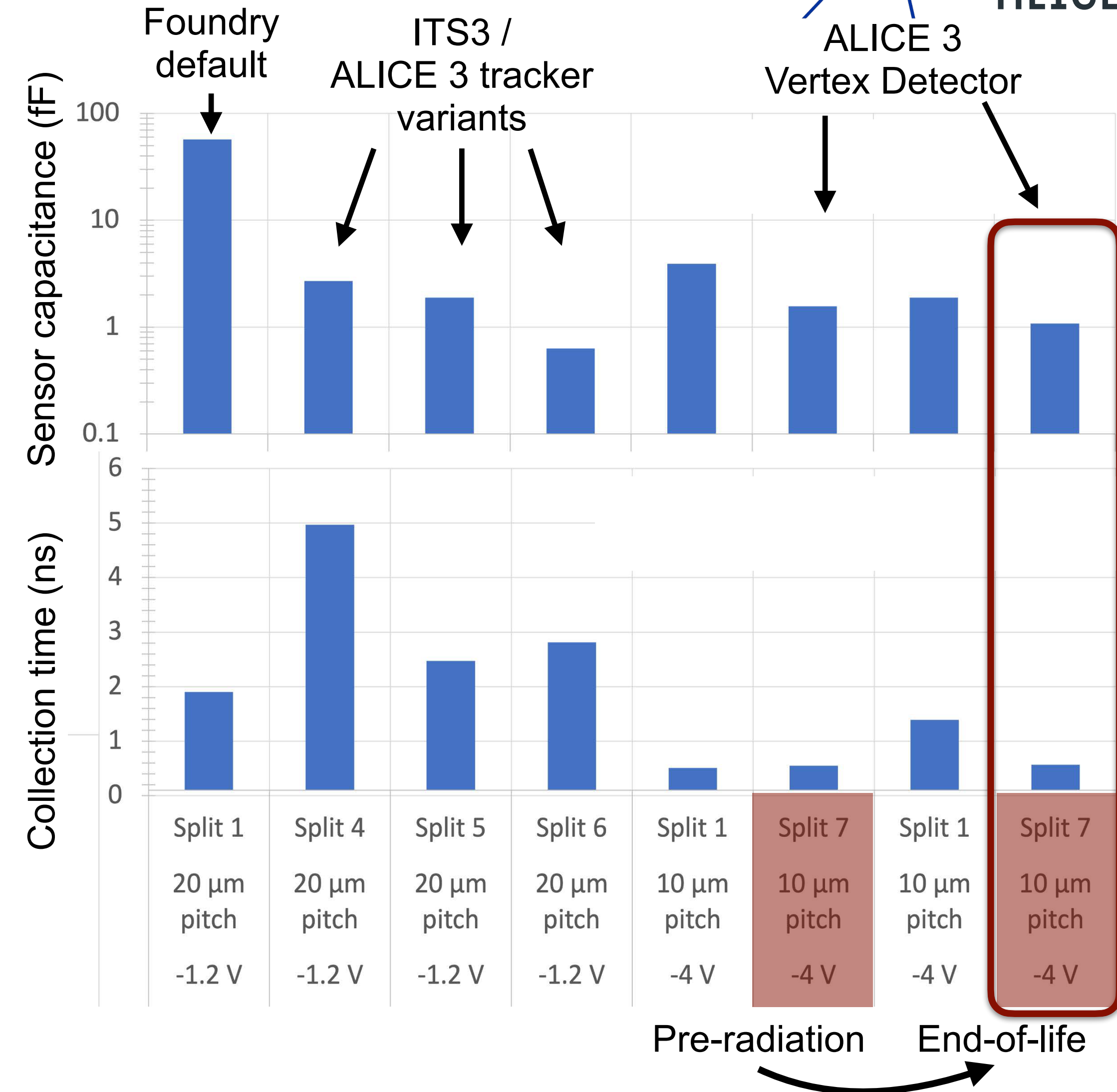


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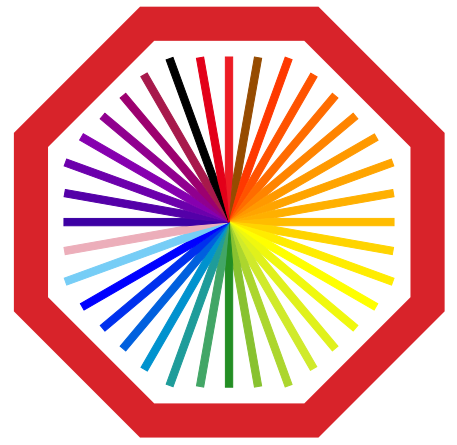
Towards an ALICE 3 pixel sensor — improving charge collection (2)



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- Faster, efficient charge collection, utilizing larger reverse substrate bias (-4 V instead of -1.2V) $\Rightarrow$ improved radiation tolerance
- Test chips expected in February

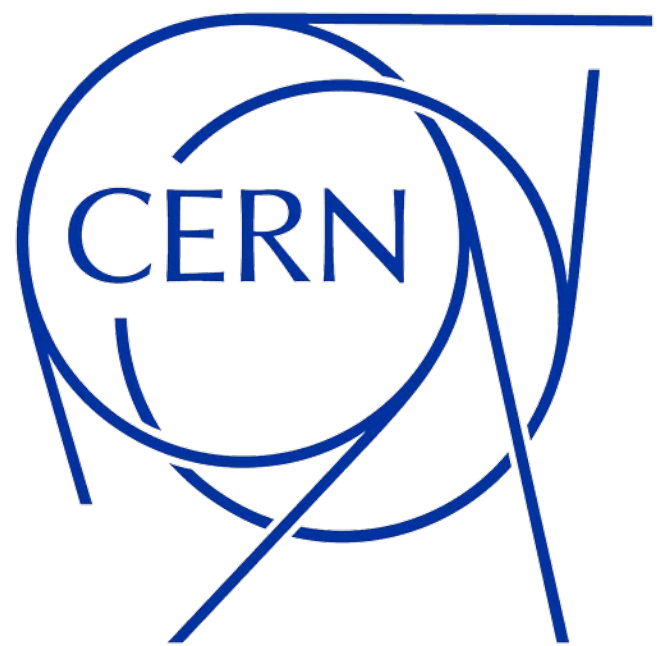


Simulations of different pixel optimisations (“splits”)

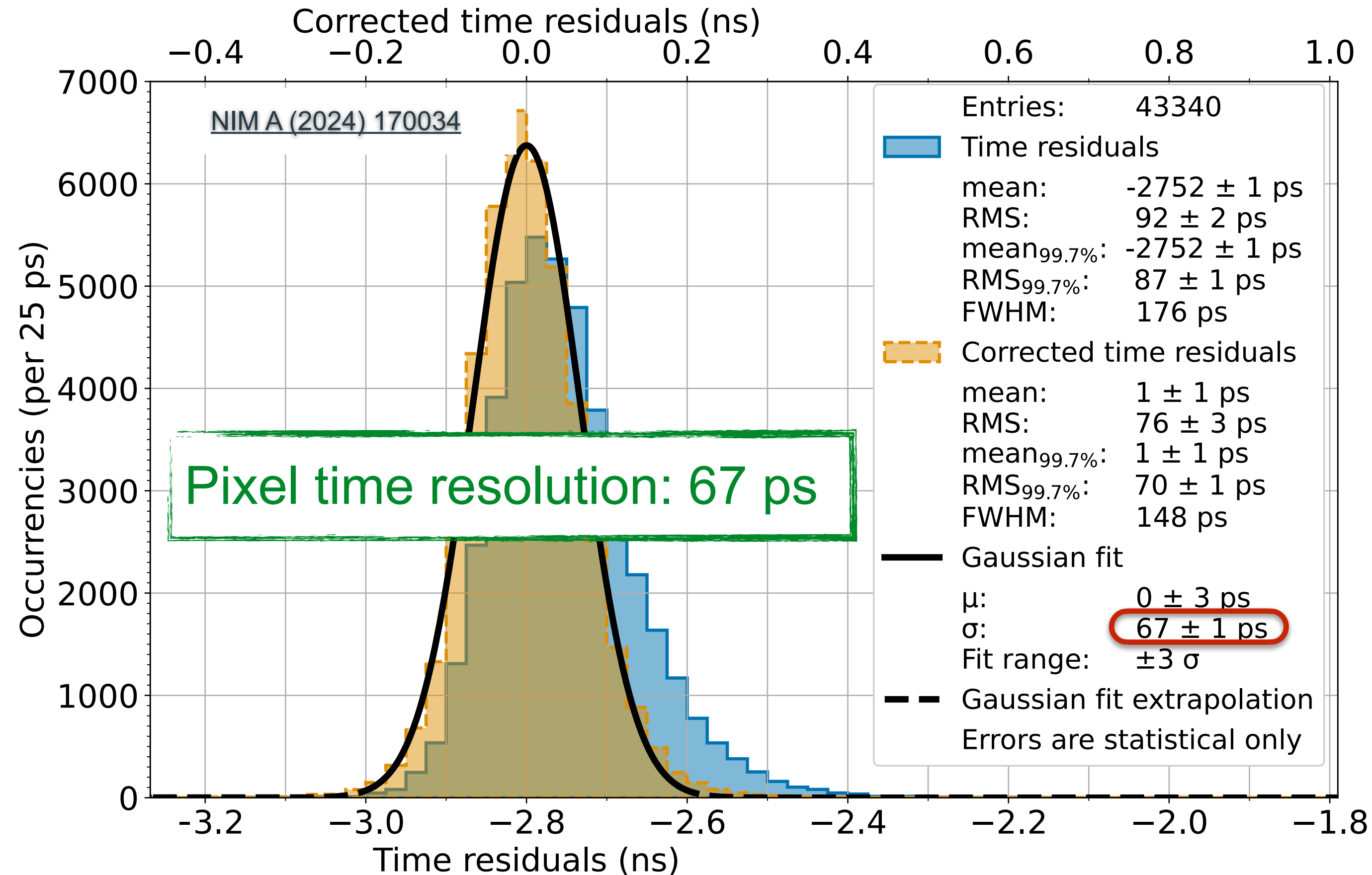


ALICE

Beyond ALICE



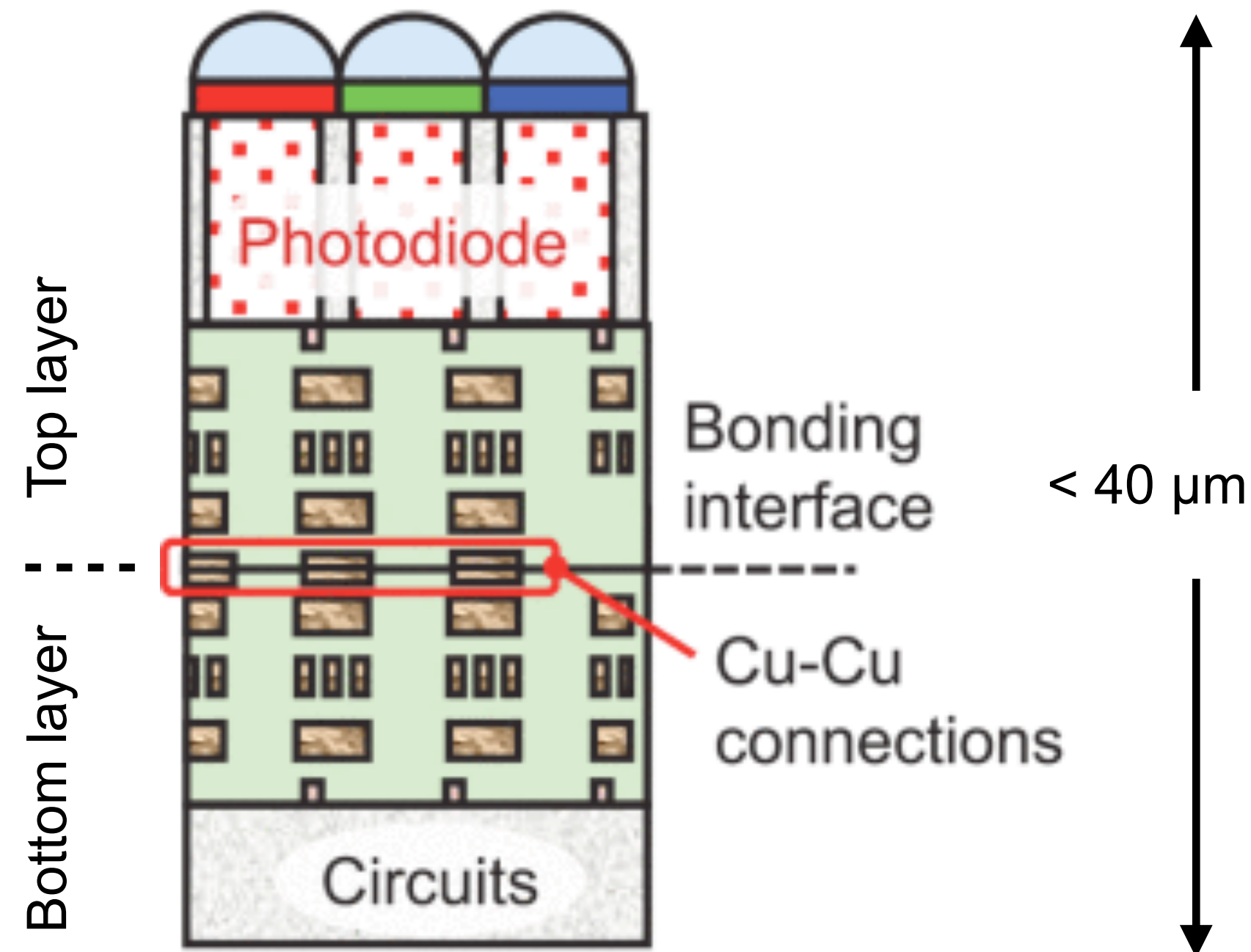
Beyond ALICE — pixel timing resolution



- 67 ps time resolution measured with APTS-OA test chip:
 - With analogue output
 - No gain layer (like in e.g. LGADs)
 - 10 μm pixel pitch
- Exploitation in fully integrated sensor power intensive

Pixel timing resolution @ - 4.8 V reverse-substrate bias, 10 μm pitch

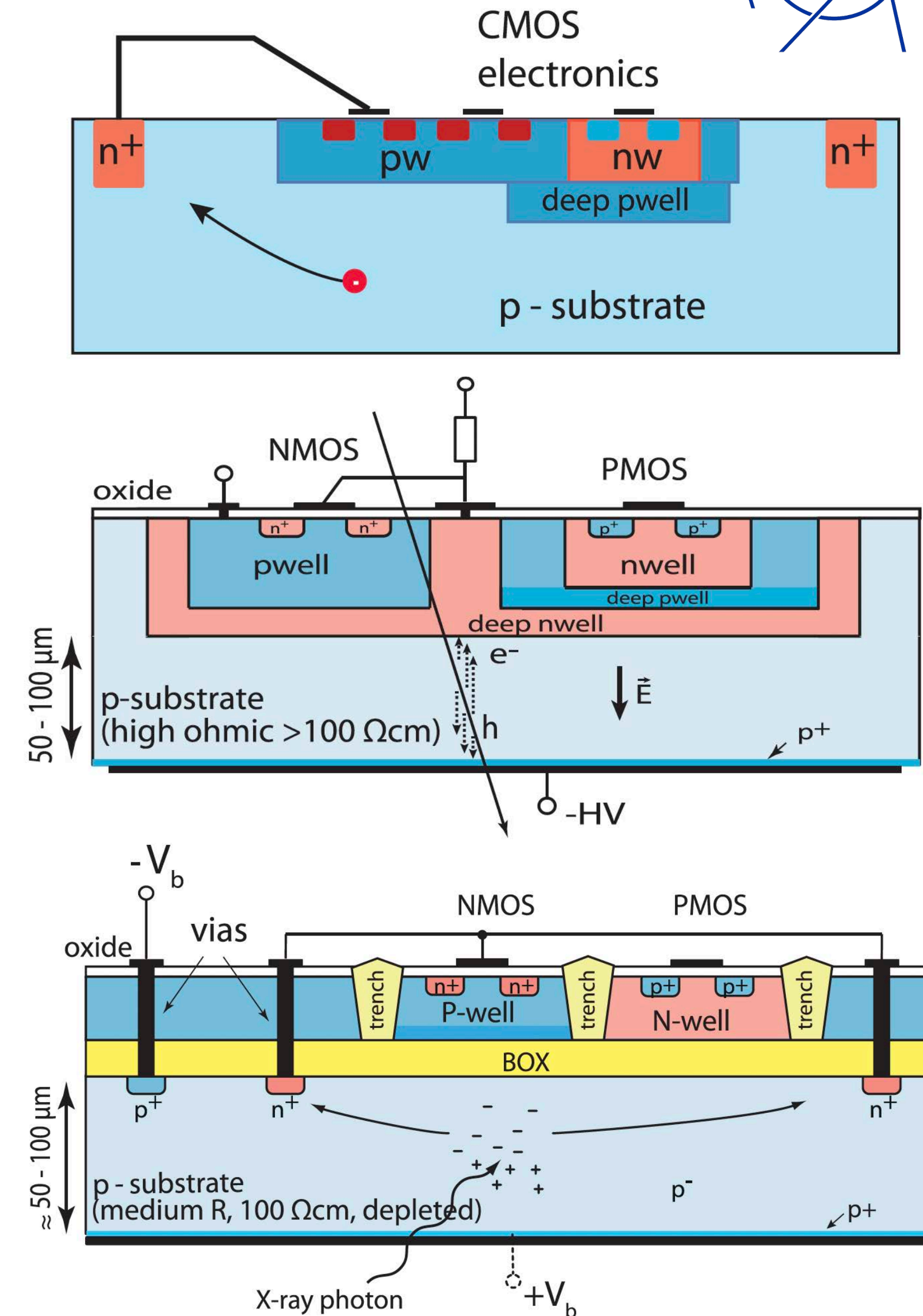
Beyond ALICE — wafer stacking

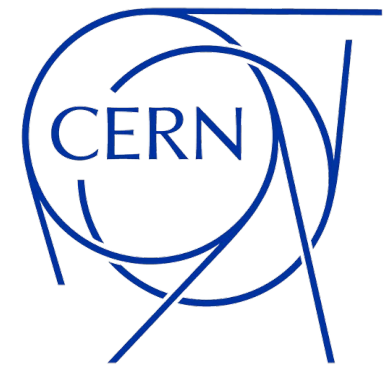


- Increasingly employed for high-end image sensors
- Direct Cu-Cu connections w/ small connection pitches ($O(1\text{ }\mu\text{m})$)
 - ➔ allowing for multiple connections per pixel
- Possibility to use multiple chips to implement functionality
 - Advantages
 - More complex circuitry possible
 - Compact
 - Can combined optimized technologies particle for detection and processing
 - Drawbacks
 - Need to design multiple chips
 - Increased cost and complexity

Similar developments

- Other small collection electrode developments:
(CLICTD, MALTA, FastPix, MIMOSIS, OBELIX, CEPC chips, ARCADIA,...)
 - Small collection electrode featuring small capacitance
 - Limited active volume thickness (few tens of μm)
 - Moderate reverse-substrate bias
- HV-CMOS developments
(MuPix, MightyPix, ATLASpix, RD-50 chips, LF-Monopix, COFFEE,...)
 - Large collection electrode encompasses electronics
 - High voltage ($O(10\text{ V})$) applied to the substrate
 - Larger ionization, but also larger capacitance
- Silicon-on Insulator (Sol)
 - Isolation layer separating electronics from active volume





Summary

- ITS2: 10 m² CMOS pixel-sensor-based detector operating successfully at LHC
- ITS3 is getting close to ideal vertex detector
 - Low material budget in the acceptance
 - Close to interaction point
 - Next step: testing of full-size, full-functionality prototype pixel sensor
- ALICE 3 poses the next major challenge
 - Extreme environment in the Vertex Detector
 - Very large surface, low power tracker
- What might be next? ALICE 3 is a de-facto prototype for an FCC-ee detector

Thanks a lot for your attention



Picture taken with
ALPIDE-based camera