The state of the art and future of CMOS particle sensors for high energy physics

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on behalf of the ALICE collaboration


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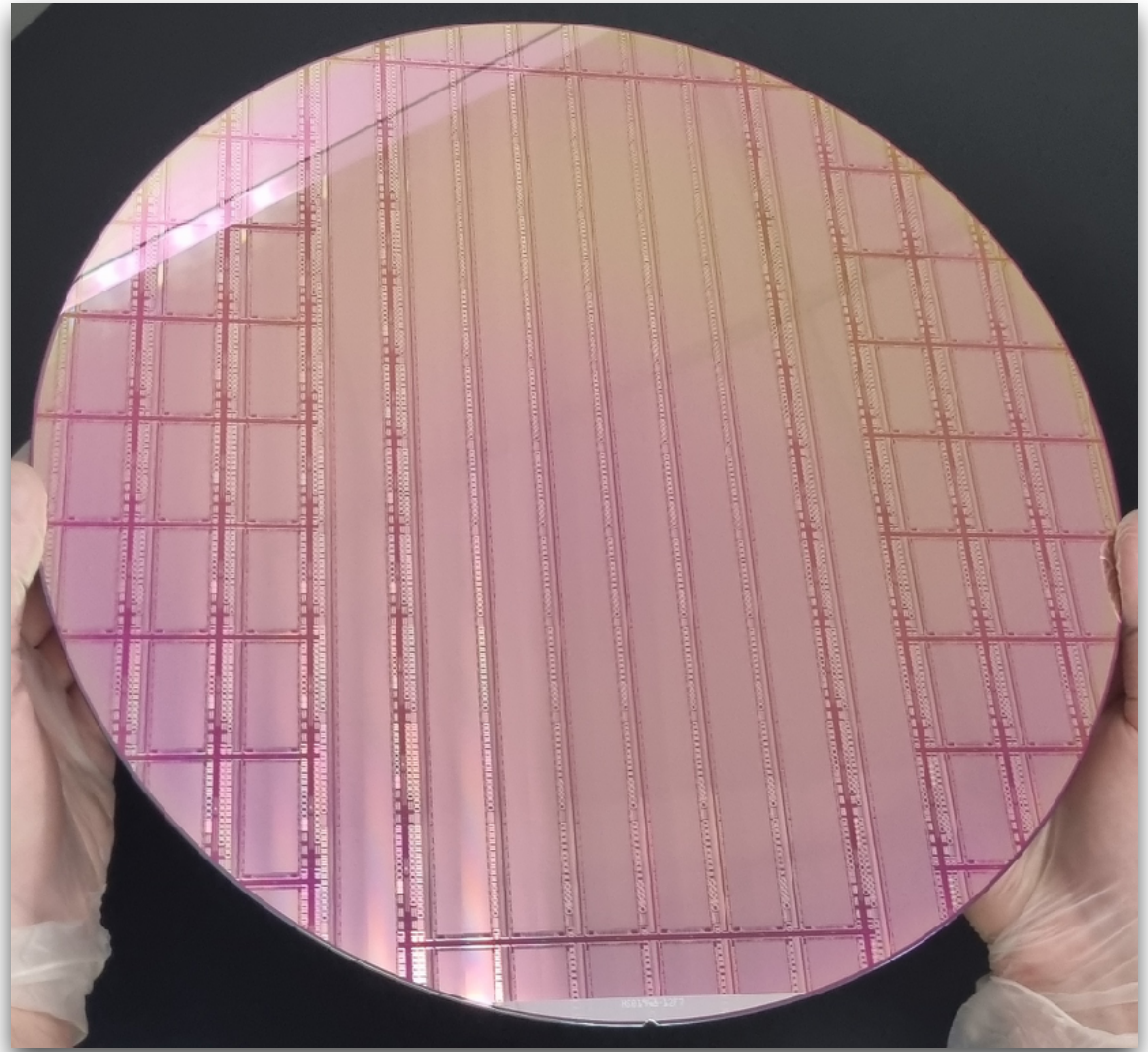
Outline

- **CMOS image/particle sensors**
  - motivations
  - working principle
- **State of the art**
  - 180 nm MAPS technology (ALPIDE, ALICE ITS2, CBM, Belle II et al.)
  - reaching full depletion
  - other developments (HVMAPS, SOI)
- **Current future**
  - 65nm technology
  - wafer-scale sensors
  - bent detectors
- **Further future**

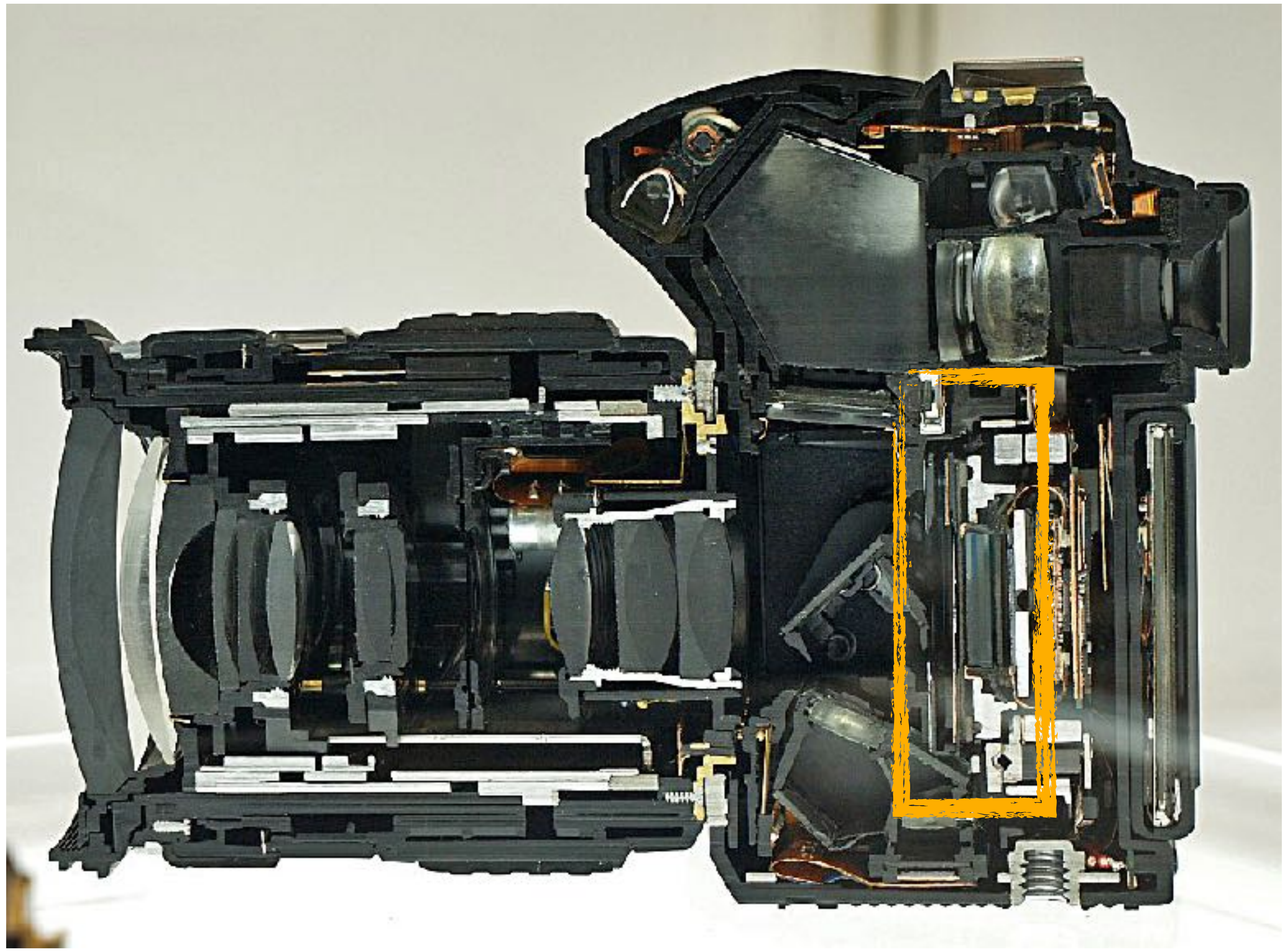


Introduction

Pixel detectors

… are nowadays present *everywhere*

Nobel Prize in Physics 2009
Willard S. Boyle and George E. Smith
"for the invention of an imaging semiconductor circuit – the CCD sensor."

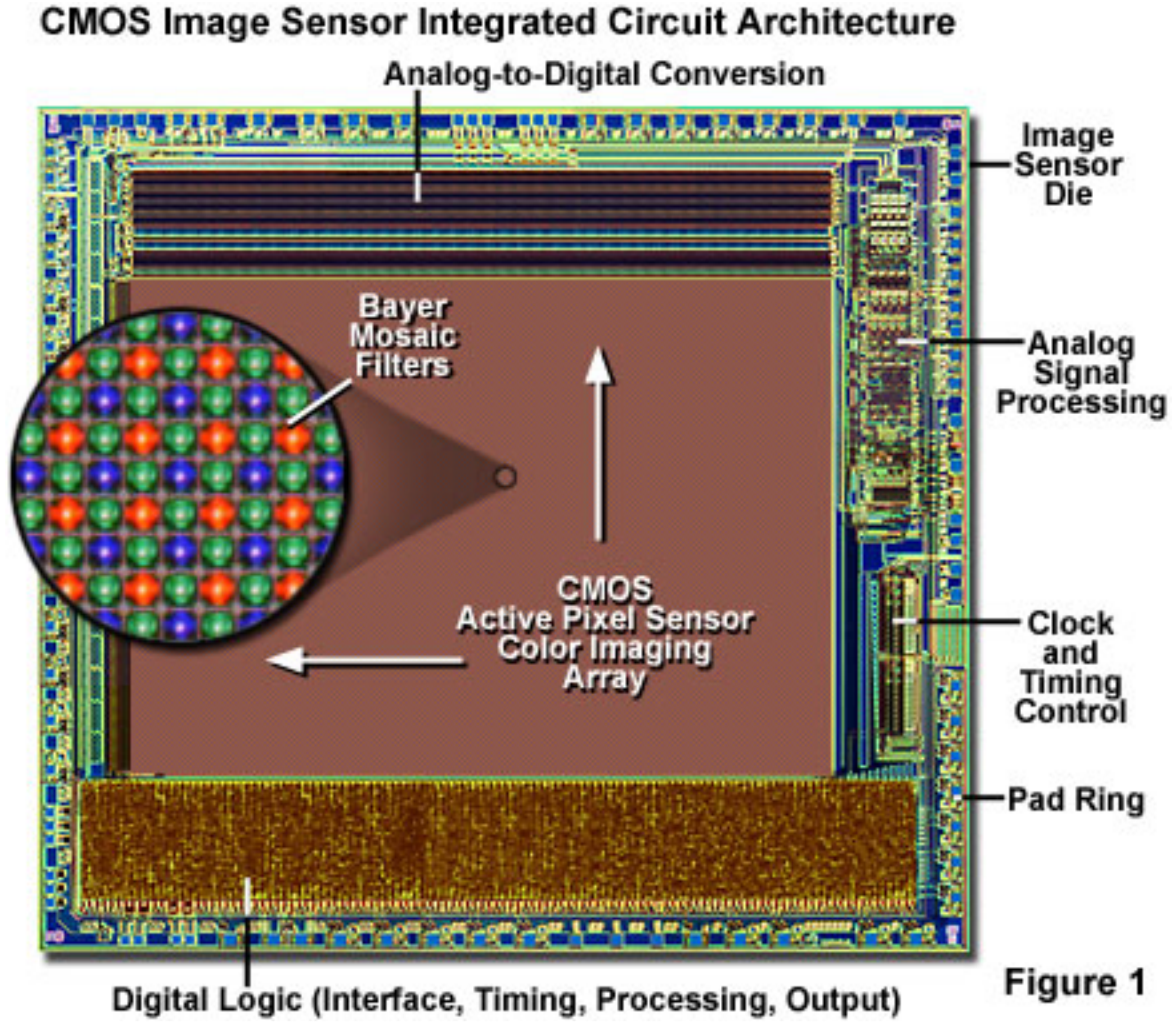


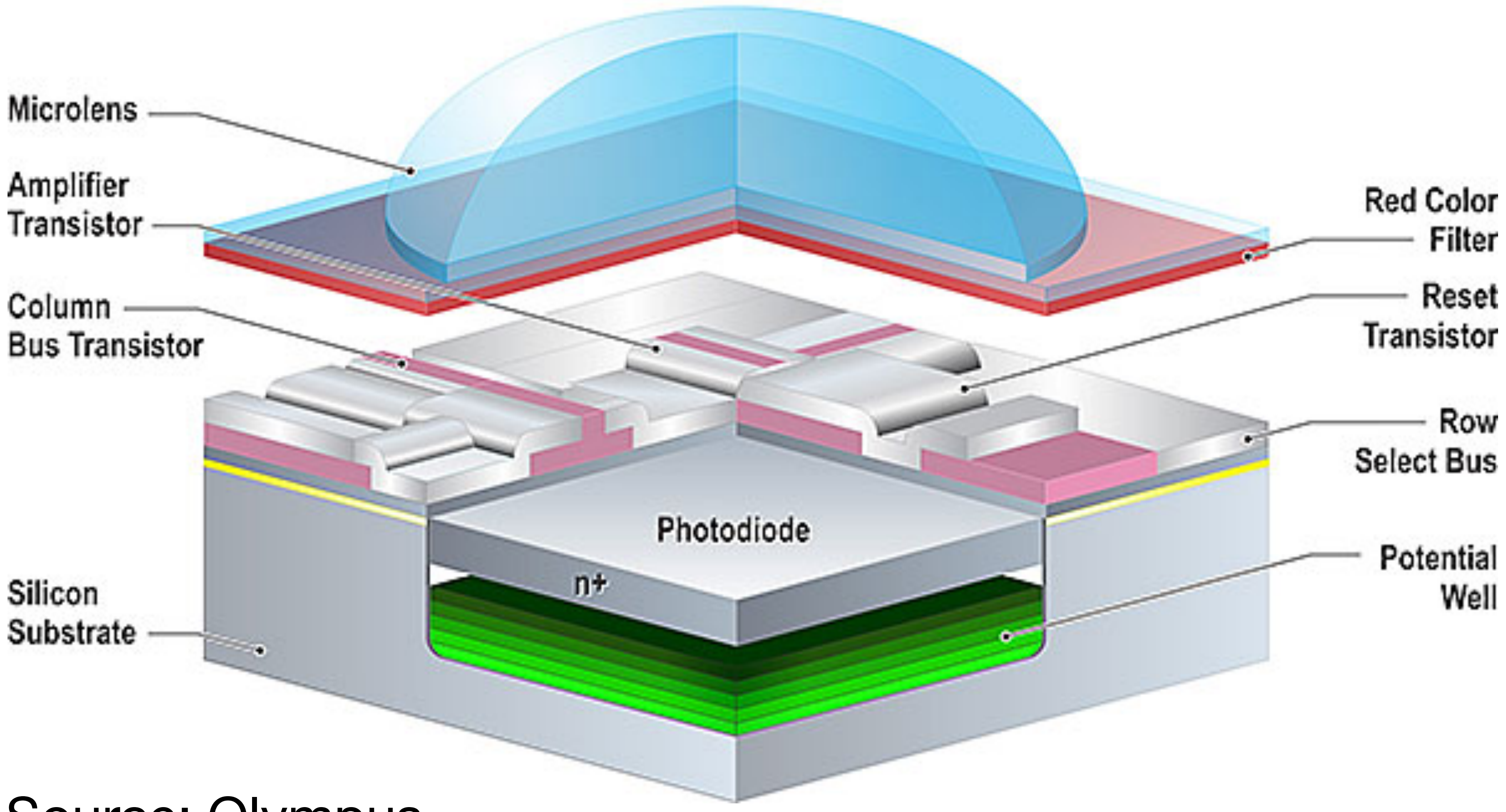
[https://commons.wikimedia.org/wiki/File:E-30-Cutmodel.jpg]

Cut through a modern DSLR
Pixel detectors are abundant (smartphones, surveillance, etc.)
though mostly for (visible) light

CMOS image sensors

… are nowadays present *everywhere*



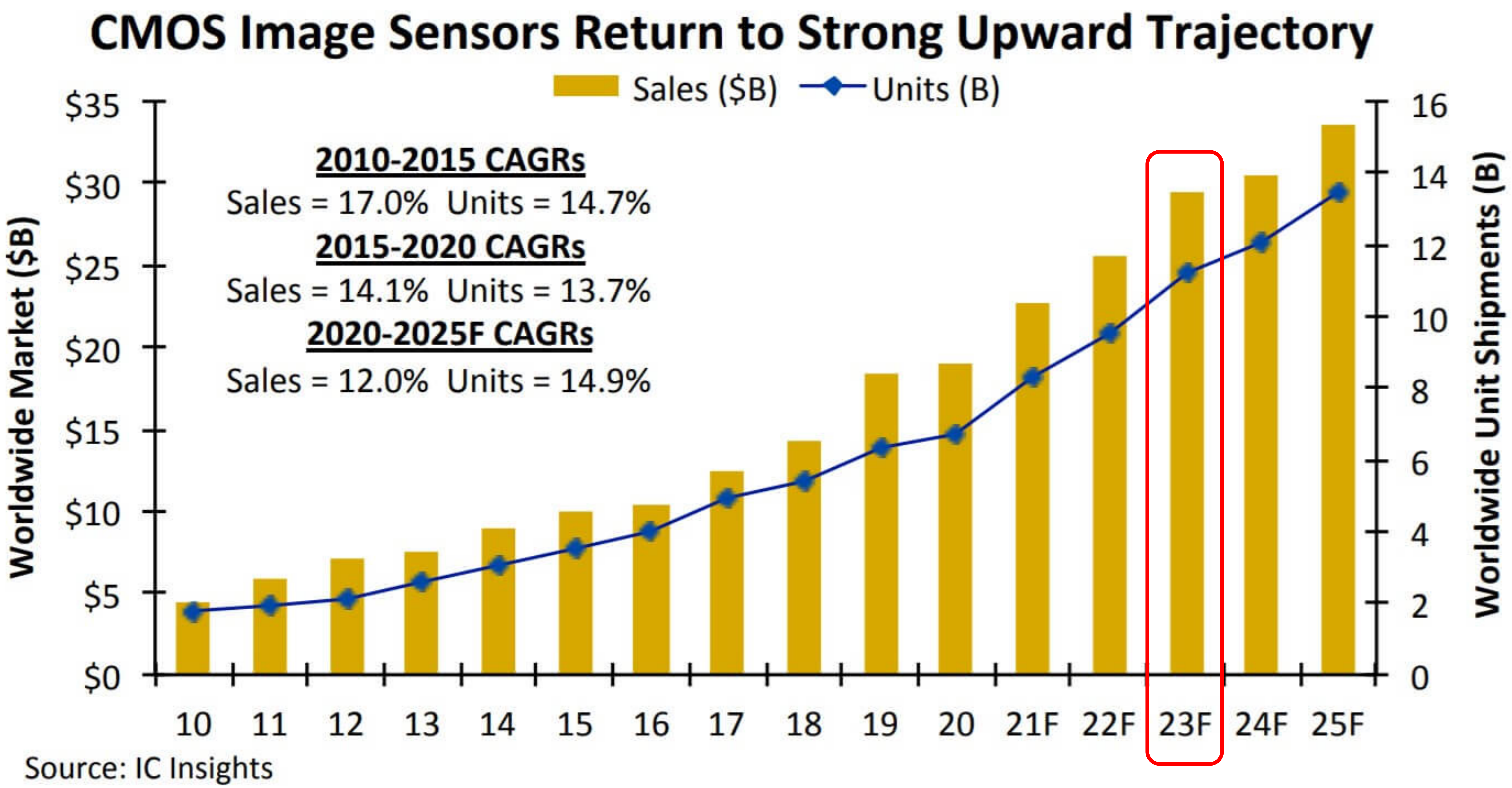


Source: Olympus

- Nowadays the most widespread implementation of image sensors
  - main advantage: price
- Light vs charged particles:
  - both generate electron/hole pairs
  - need to increase sensitive area to 100% (no focussing lenses for charged particles)

CMOS image sensor market

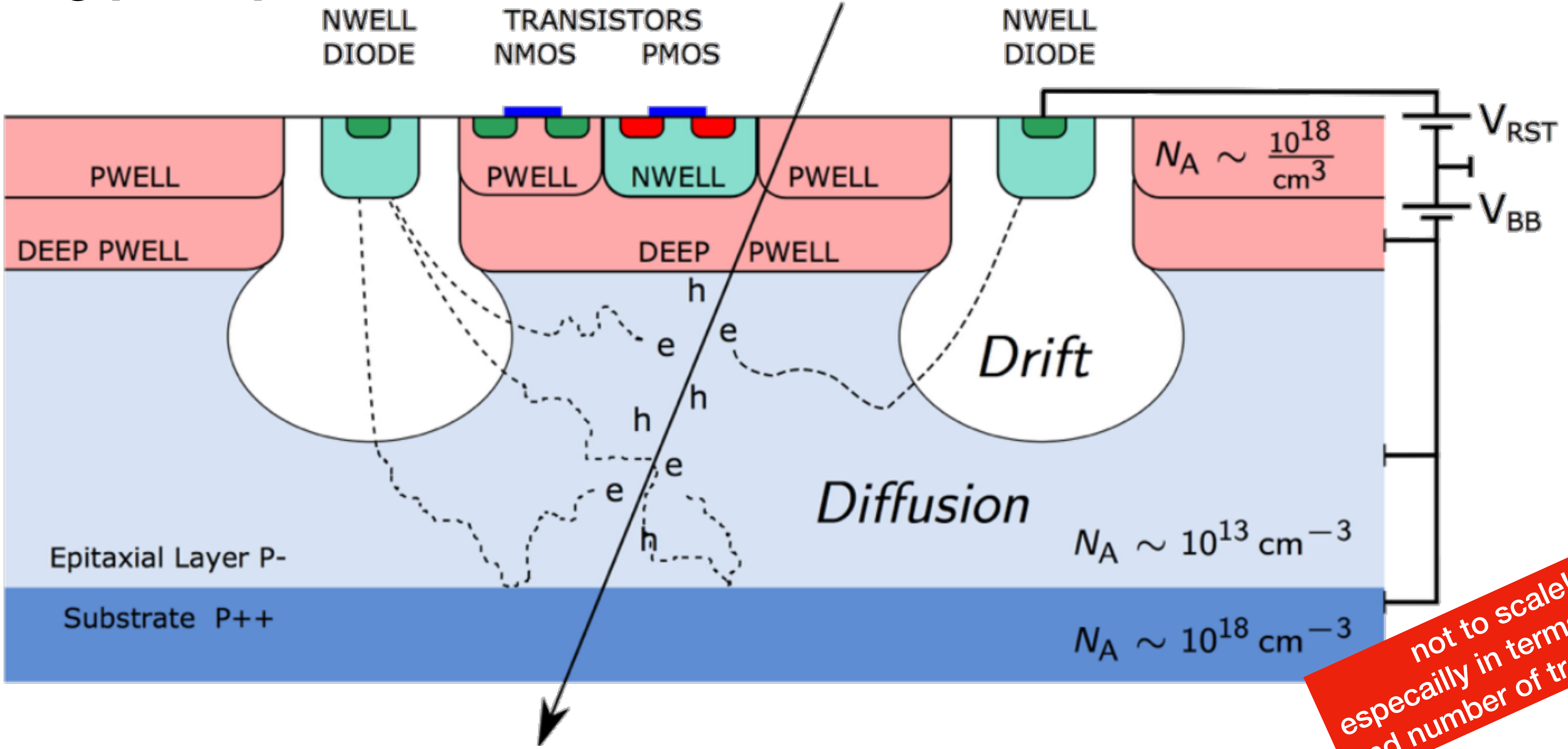
rapidly growing



- Huge commercial interest
- A lot of development ongoing in industry
- Many developments are directly applicable to particle detectors
- Available in large quantities

Monolithic active pixel sensors (MAPS)

working principle

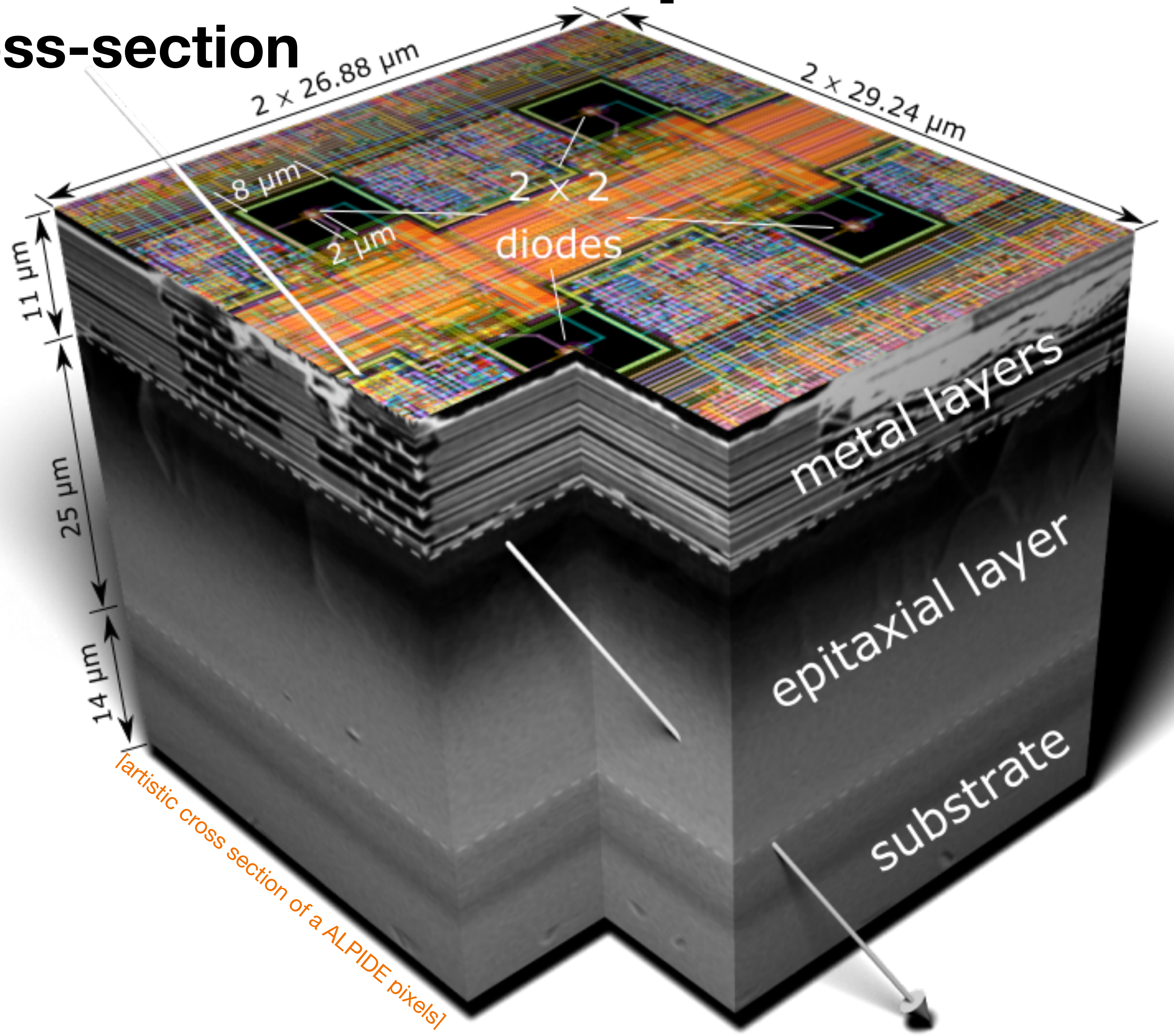


not to scale! especailly in terms of size and number of transistors.

This is the basic structure of “ALPIDE”-like sensors. A lot of effort is put into improving the charge collection/drift regions.

Monolithic active pixel sensors (MAPS)

cross-section



- Thin: O(50 µm)
- Very granular: O(10-30 µm)
- Small diodes: capacitances of O(1-5 fF)
- Highly integrated: O(100) transistors in-pixel

Performance and features

in reach for production tomorrow

- **Input capacitance:** O(1-5 fF)
- **Power density:** 20-40 mW/cm^2 (30 µm pixels)
- **Material budget:** 0.05% (50 µm Si)
  - additional gain from low power consumption
- **Pixel pitch:** 10-30 µm
- **Spatial resolution:** O(5 µm)
- **Time resolution:** O(1 ns - 1 µs)
  - intrinsic charge collection faster O(100 ps)
- **Detection efficiencies:** 100%
- **Radiation hardness:**
  - NIEL: 10^{15} 1MeV n_{eq}/cm^2
  - TID: several Mrad
  - SEE: mitigation techniques exist

The best tradeoff *can* to be chosen to fit the specific application

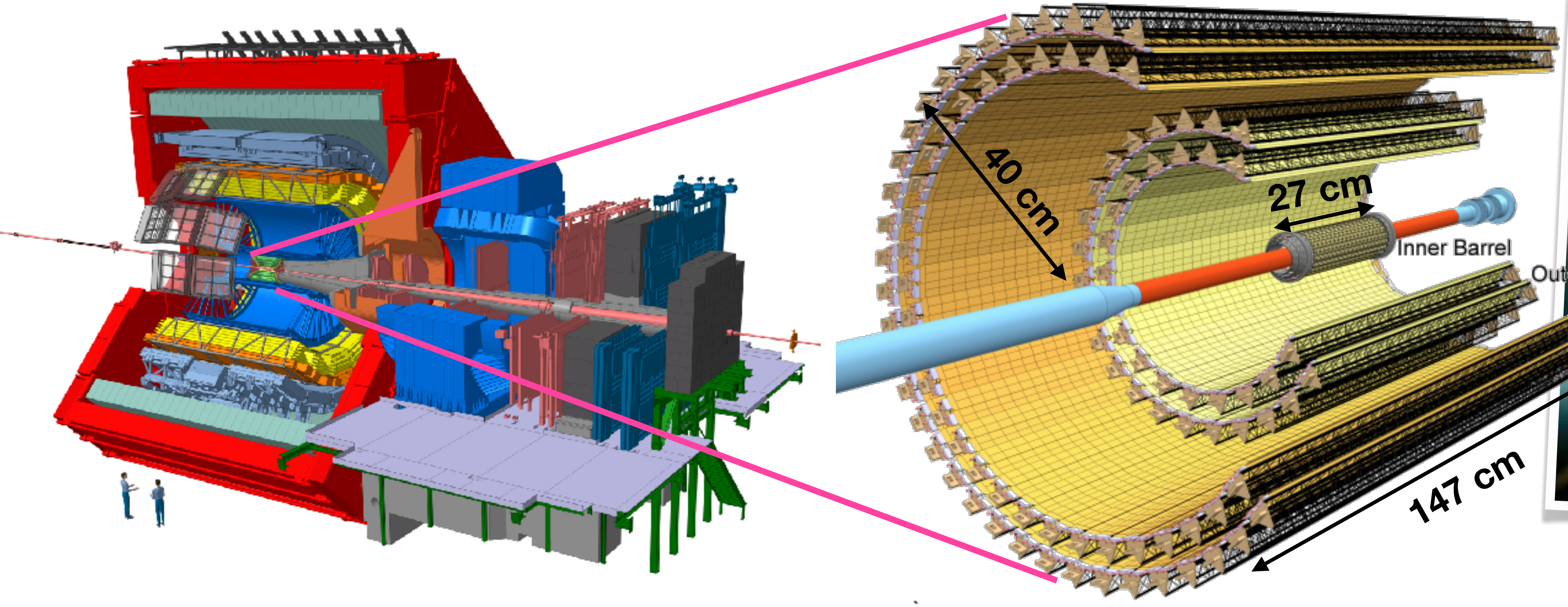
All parameters are still being improved a lot in oging R&D activities

State of the art

ALICE Inner Tracking System 2 (ITS2)

the large-scale application of MAPS

- > 20k **ALPIDE** chips are currently working on detector
  - > 70k chips produced, serving other experiments/ applications (sPHENIX, proton-CT, etc)
- Large step in the development of the technology



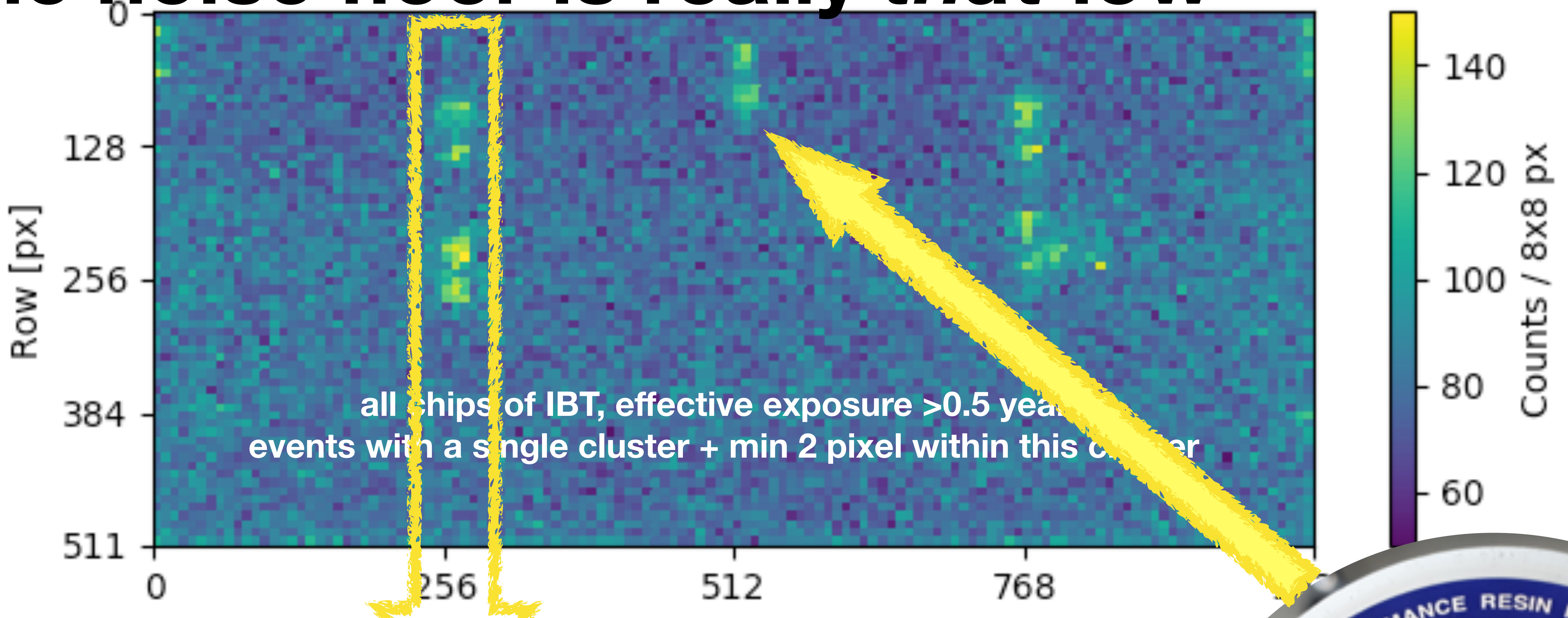
ITS2 installation

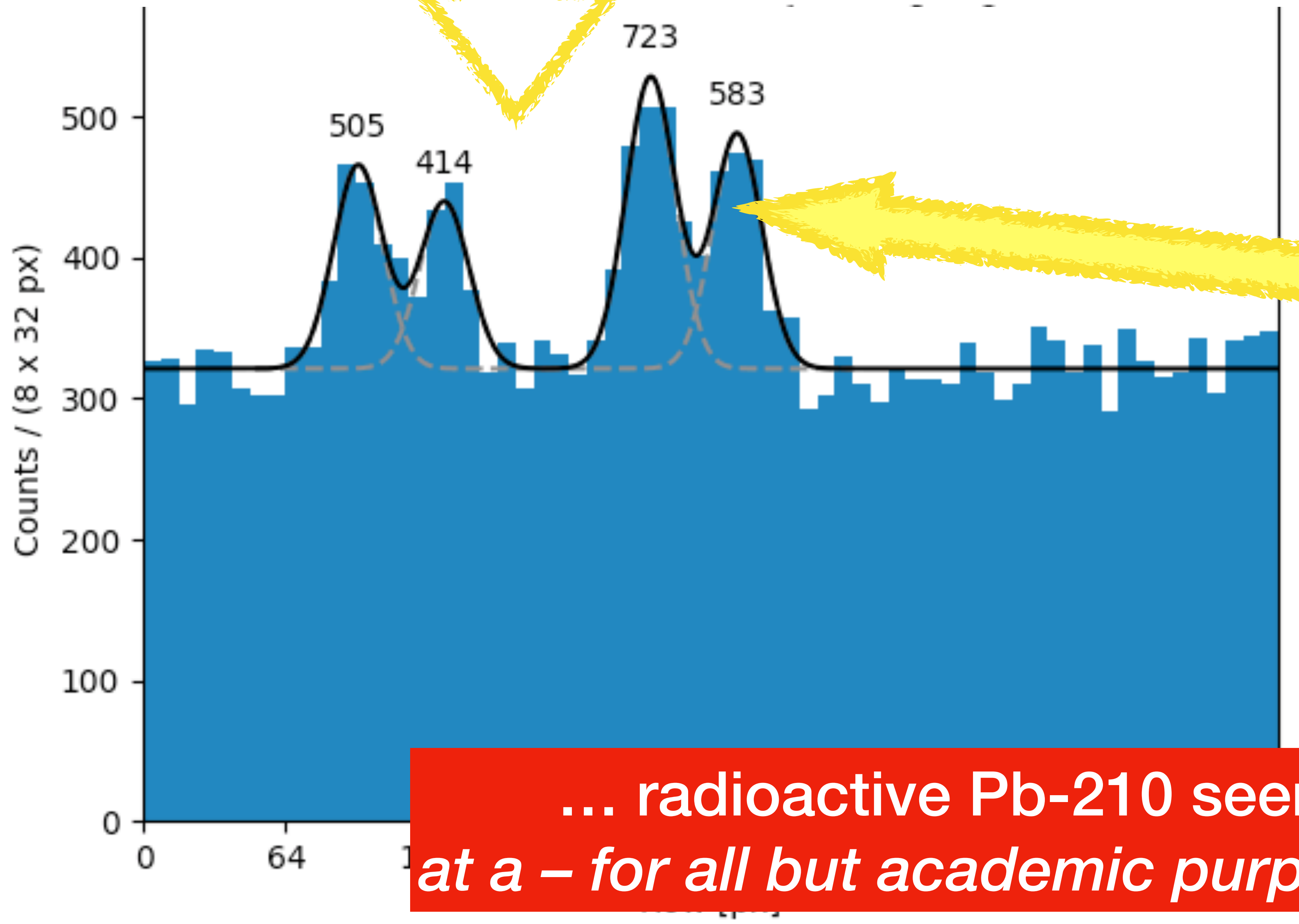
Insertion of first Outer Half-Barrel

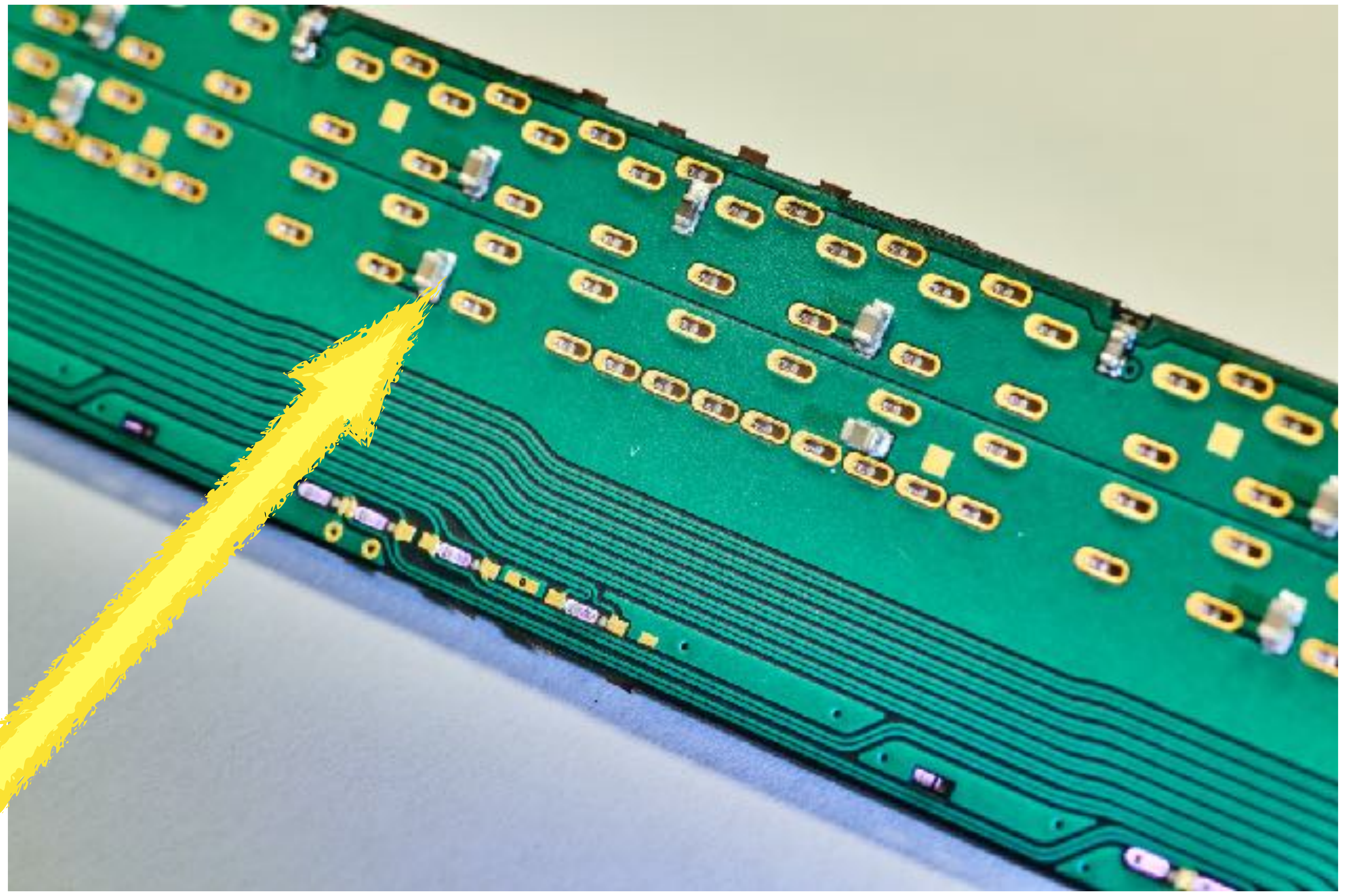

ALICE
Pb-Pb 5.36 TeV
LHC22s period
18th November 2022
16:52:47.893

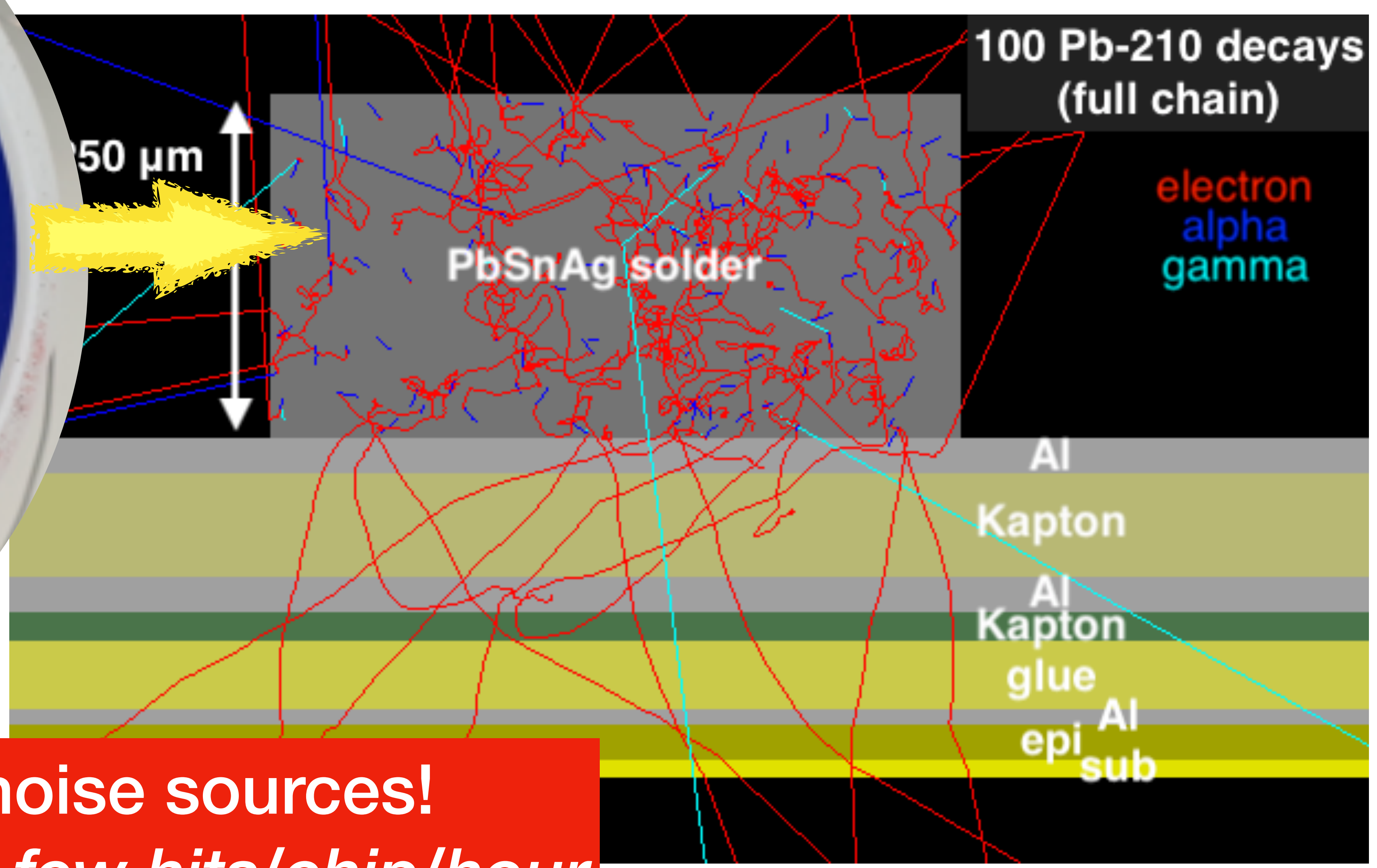
ITS2 performance

the noise floor is really *that* low







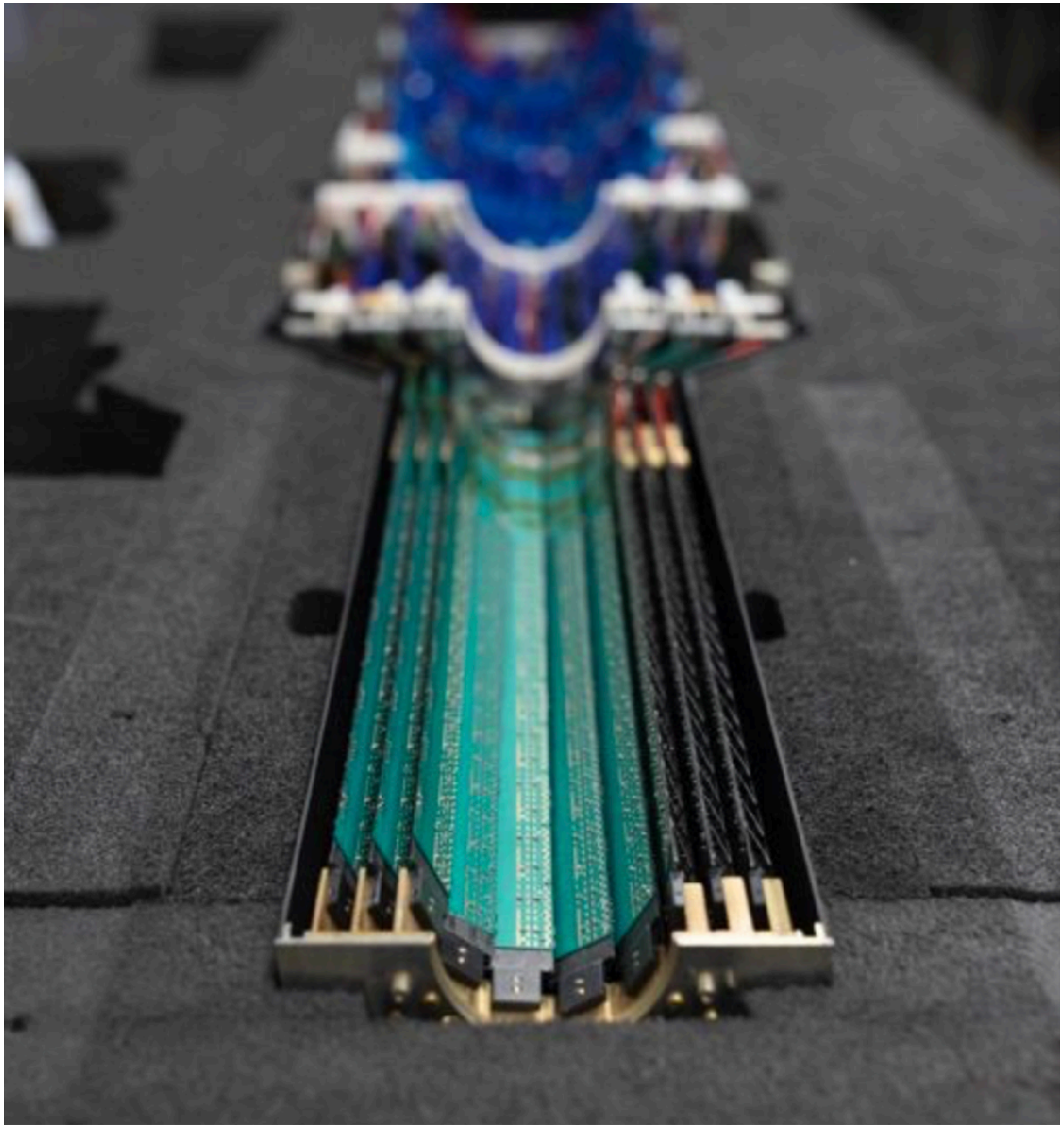


... radioactive Pb-210 seems to be one of the main real noise sources!

at a – for all but academic purposes – negligible rate of totals few hits/chip/hour

Offspring

sPHENIX



- Copy of ALICE ITS2 Inner Barrel
- Installed and taking data

Reaching full depletion

process variants

Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Excellent co-operation with foundry!

Fully depleted epitaxial layer
Charge collection time < 1 ns
Operational up to 10^{15} 1 MeV n_{eq}/cm^2

[doi:10.1016/j.nima.2017.07.046]

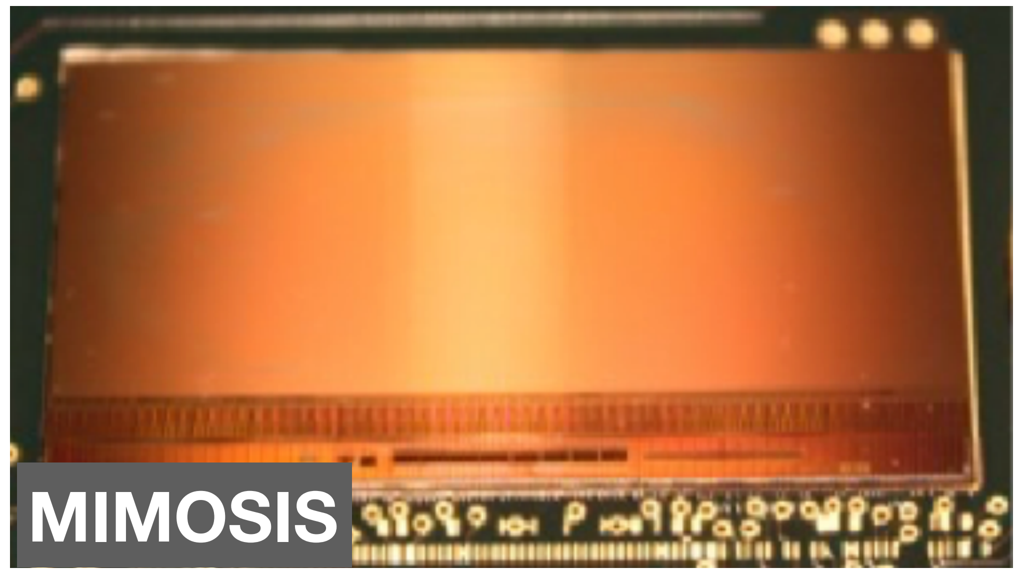
[doi:10.1088/1748-0221/14/05/C05013]

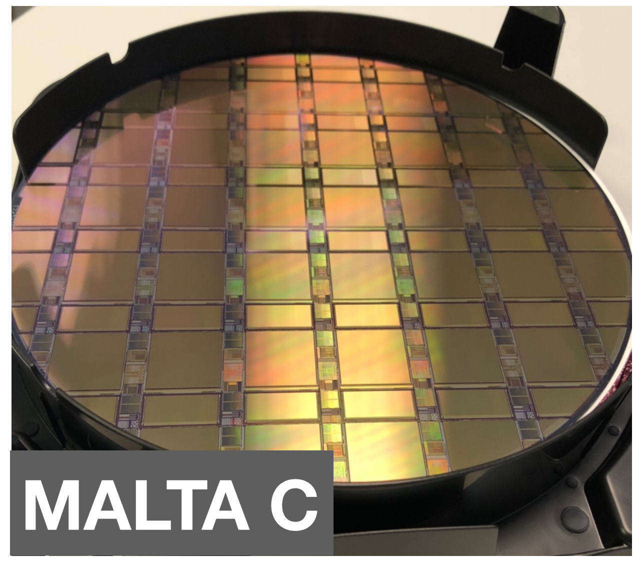
- Process modification as side activity of ALICE R&D
- Further optimised within ATLAS R&D
- Full depletion: faster charge collection, higher radiation hardness

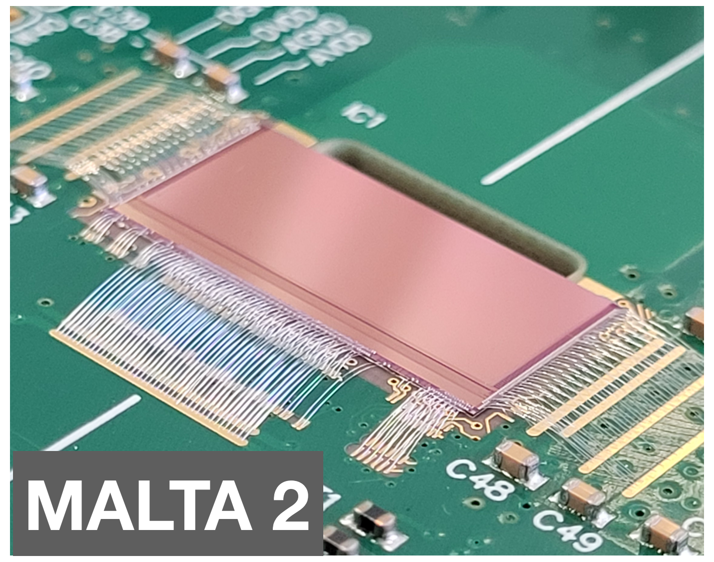
Families of more developments

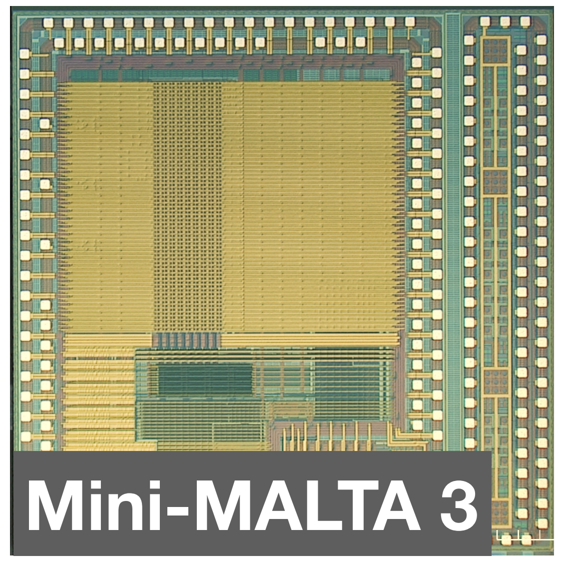
selection

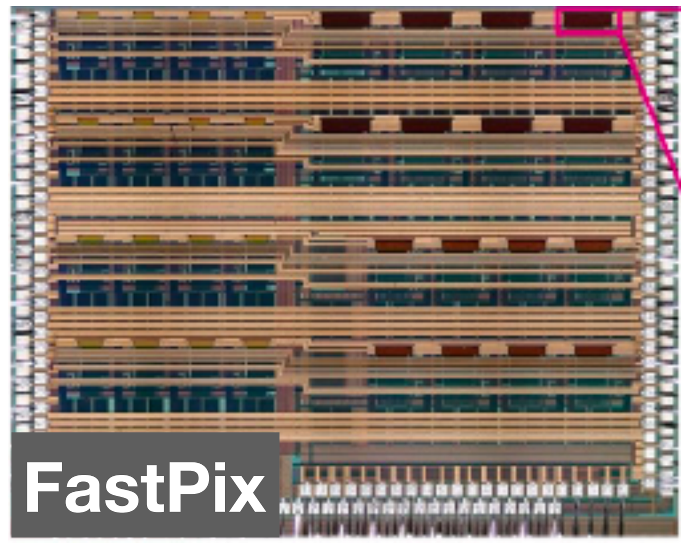
- CLICTD, MALTA, Fastpix, MIMOSIS, OBELIX, CEPC chips
  - 180 nm TJ (and similar) with different optimisations and applications

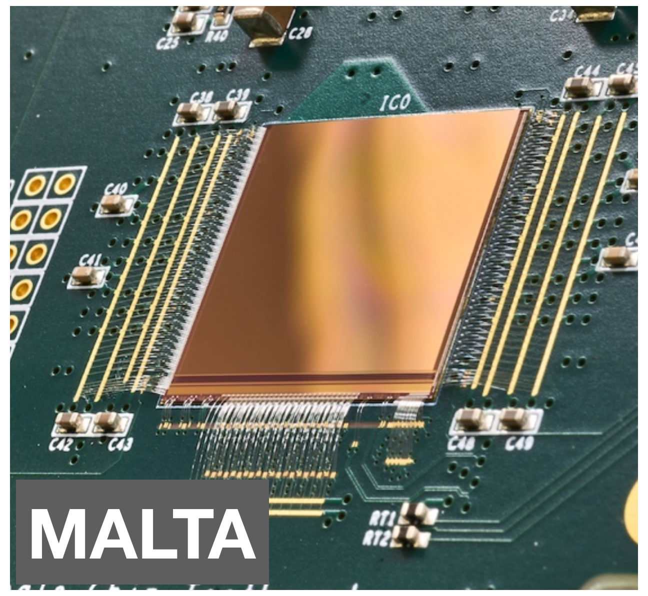


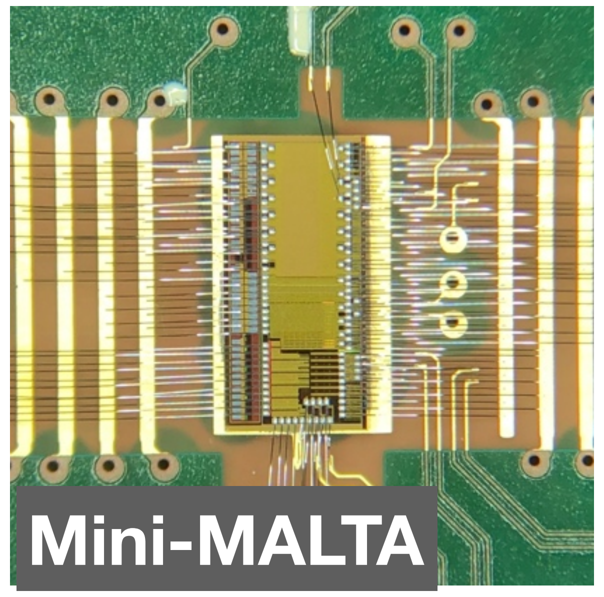




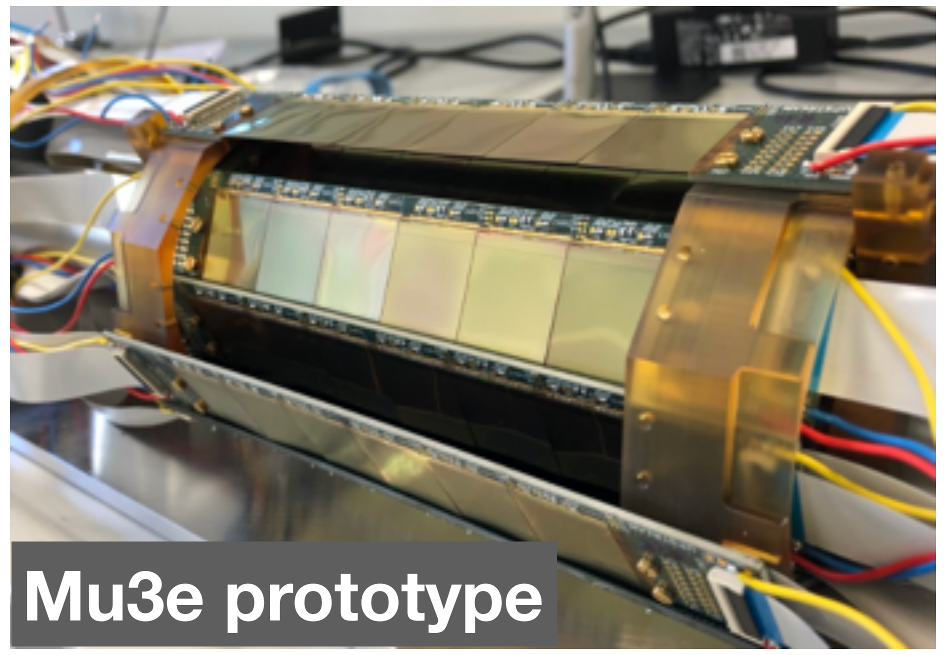


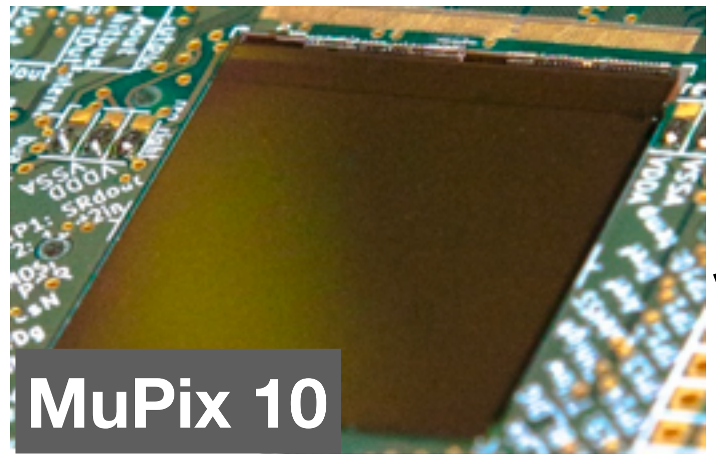


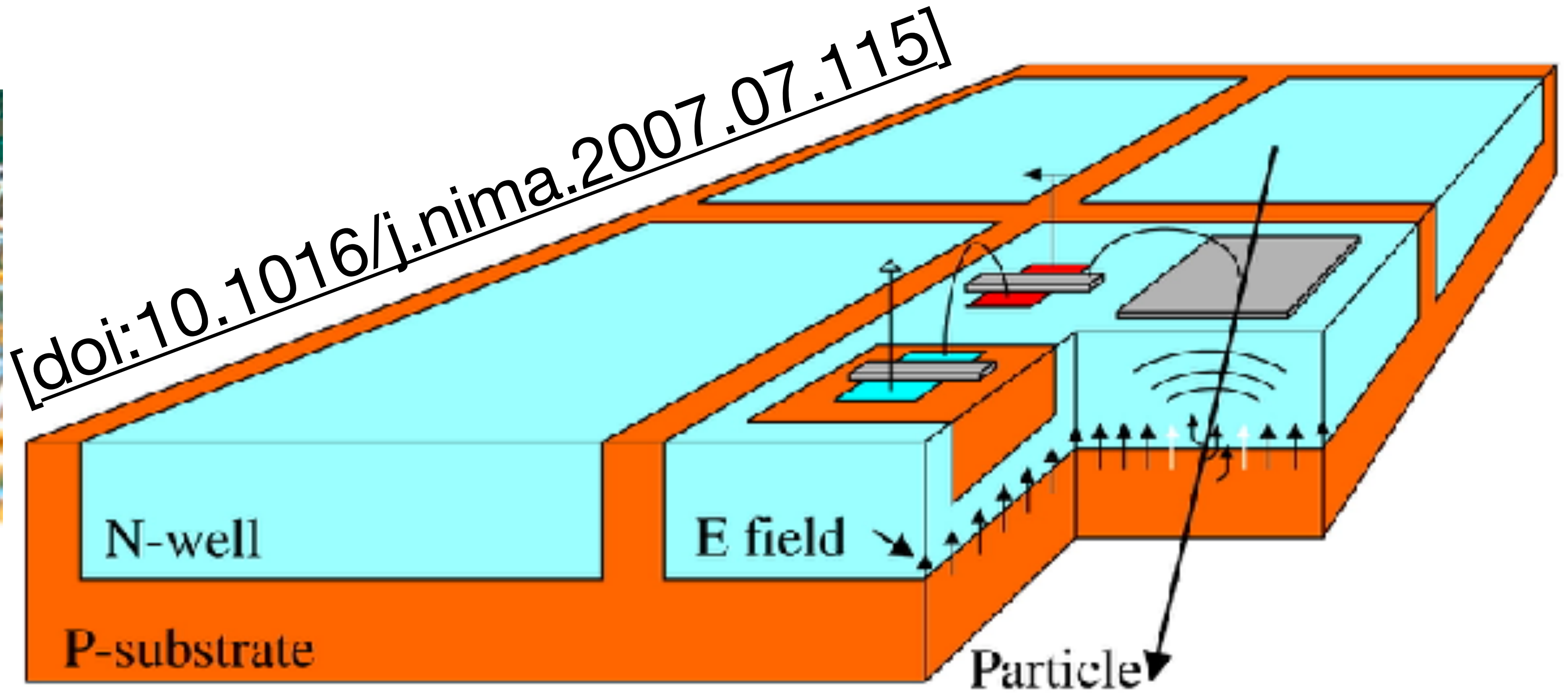




- HVMAPS: MuPix, TelePix, ATLASPix
  - different approach: large collection well in which the electronics sits







- SOI: isolation layer to separate electronics

The number of developments is increasing quickly!

Current future

Next technology node: 180 nm → 65 nm

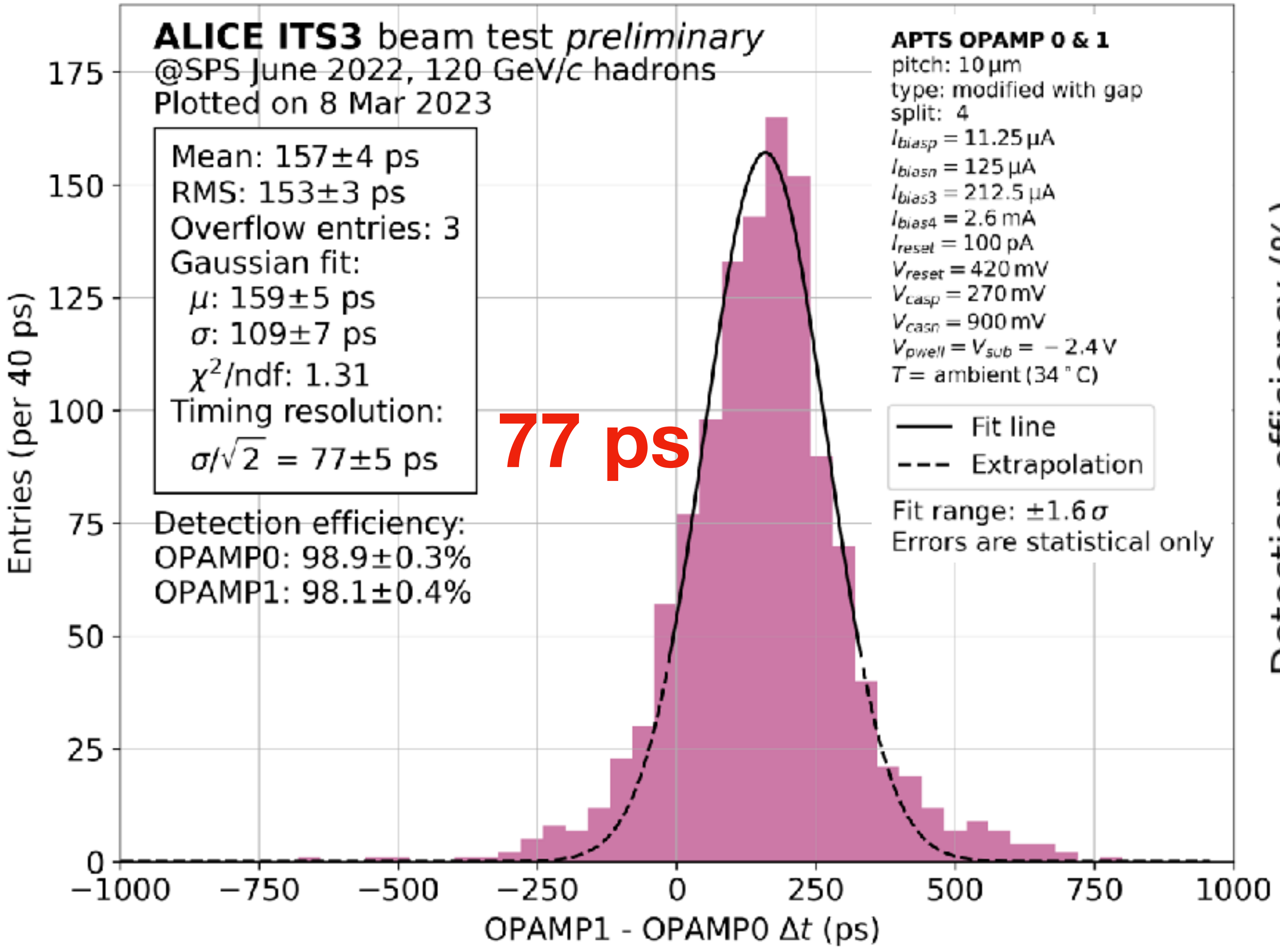
qualifying the TPSCo 65 nm CMOS Imaging Technology

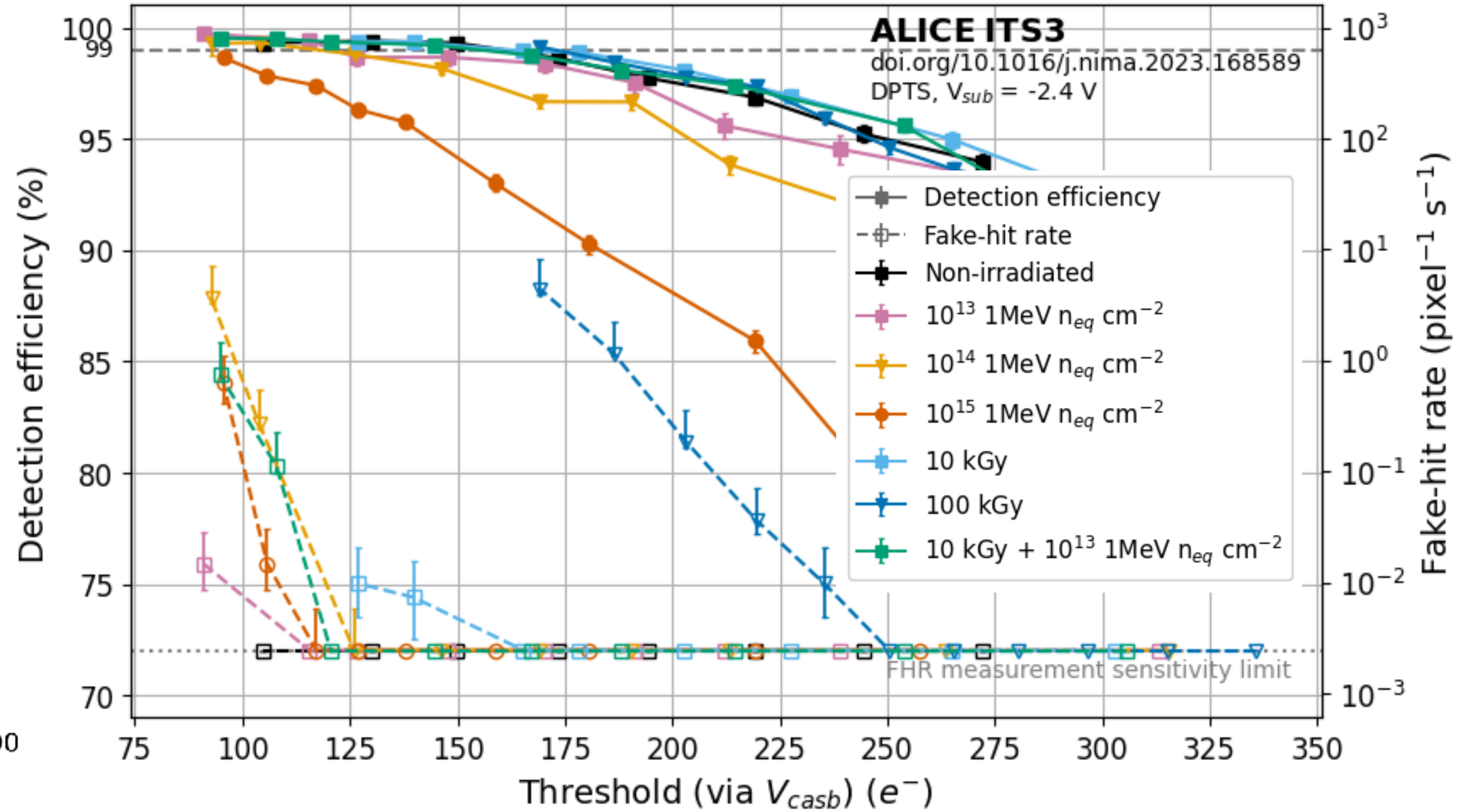
- **Key benefits:**
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - larger wafers
- ALICE ITS3 together with CERN EP R&D
  - leverages on experience with 180 nm (ALPIDE)
  - excellent links to foundry
- Comprehensive *first* submission: **55** prototypes
  - works excellently!

Qualification of 65 nm CMOS

2 selected results

- Intrinsic time resolutions of 77 ps for 10 µm pixels
- >99% detection efficiency even after 10^{15} NIEL for 15 µm pixels at room temperature



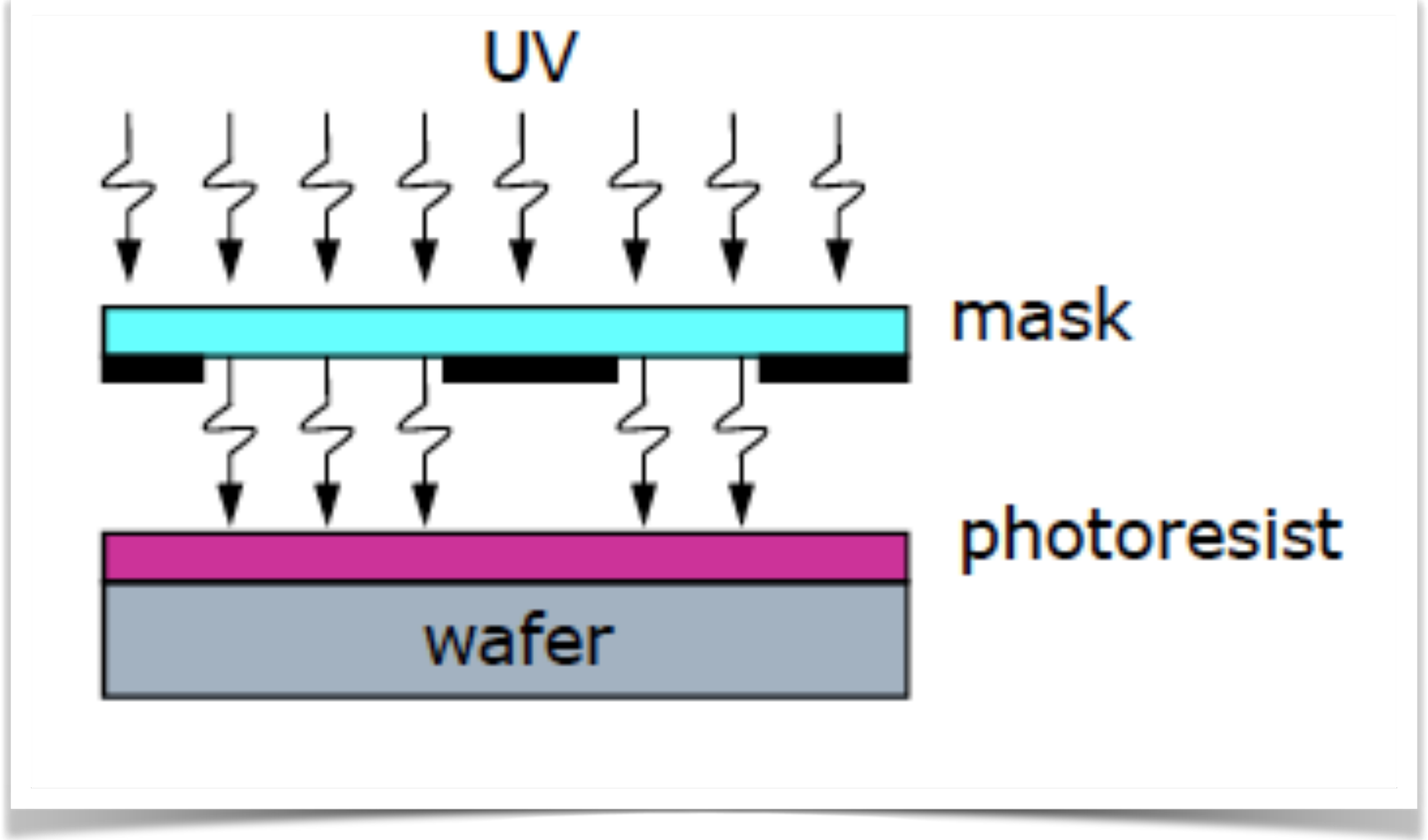


Excellent performances of the 65 nm technology have been established experimentally

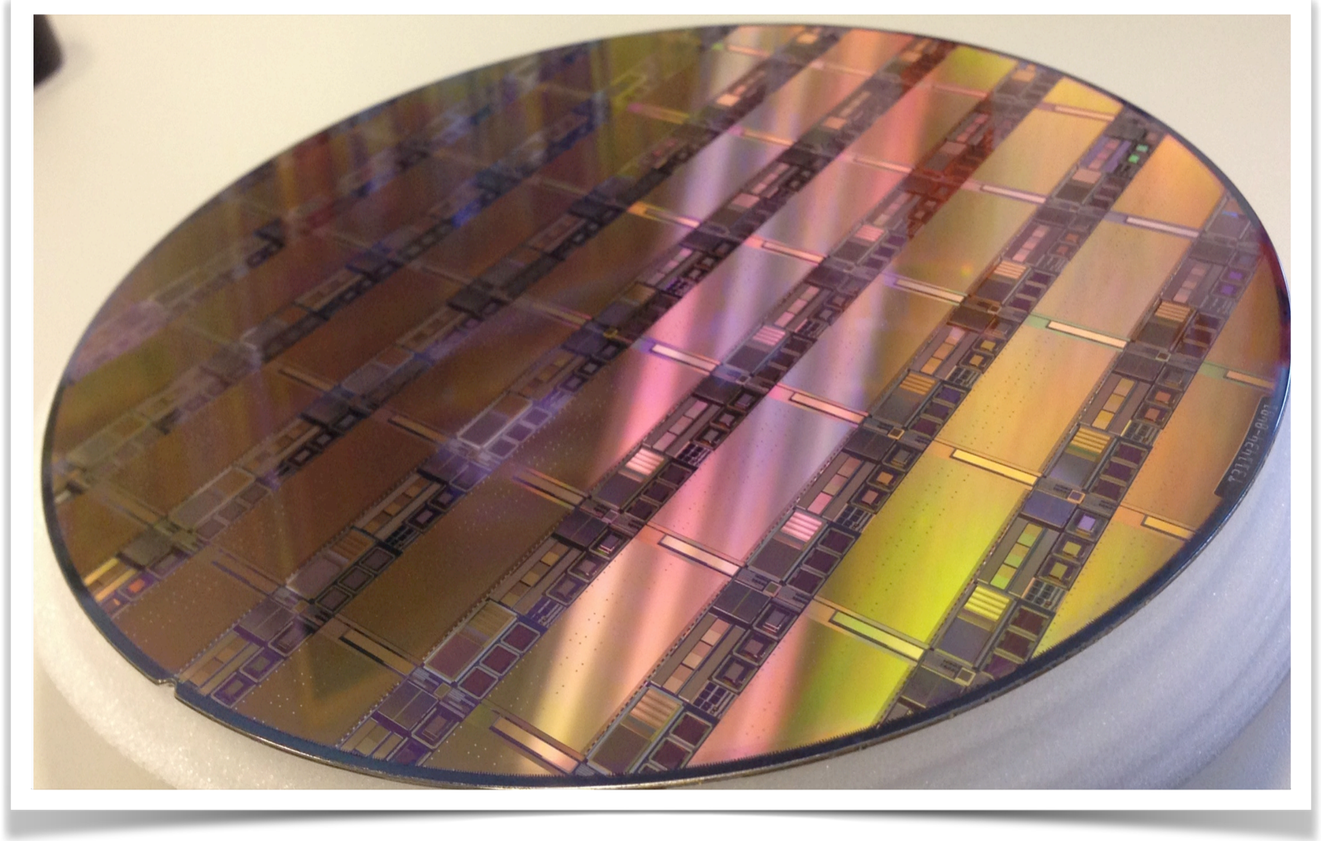
Wafer-scale sensors: stitching

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board

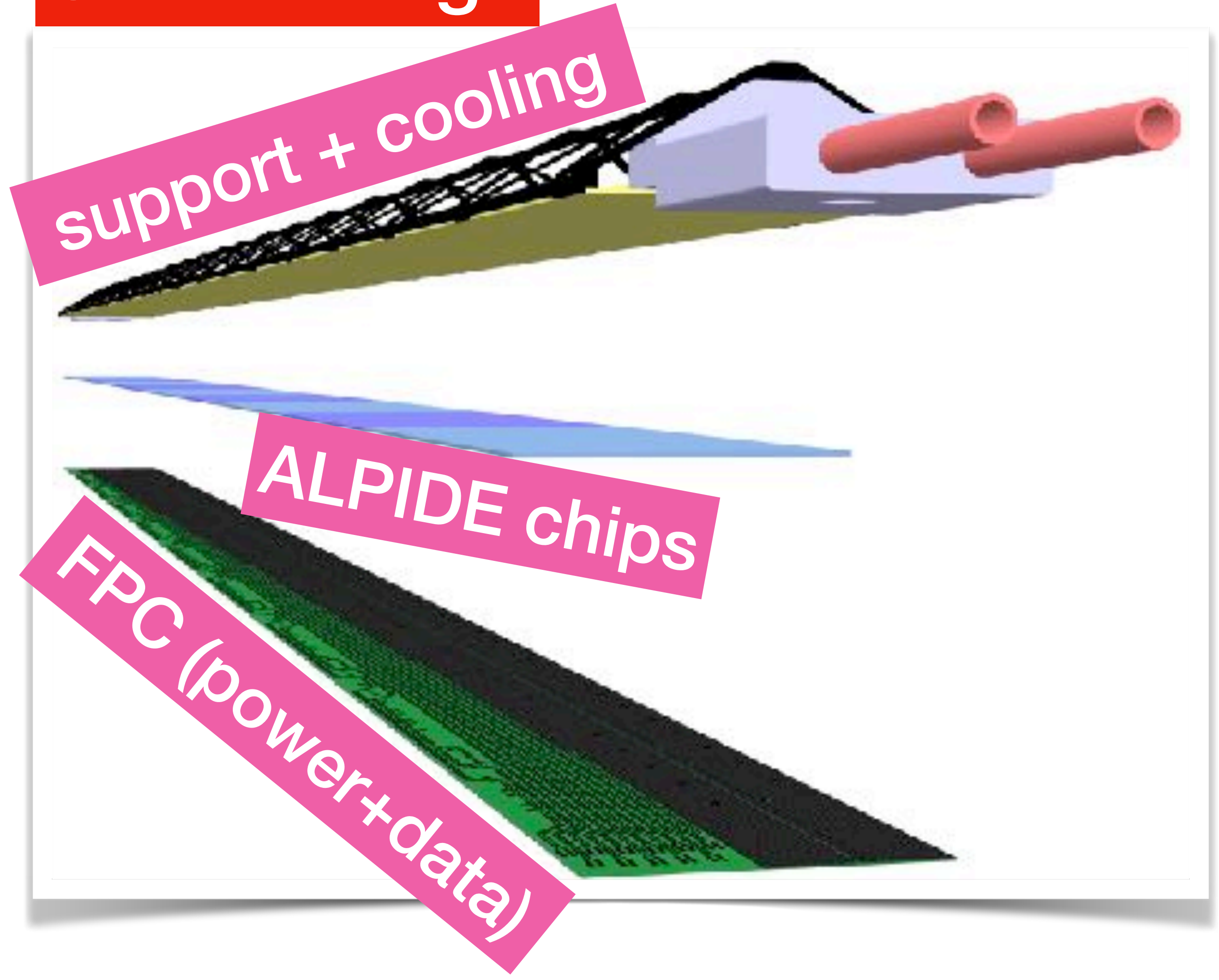
Principle of photolithography



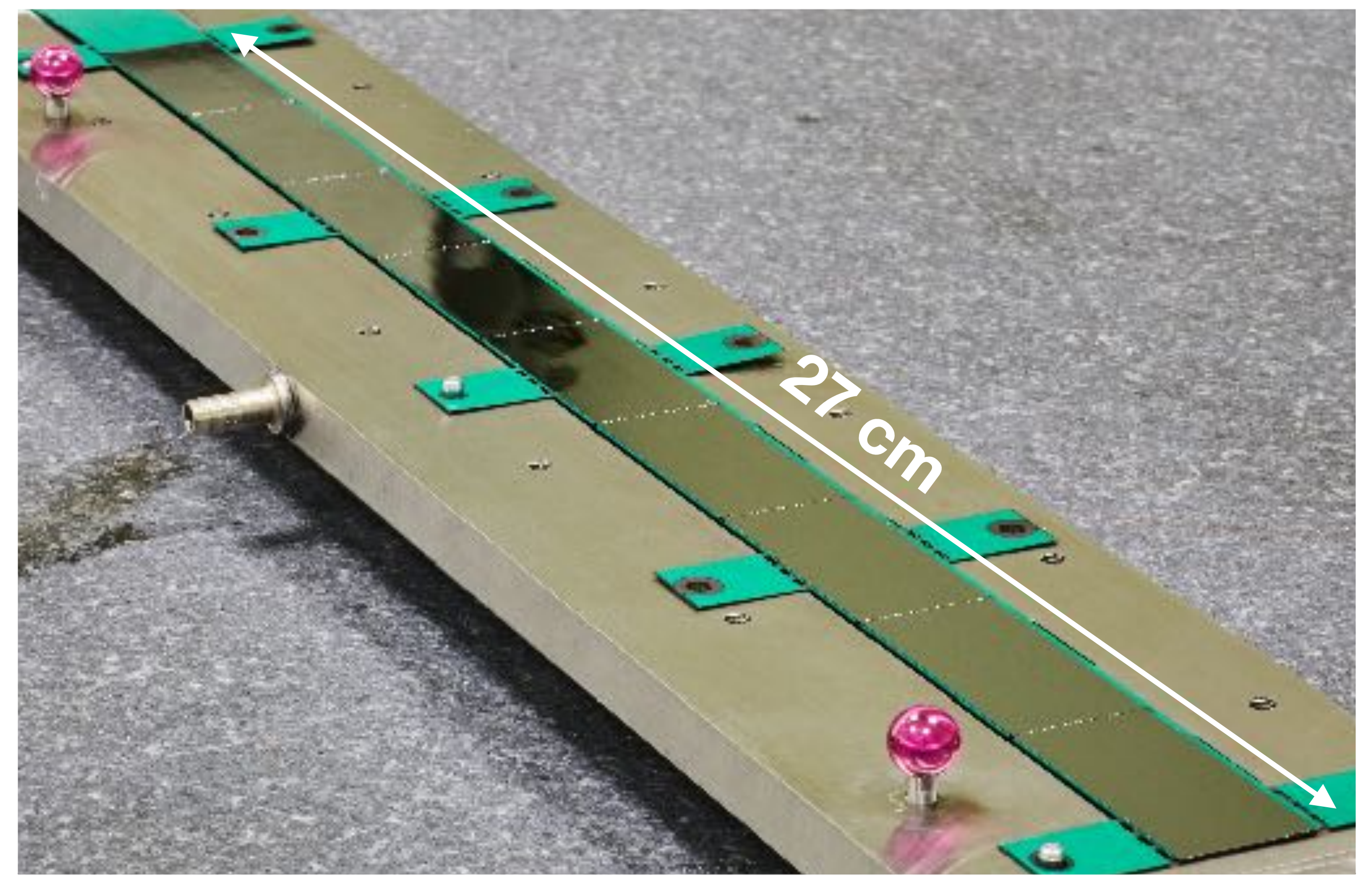
200 mm ALPIDE prototype wafer



Stave design



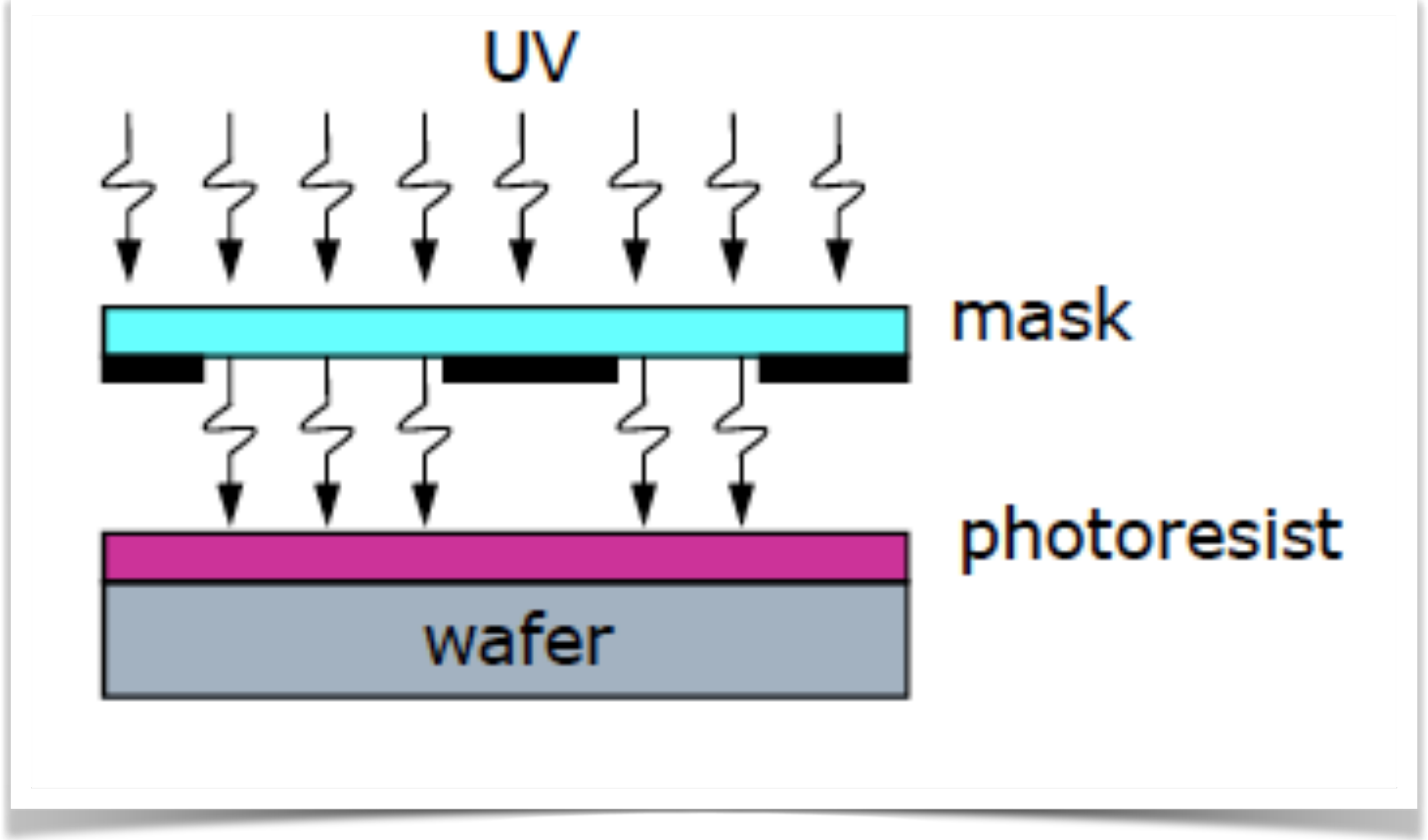
FPC + chips



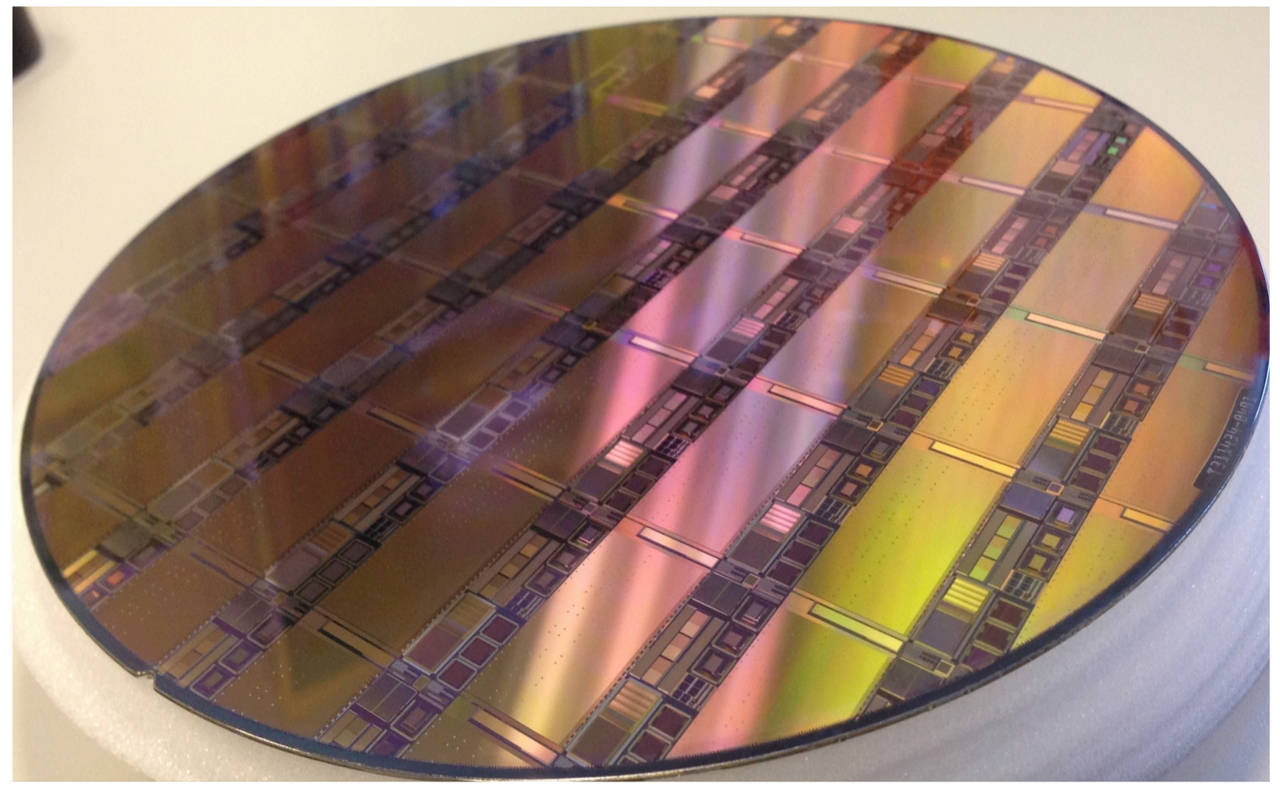
Wafer-scale sensors: stitching

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board
- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a chip to equip a full half-layer
  - *requires dedicated chip design*

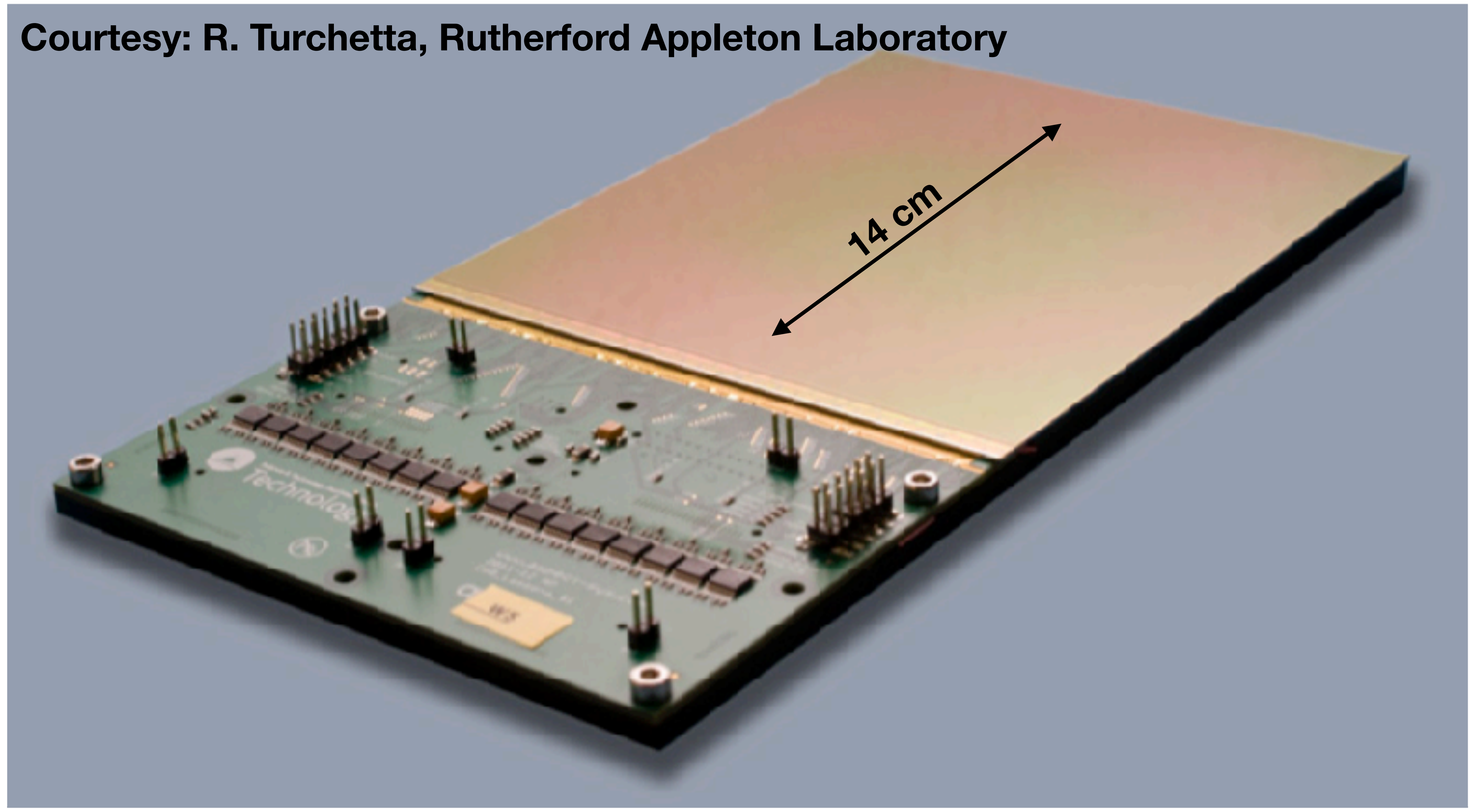
Principle of photolithography



200 mm ALPIDE prototype wafer



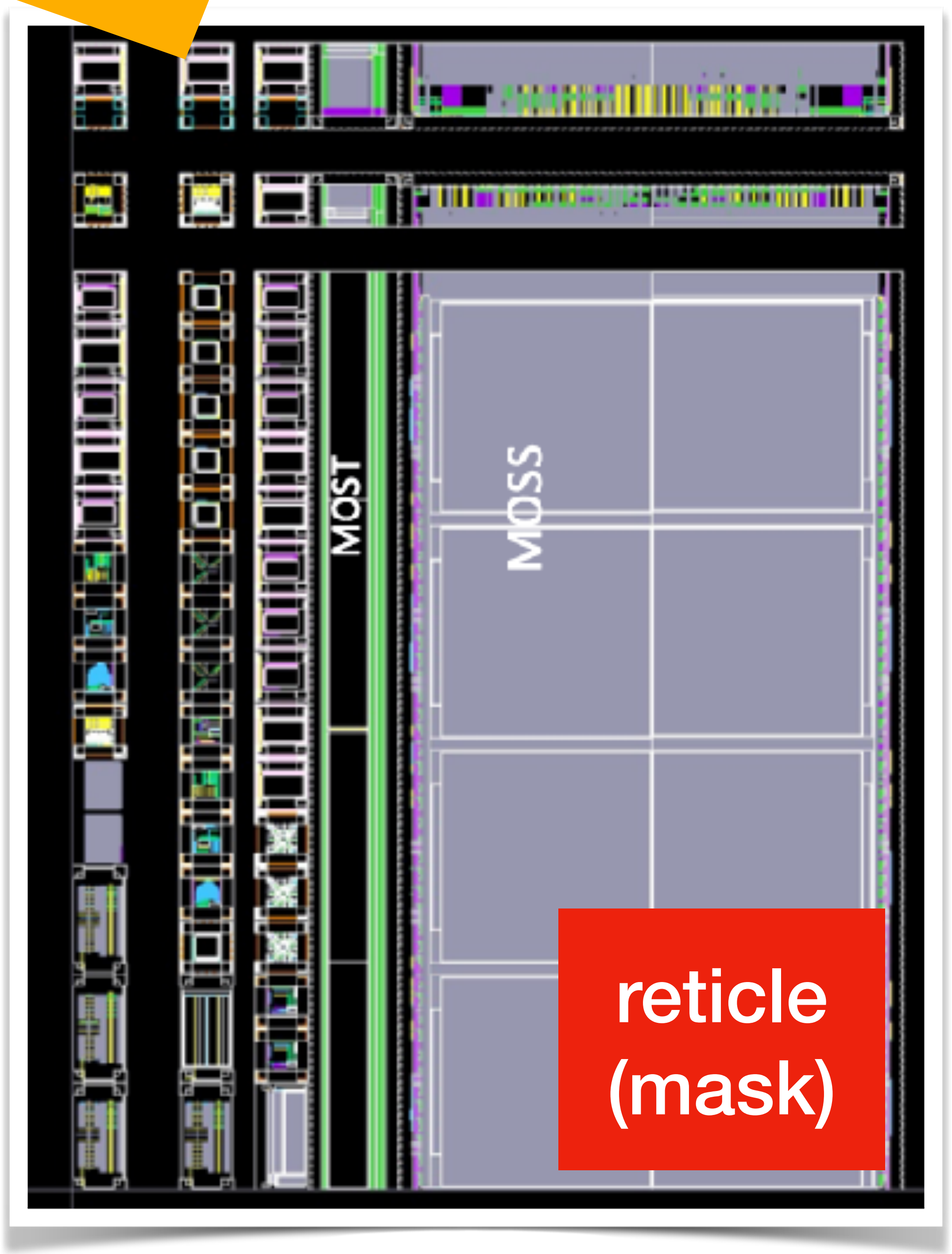
Wafer-scale sensor



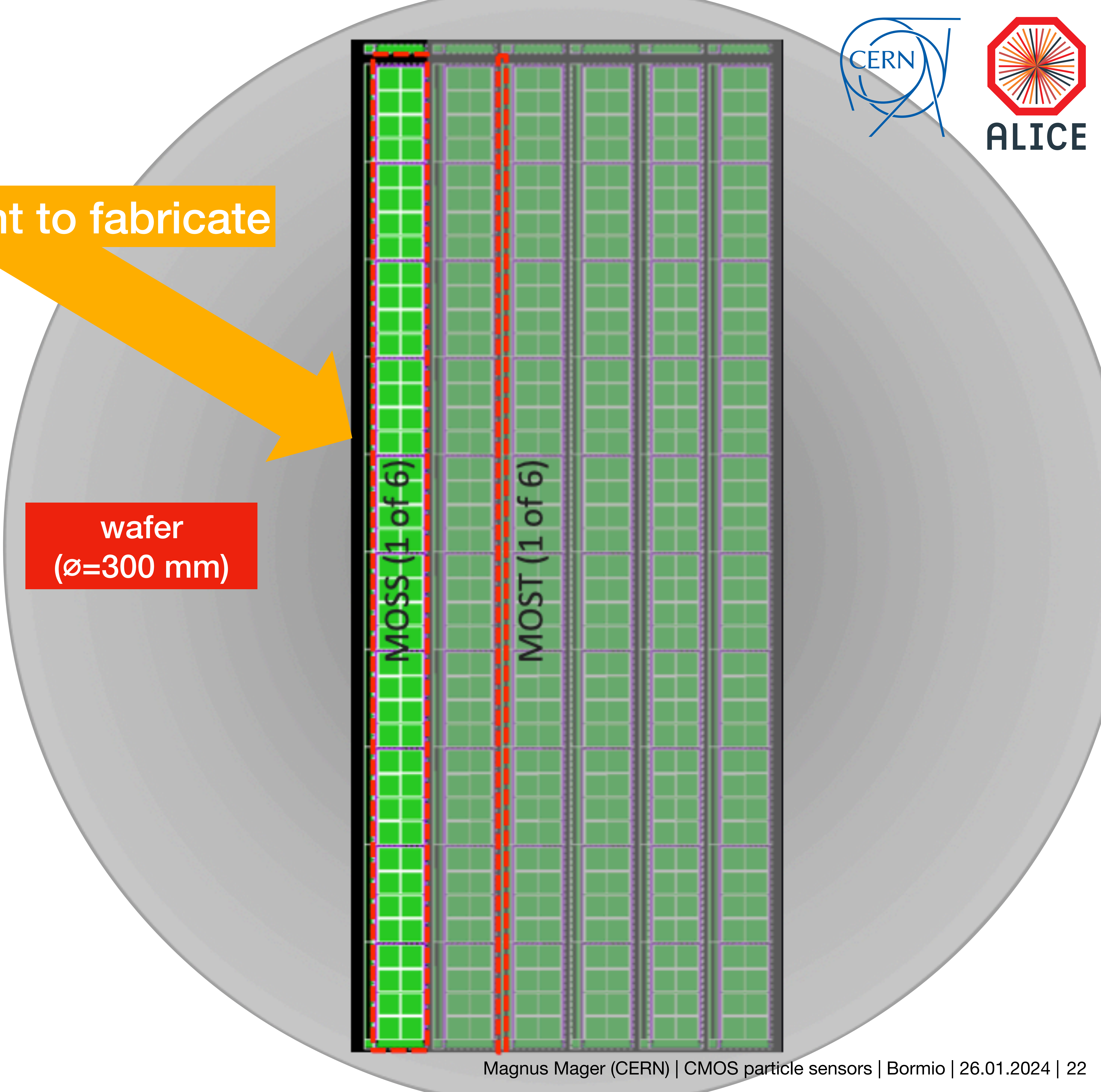
Stitching

simplified principle

what we "design"



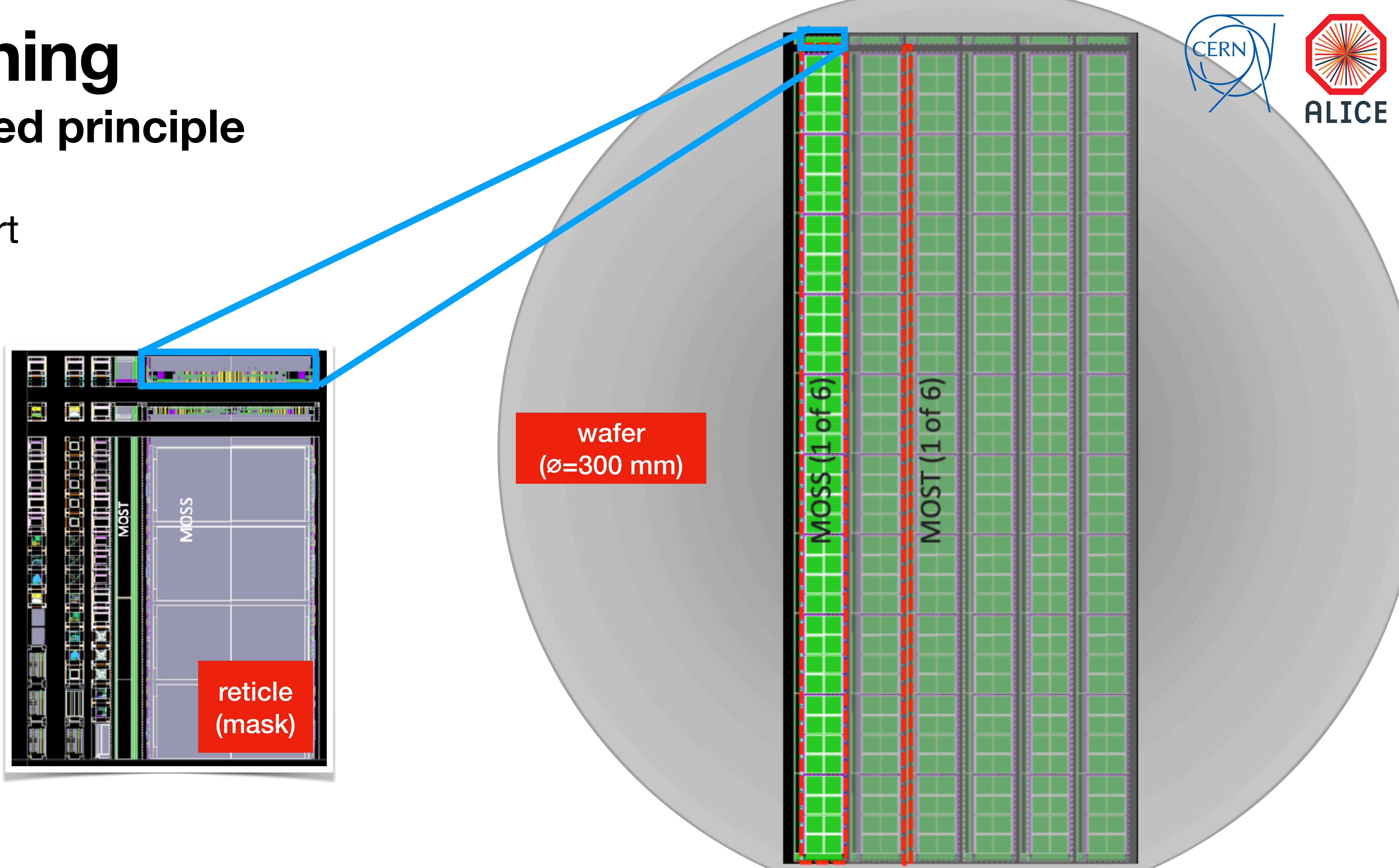
what we want to fabricate



Stitching

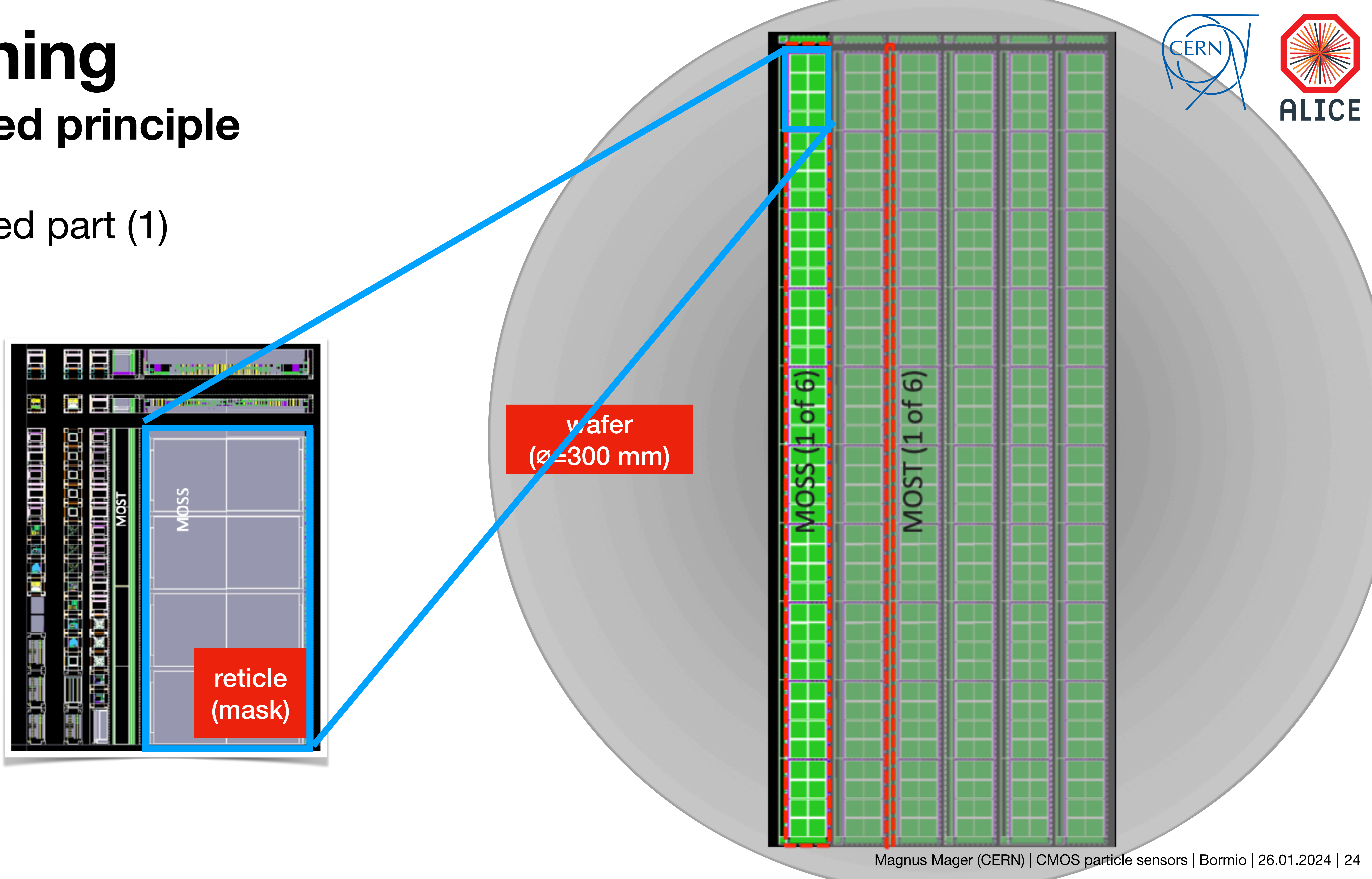
simplified principle

- top part



Stitching
simplified principle

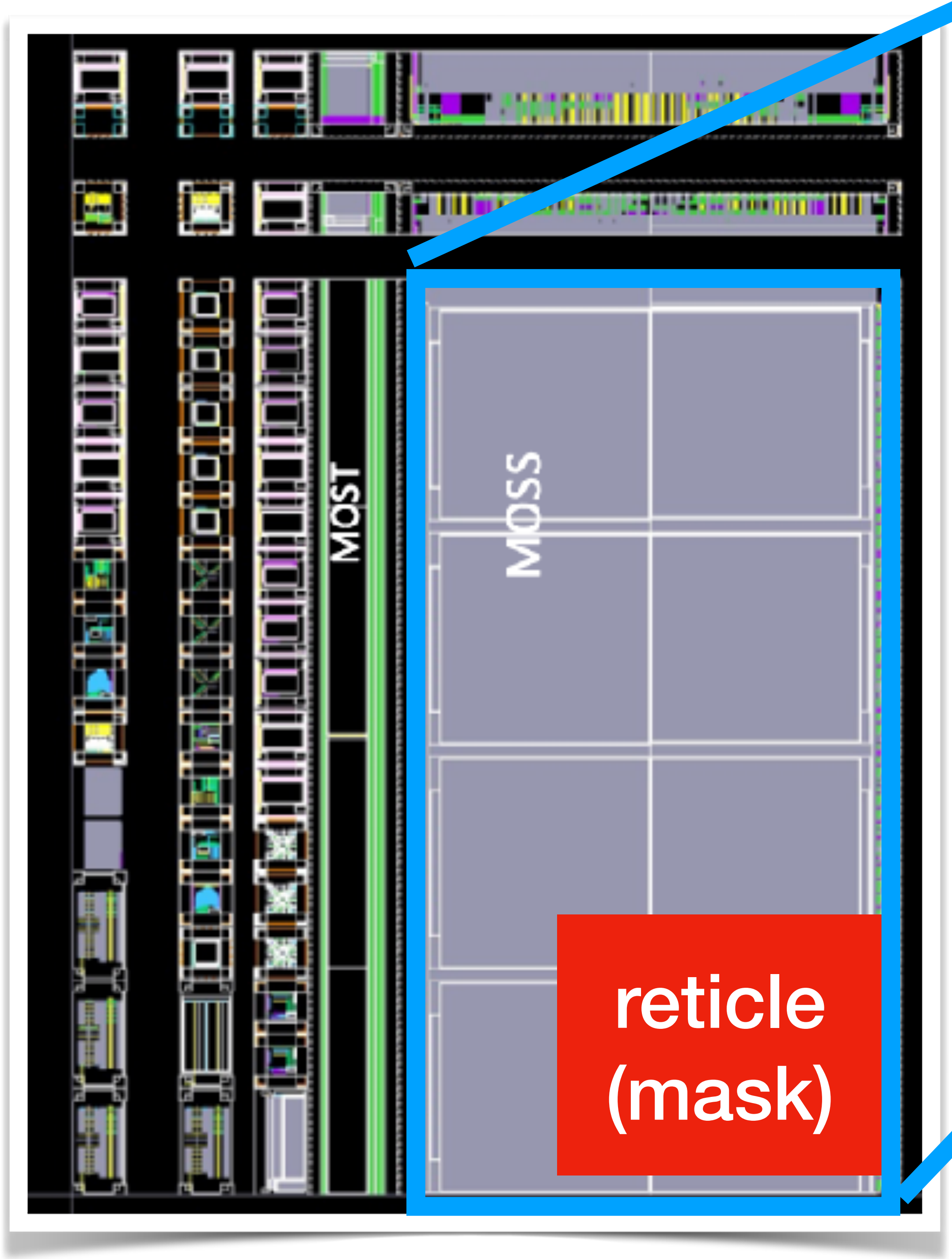
- repeated part (1)

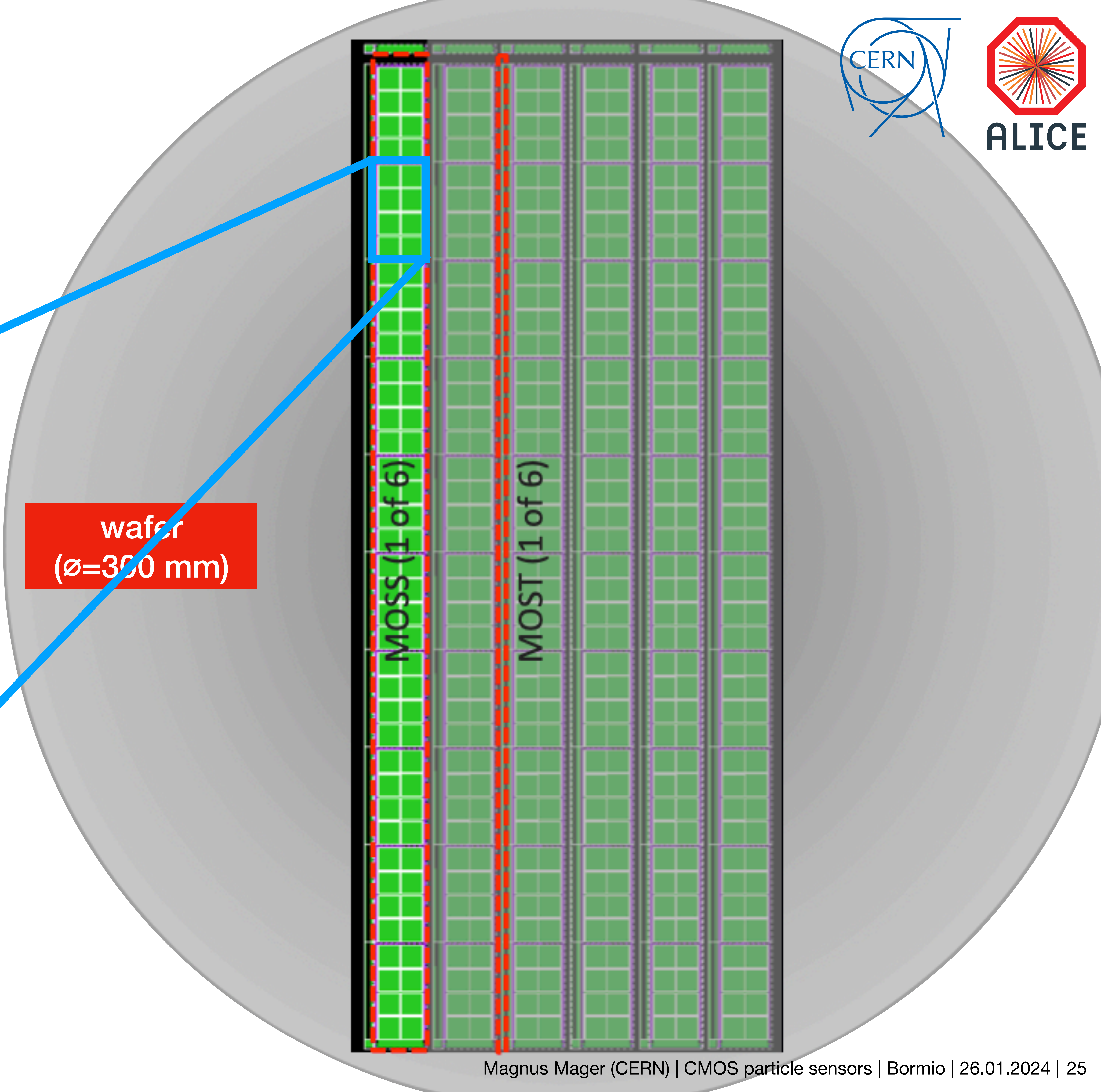


Stitching

simplified principle

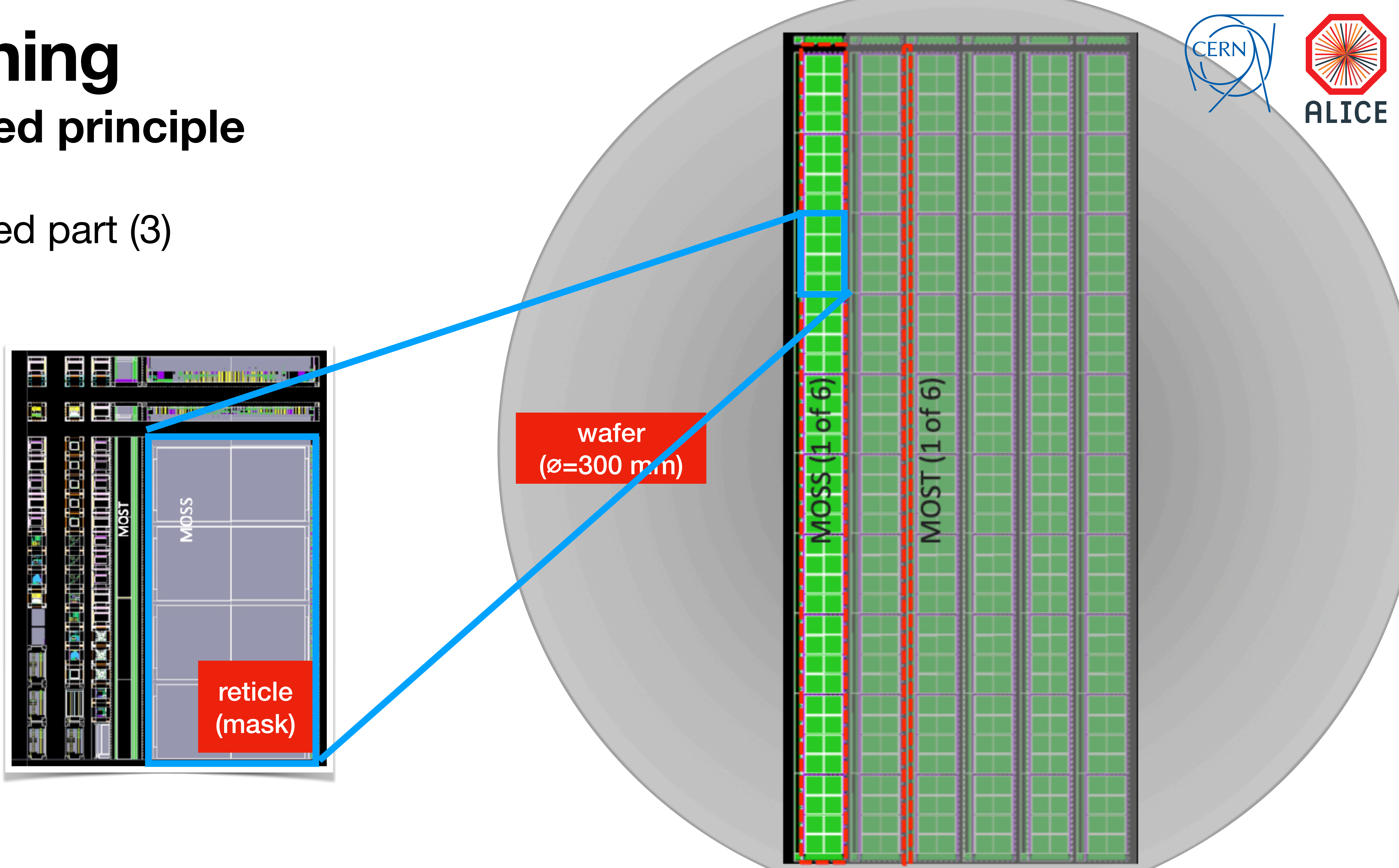
- repeated part (2)





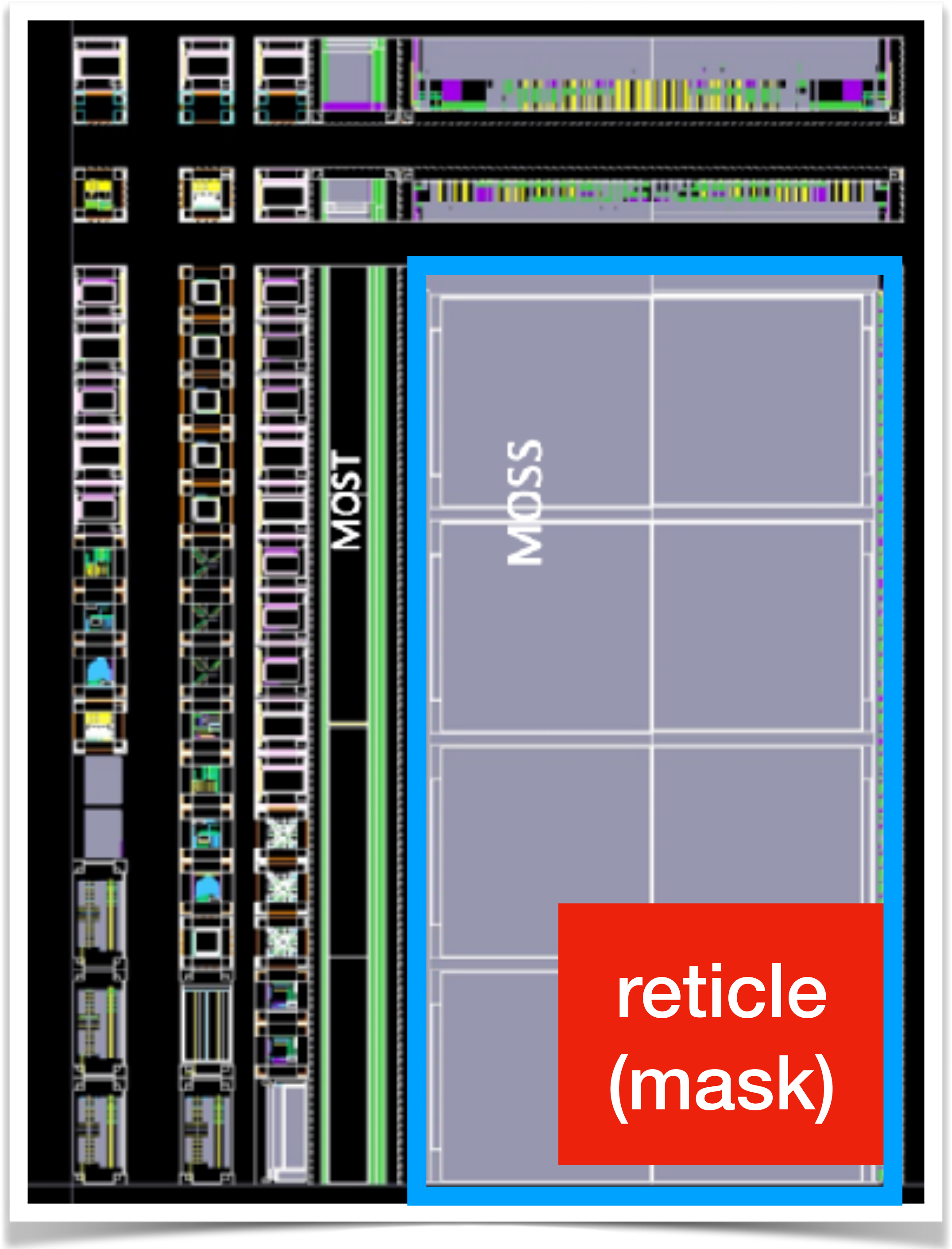
Stitching
simplified principle

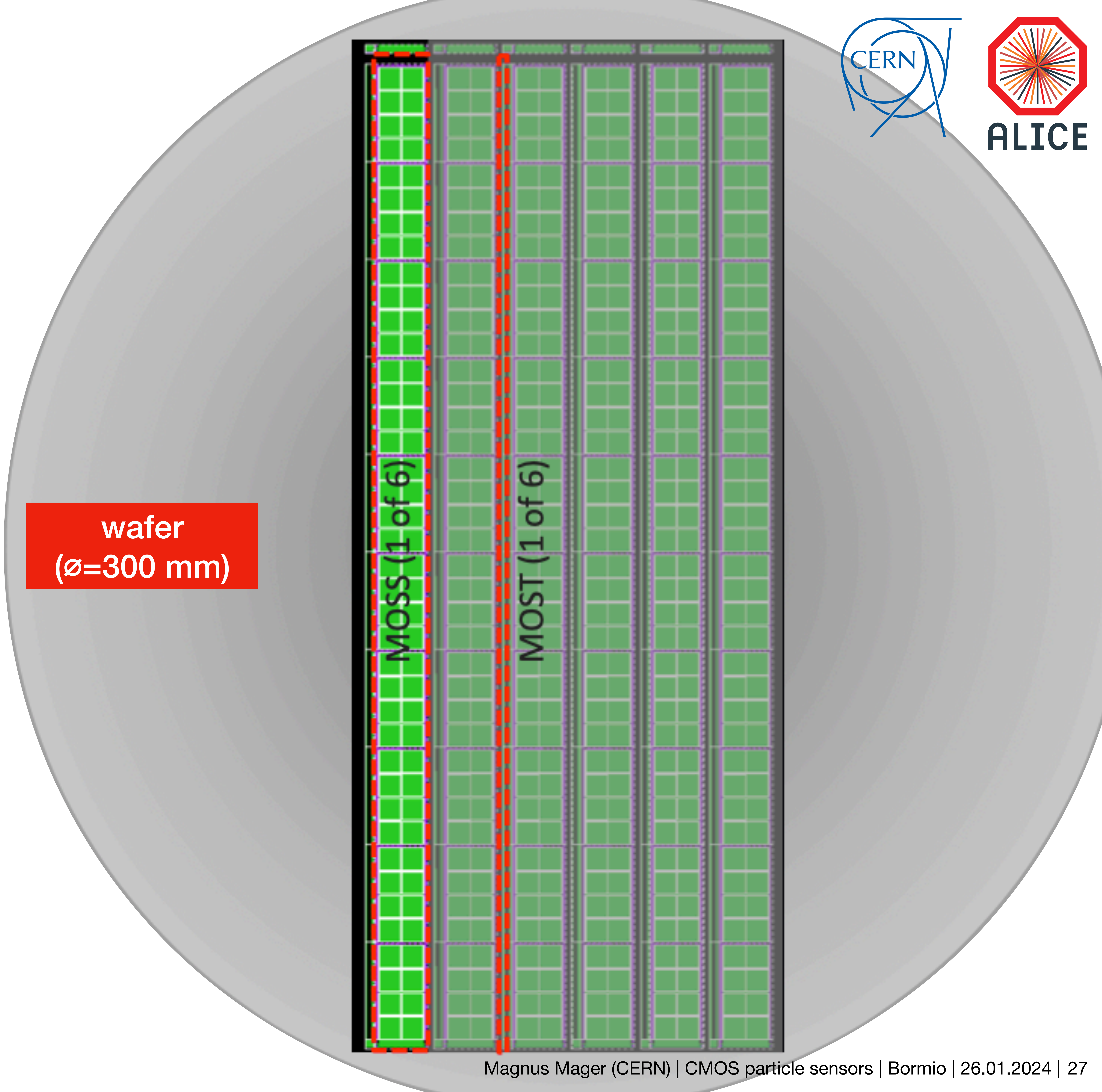
- repeated part (3)



Stitching
simplified principle

- final circuit is a concatenation of different parts of the masks





Chip development roadmap

status and plans

past

MLR1: first MAPS in TPSCo 65nm (2021)

- successfully qualified the 65nm process for particle detectors

present

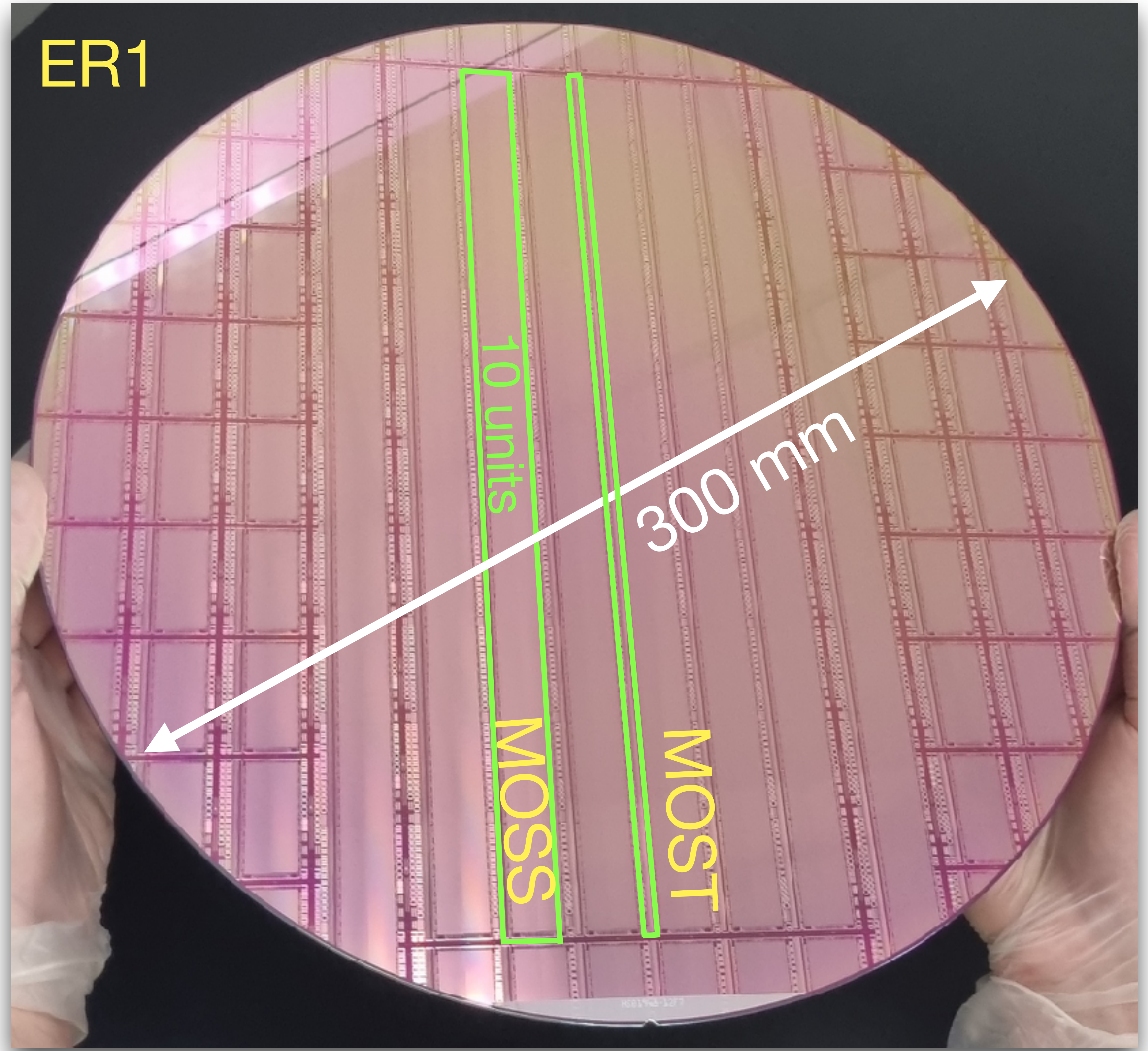
ER1: first stitched MAPS (2023)

- large design "exercise"
- "**MOSS**": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²): conservative design, different pitches
- "**MOST**": 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²): more dense design

future

ER2: first ITS3 sensor prototype (2024)

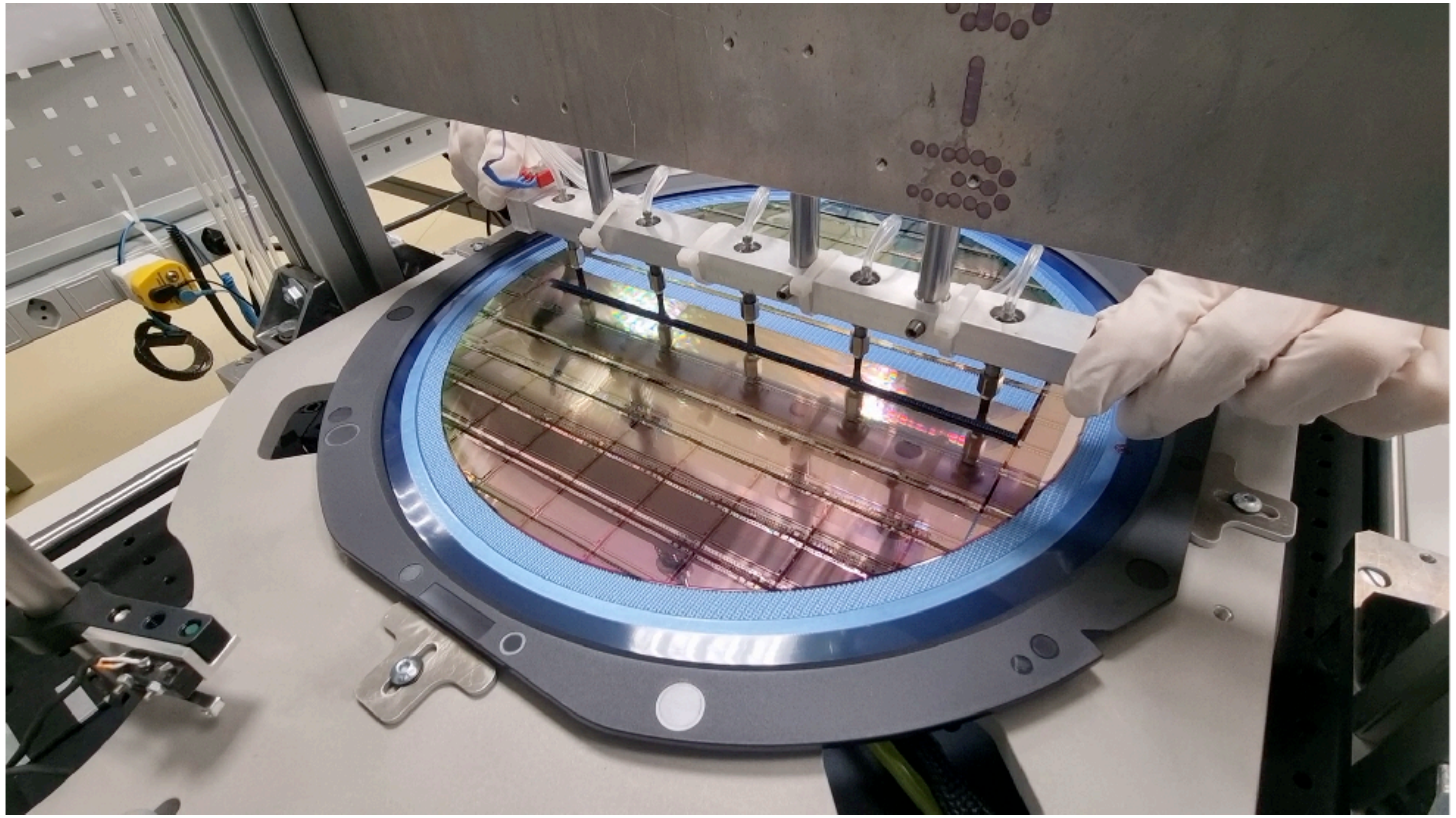
ER3: ITS3 sensor production (2025)

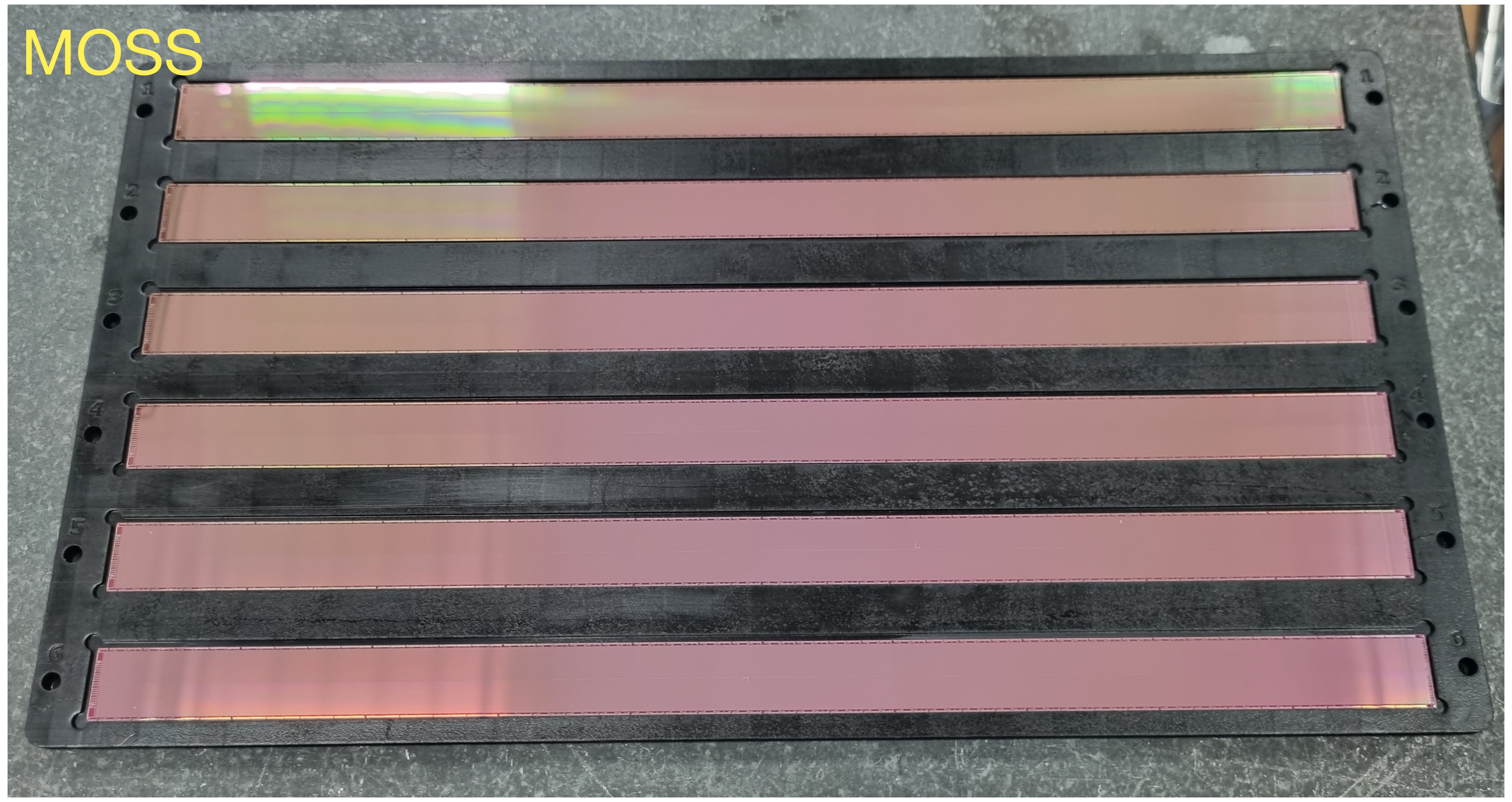


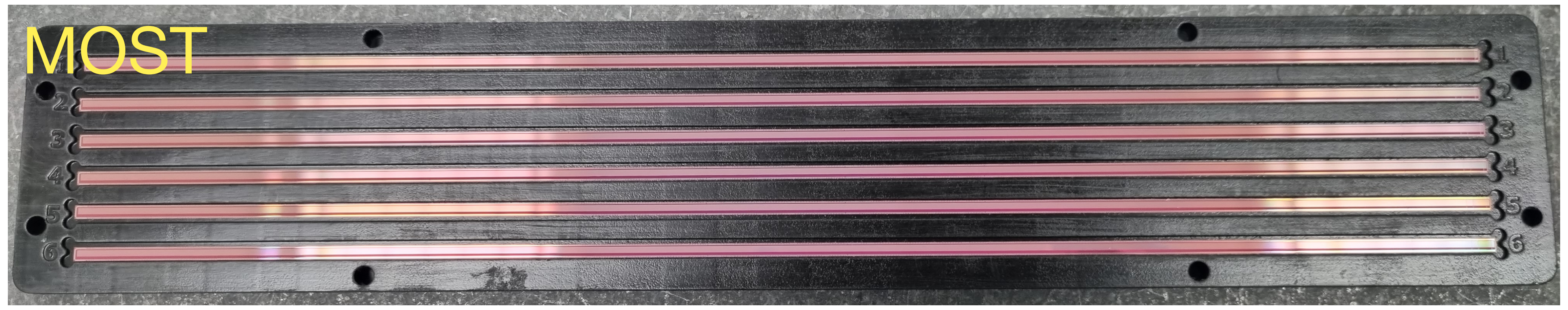
Prototypes: handling

ER1

- ER1 wafers are thinned down to 50 µm
- Tools to pick, handle and ship chips have been developed

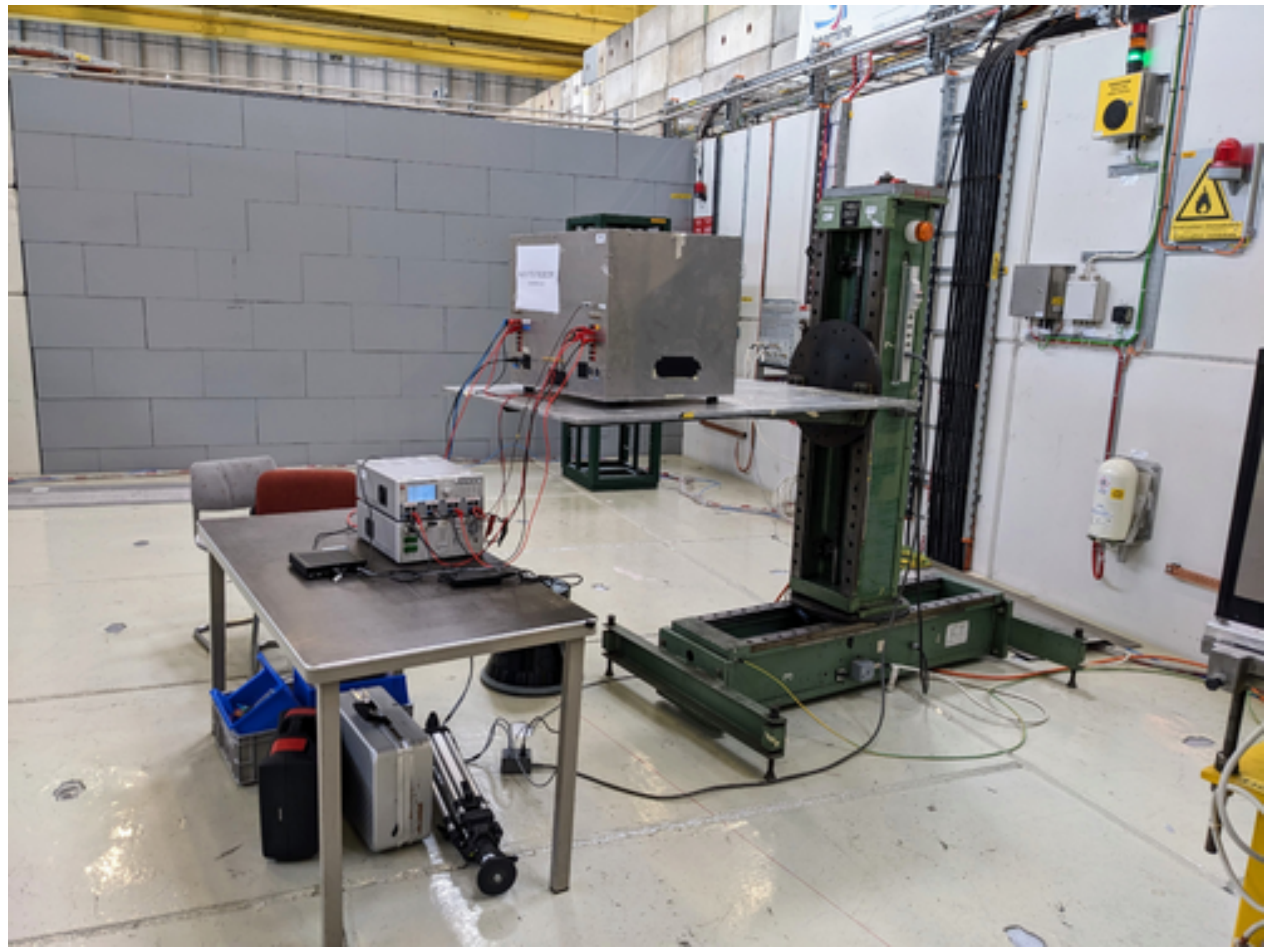




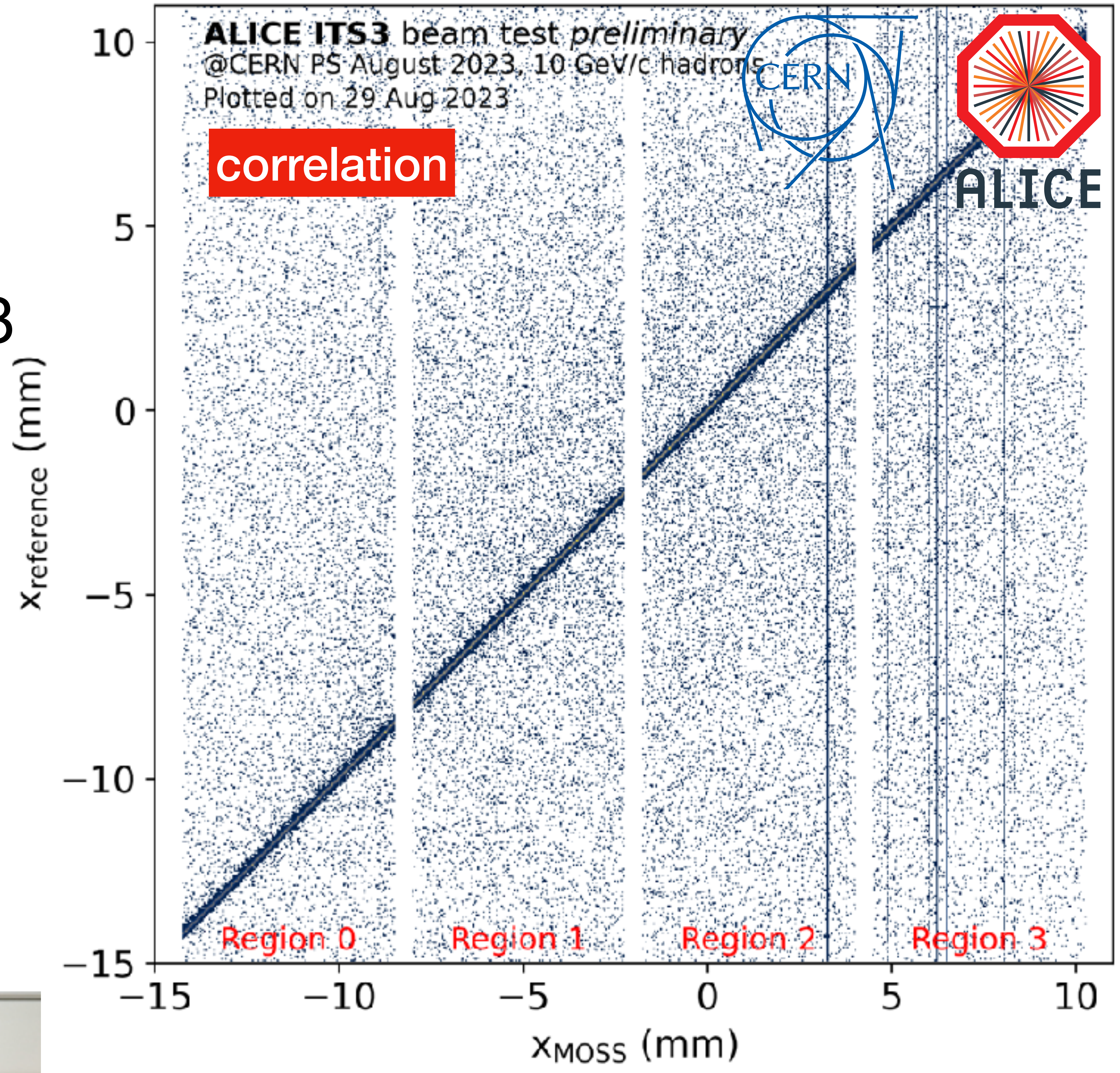


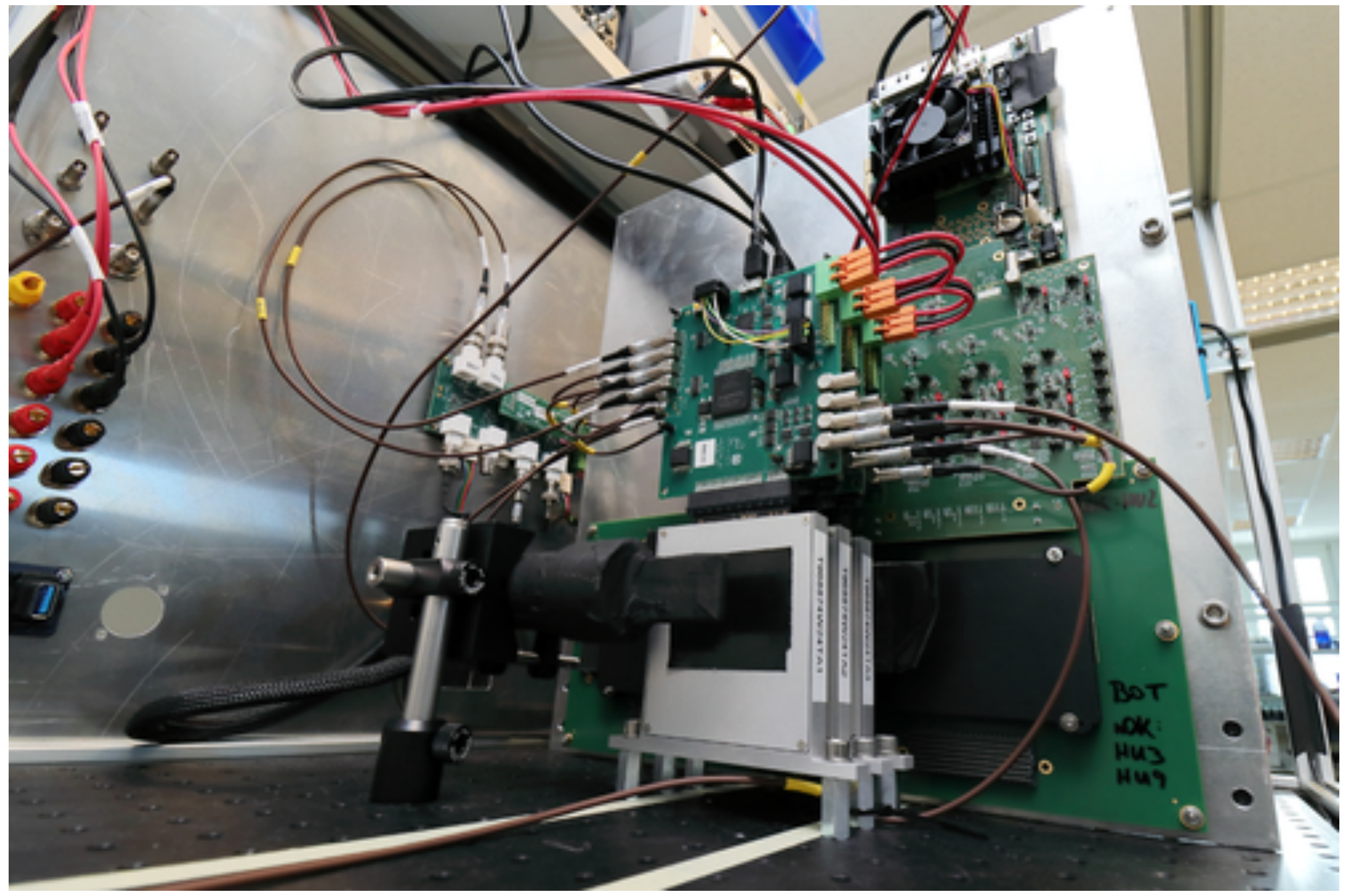
A set of dedicated tools have been developed — handling is under control

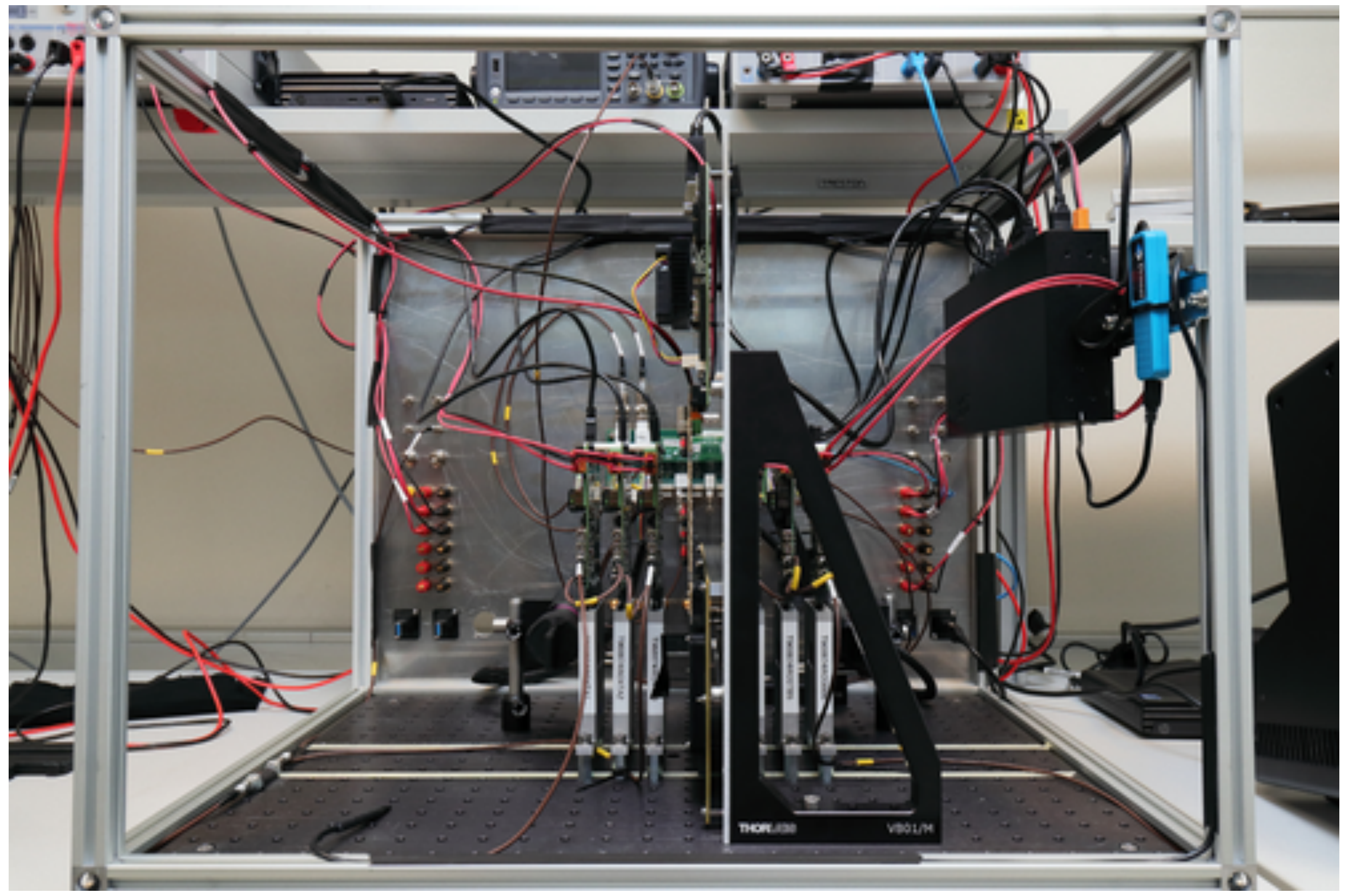
MOSS test beams

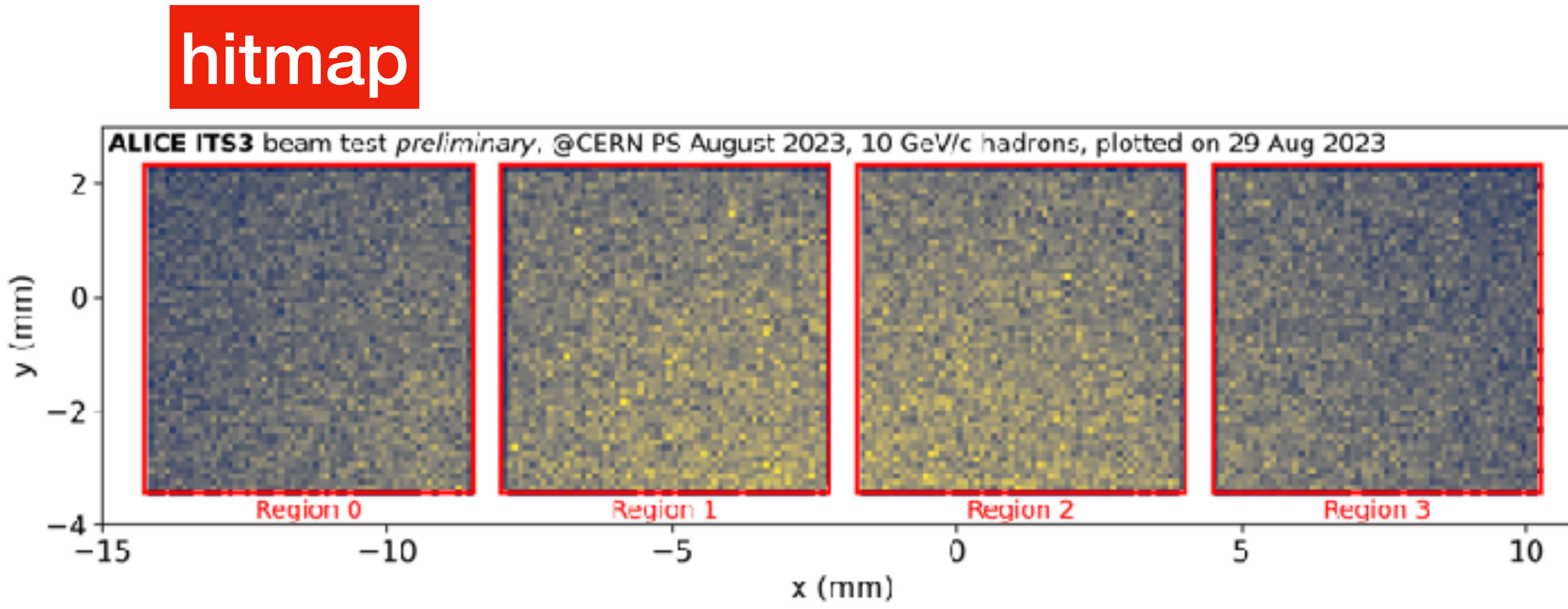


- Several campaigns in 2023
- Works out of the box
- Parameters still to be optimised and data to be analysed in more detail
- But very encouraging result!



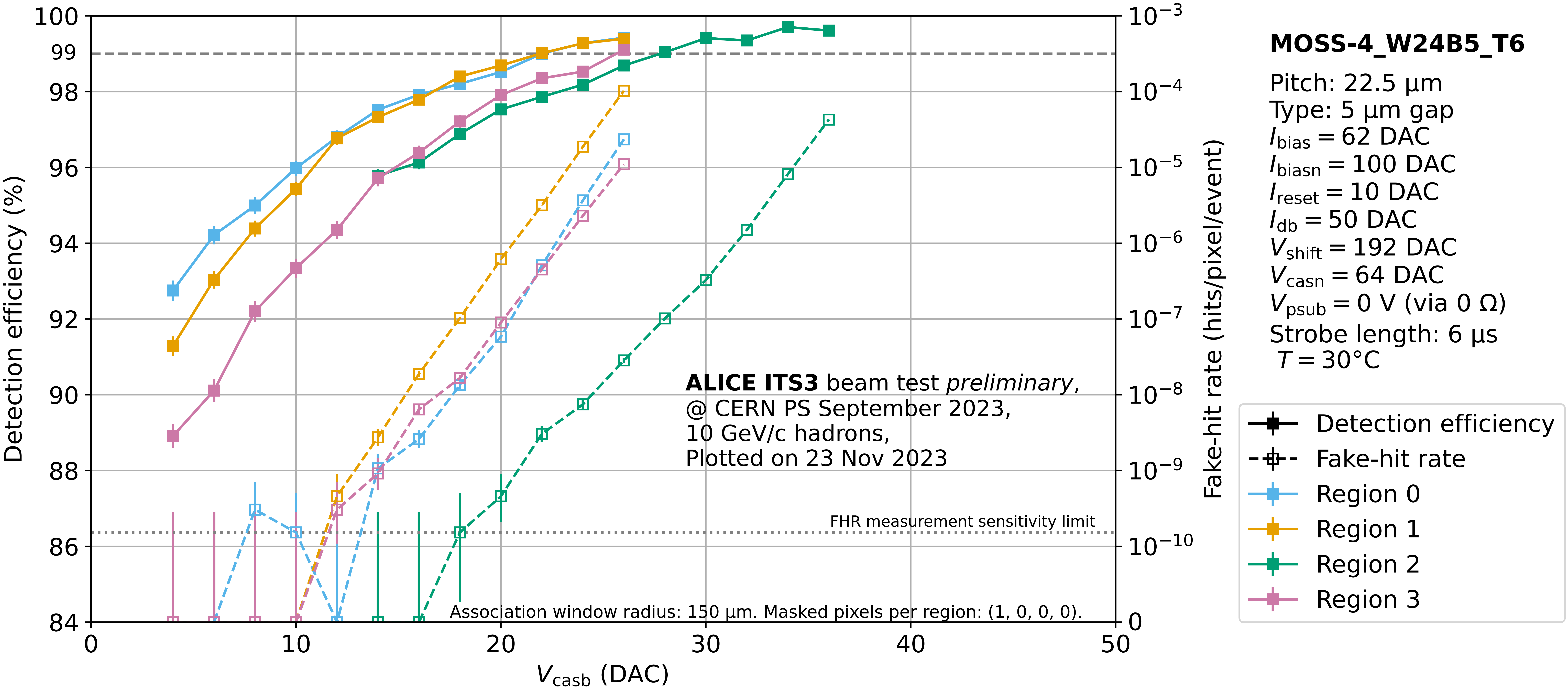






MOSS test beams

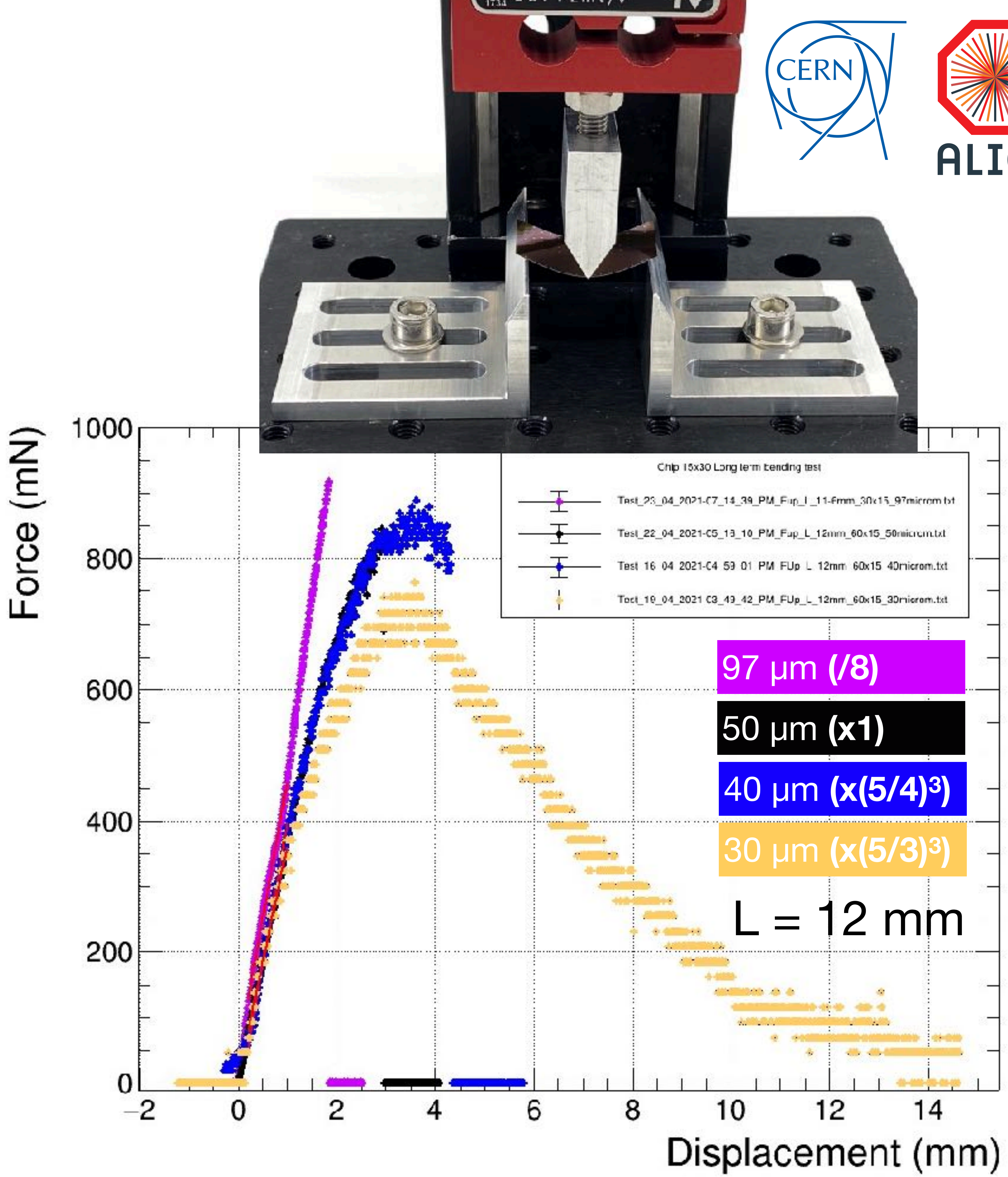
Detection efficiencies and fake-hit rates



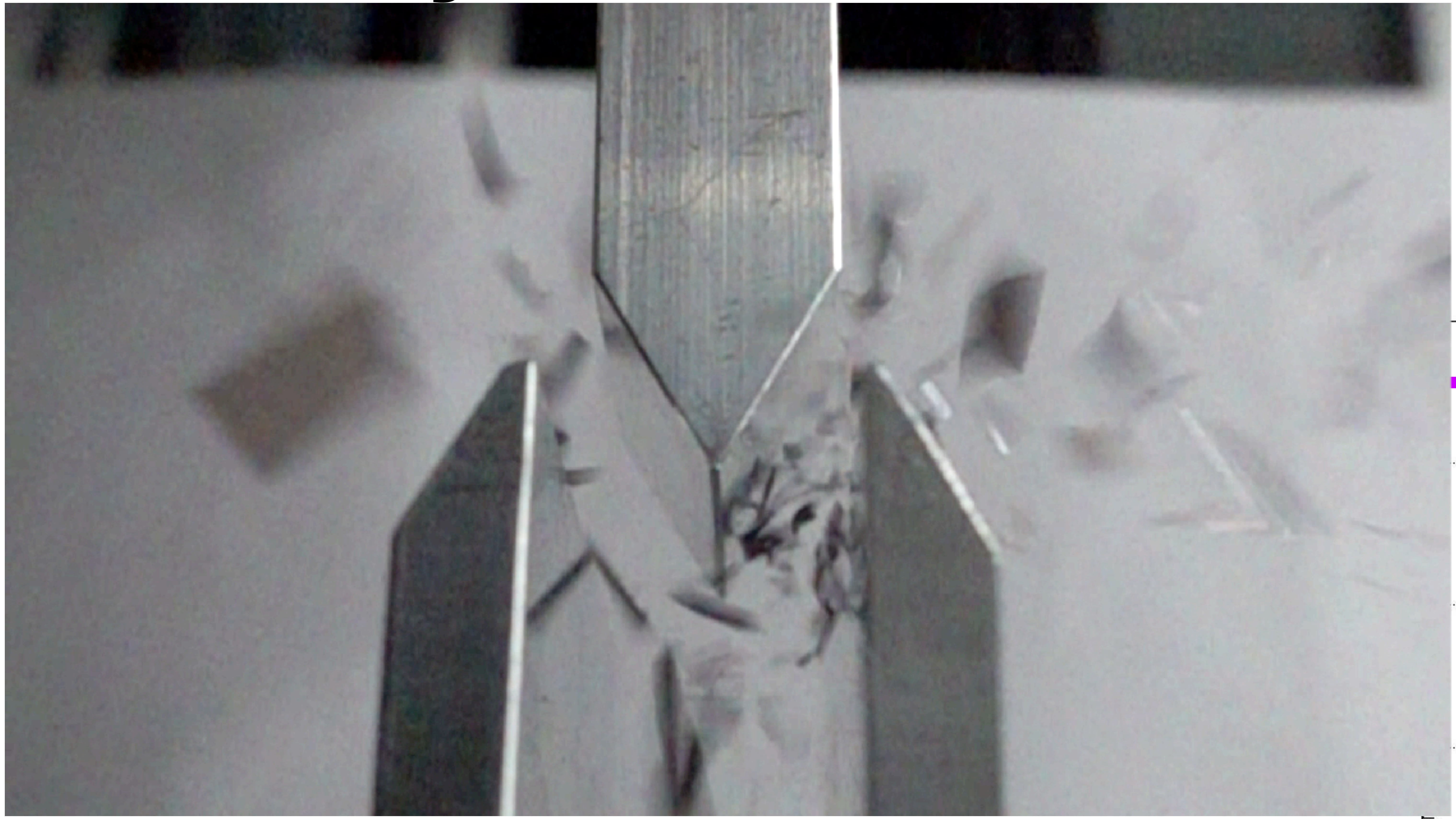
Operational with a bit of margin — NB: bias settings are still being optimised

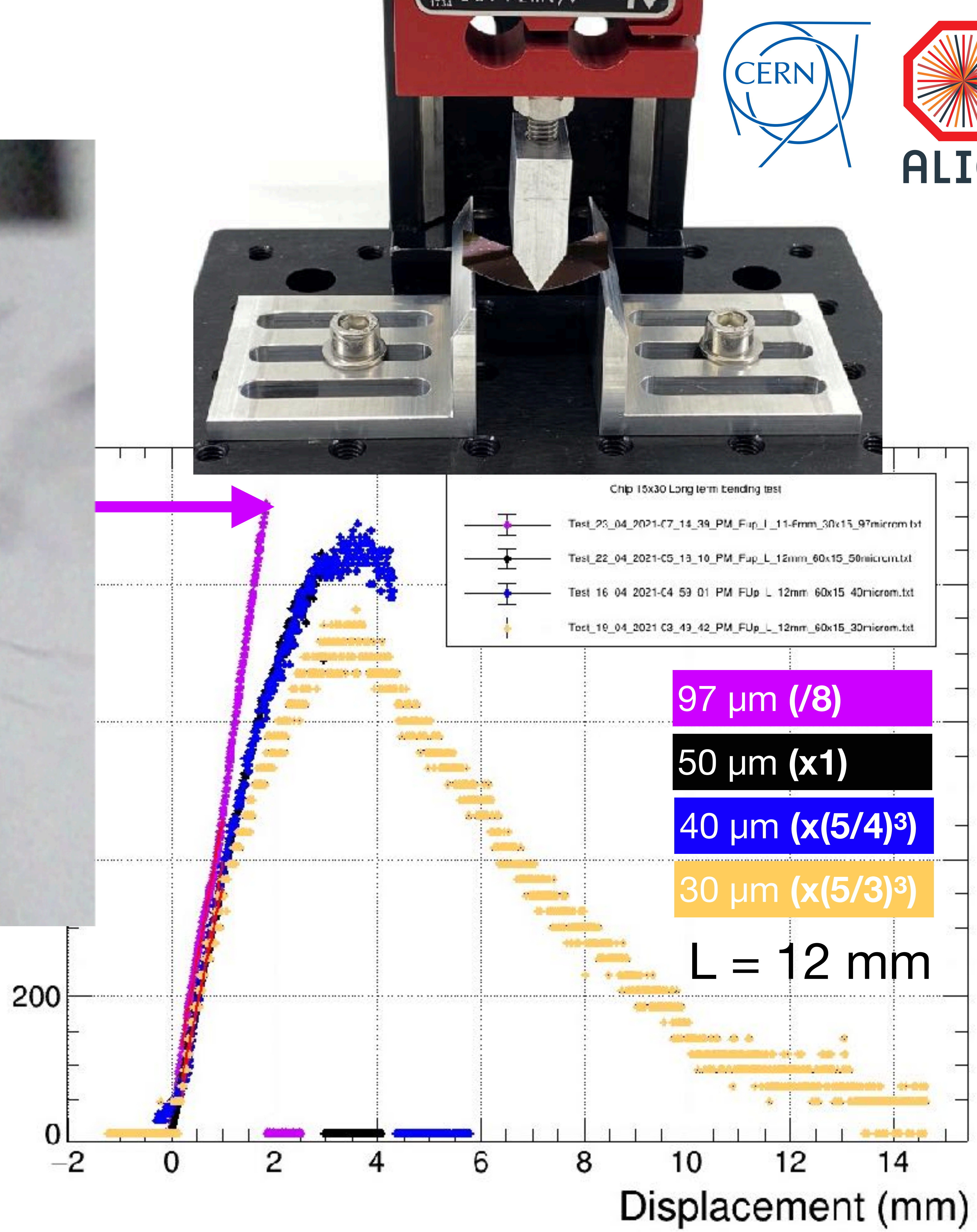
Flexibility of silicon

- **Monolithic** Active Pixel Sensors are quite flexible
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors

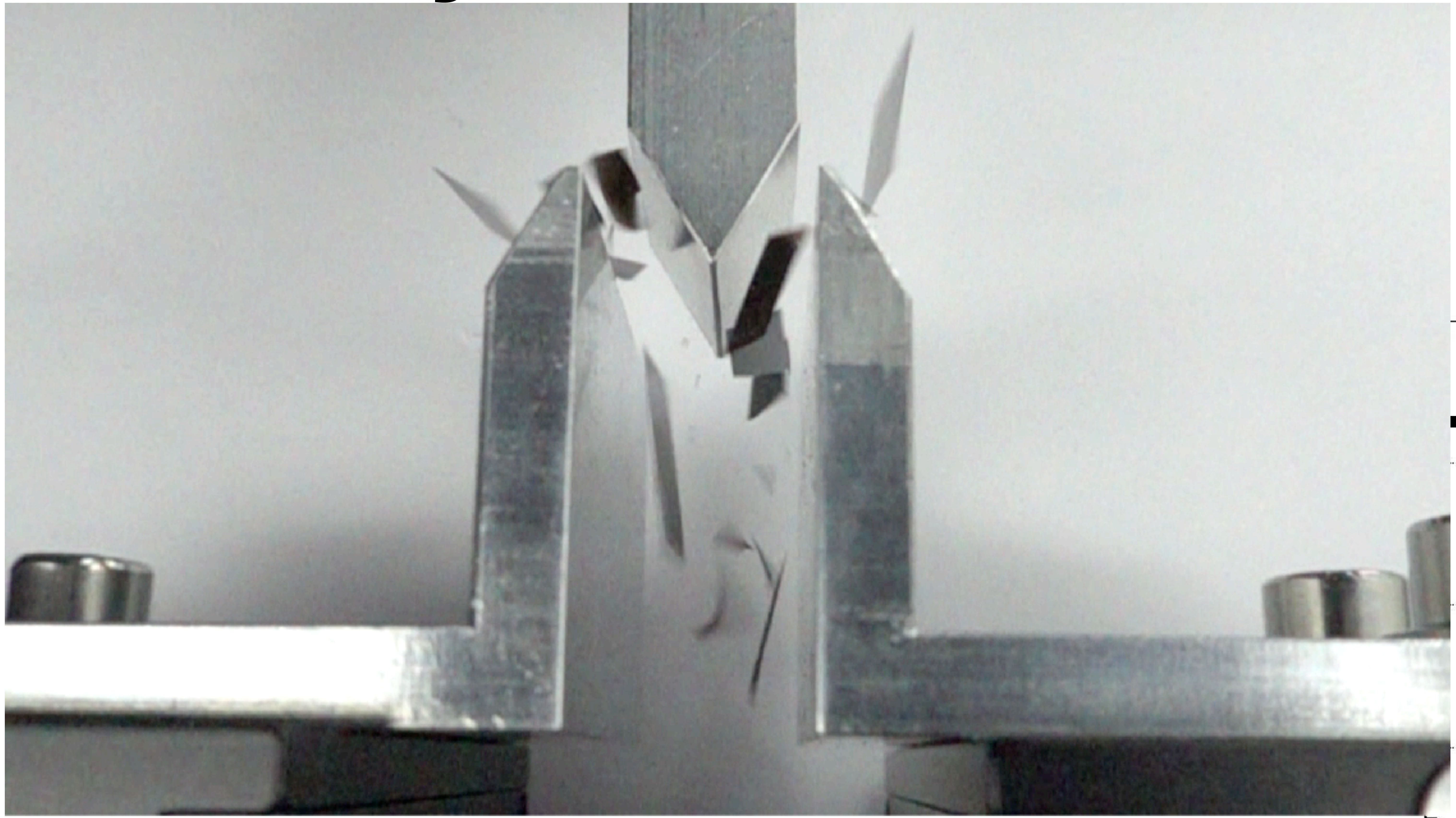


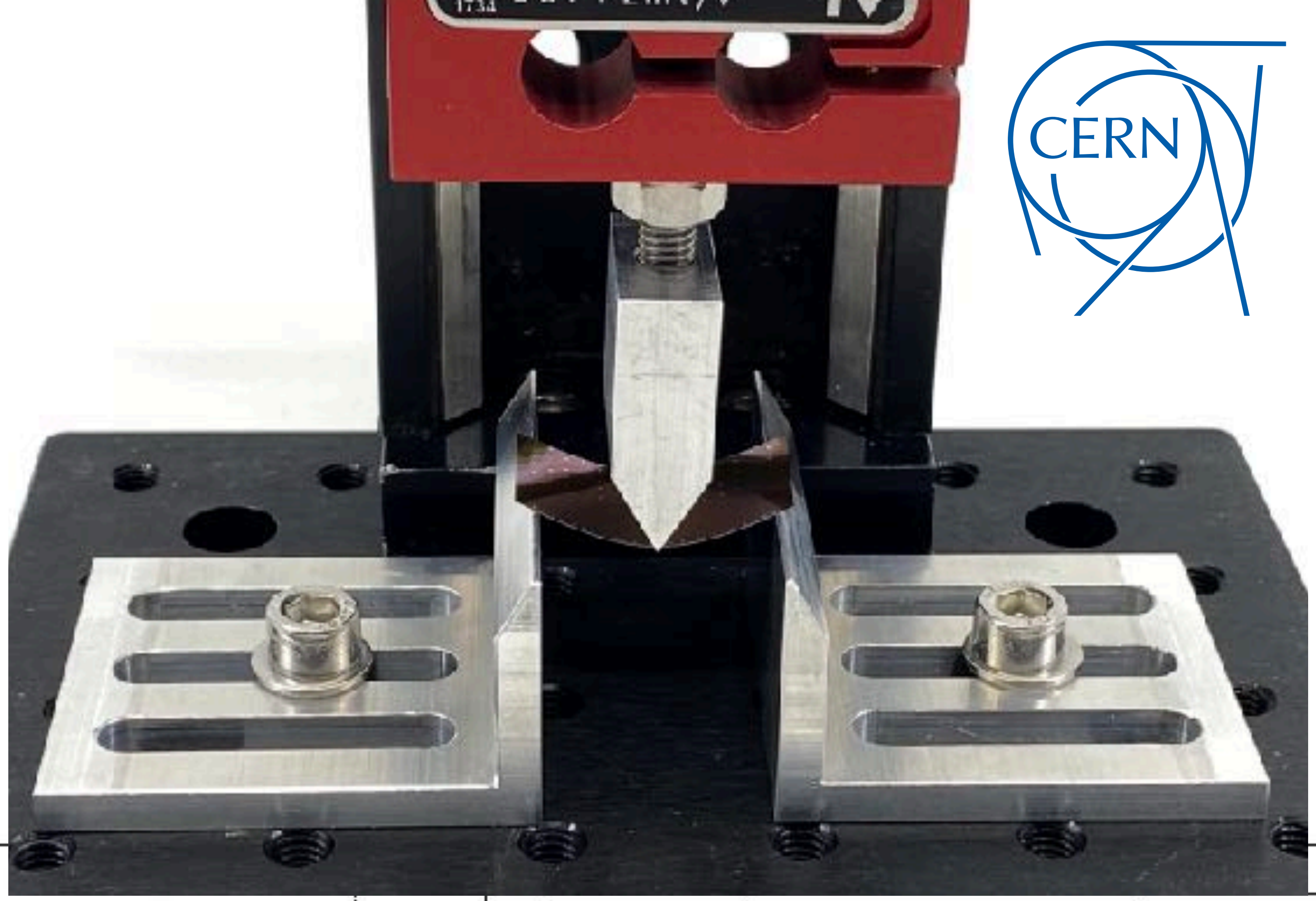
Flexibility of silicon

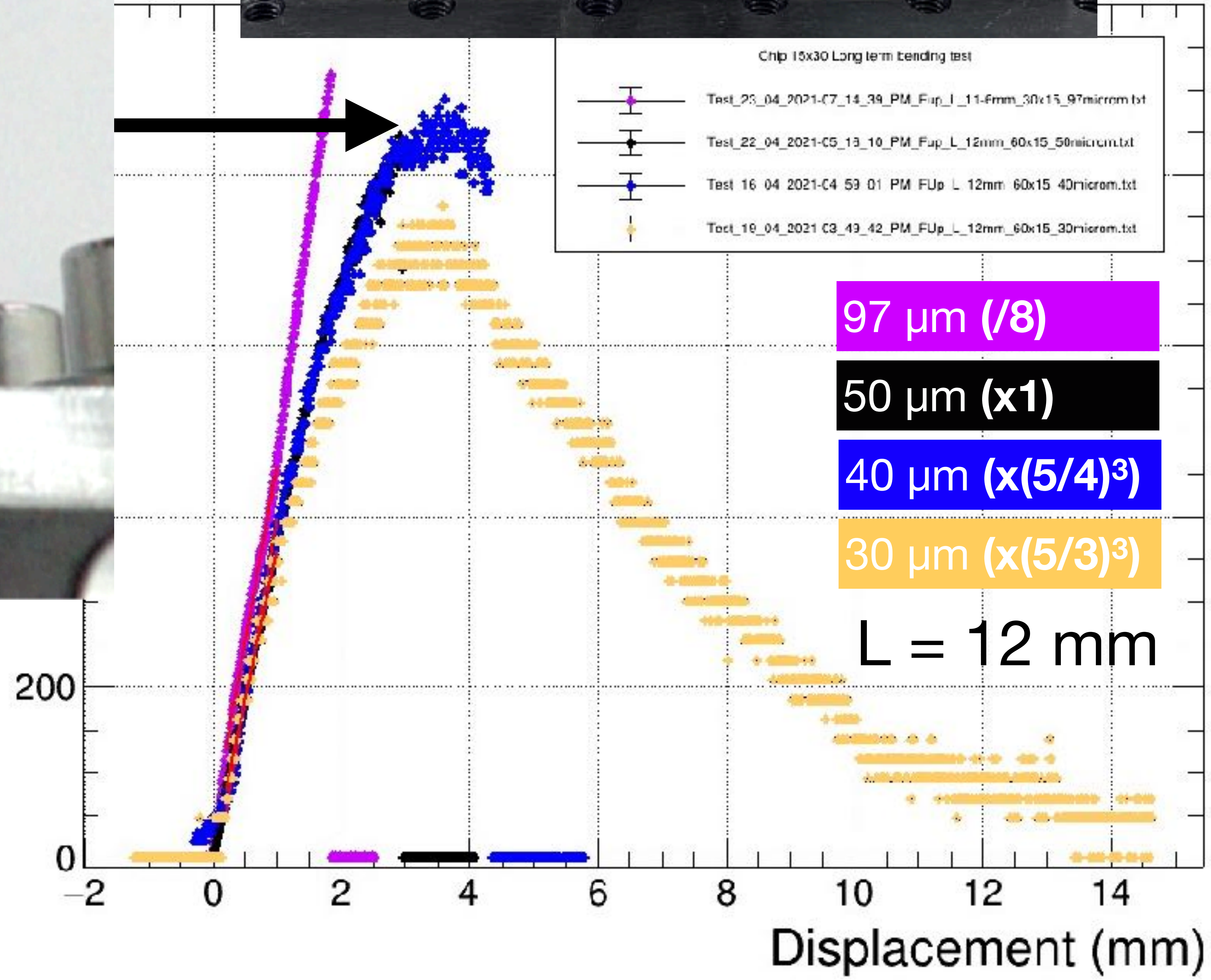




Flexibility of silicon







Flexibility of silicon

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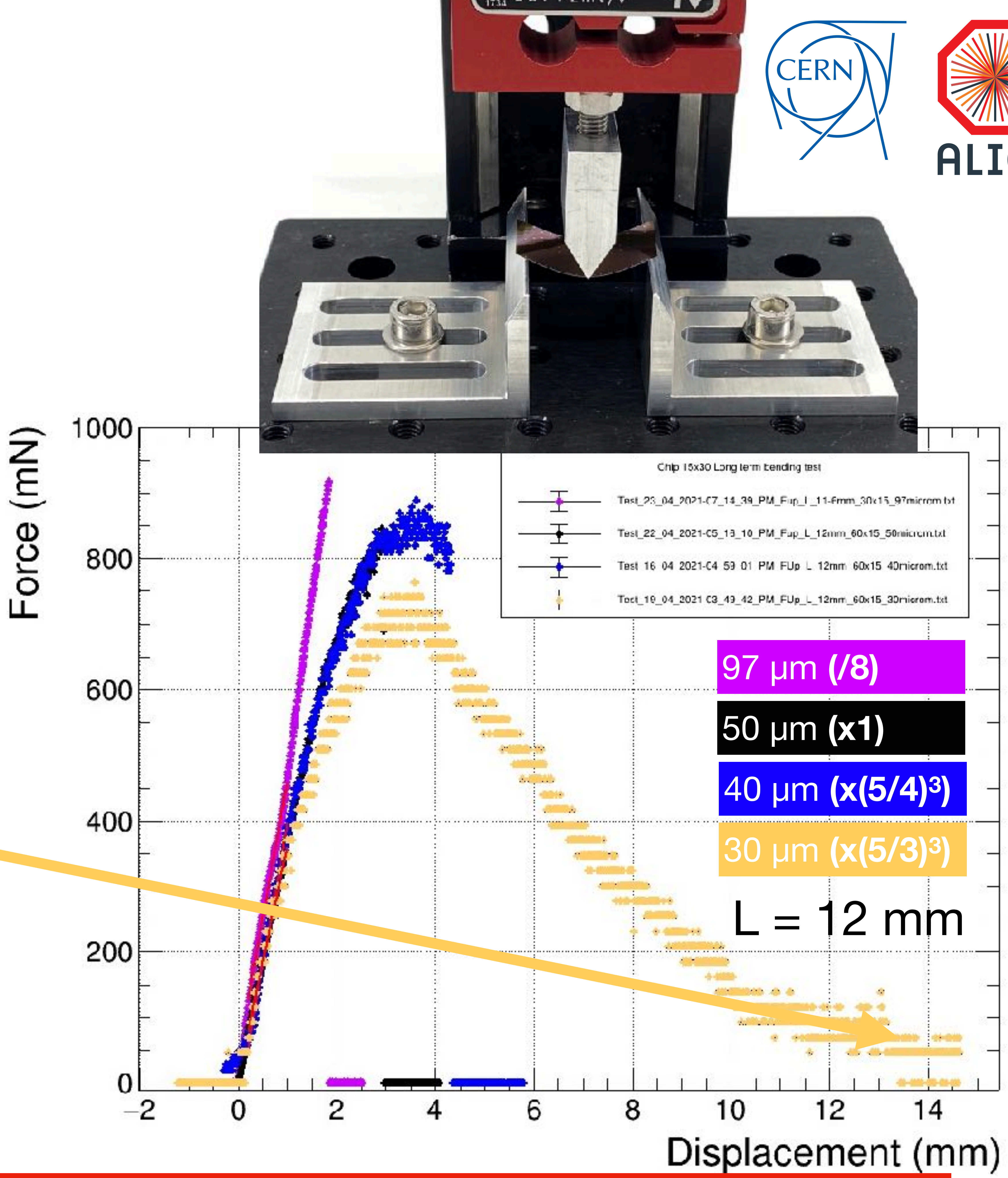


Radii of 2 cm are easily in reach — This is a unique feature of thin, monolithic silicon sensors

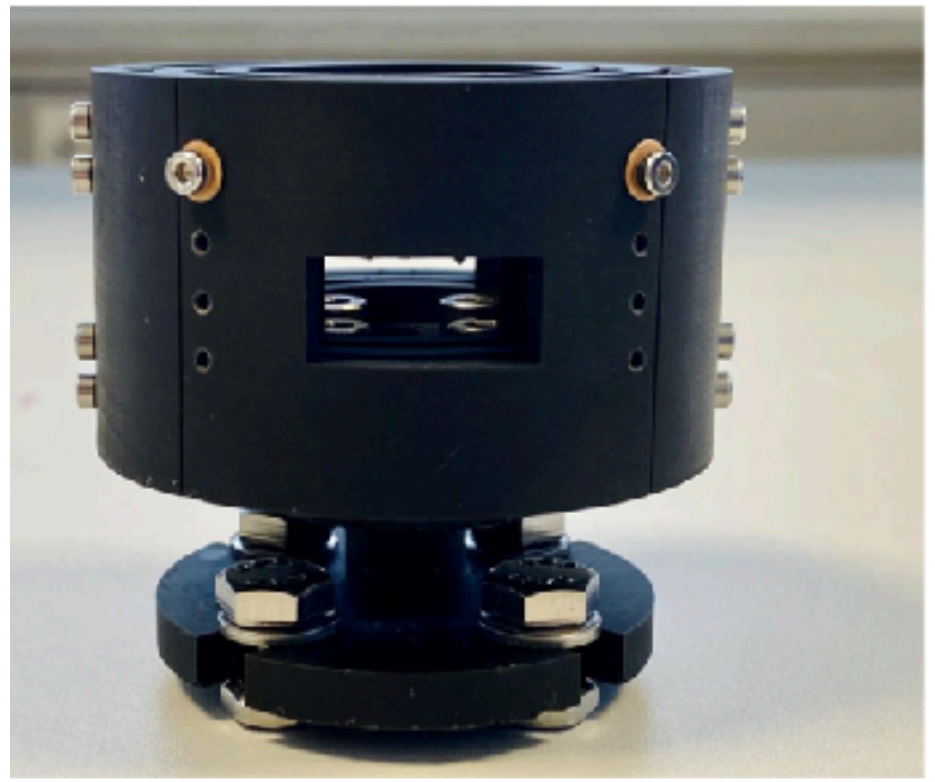
Bending ALPIDE

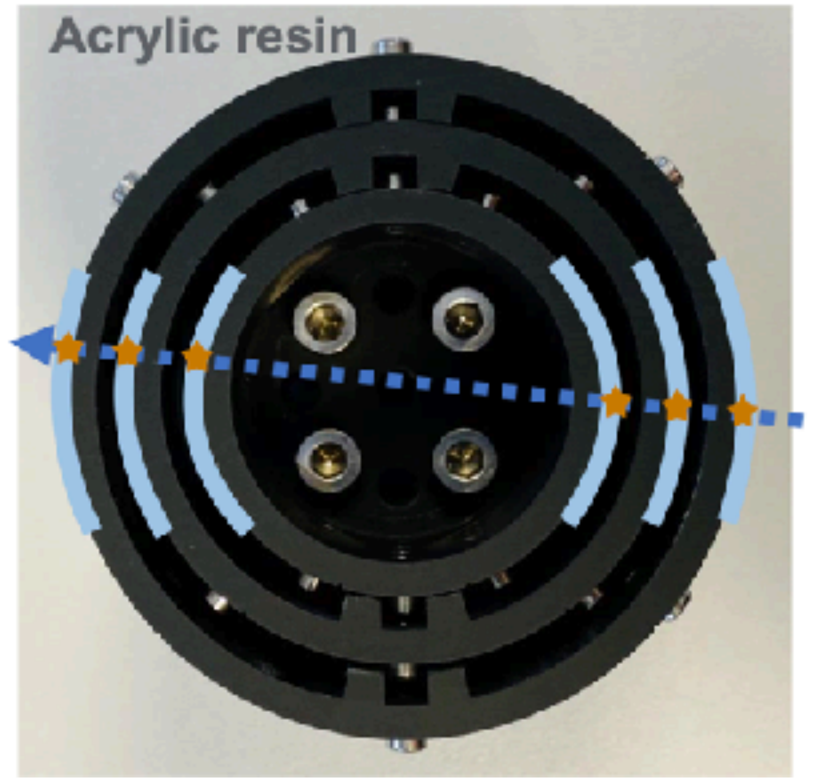
example

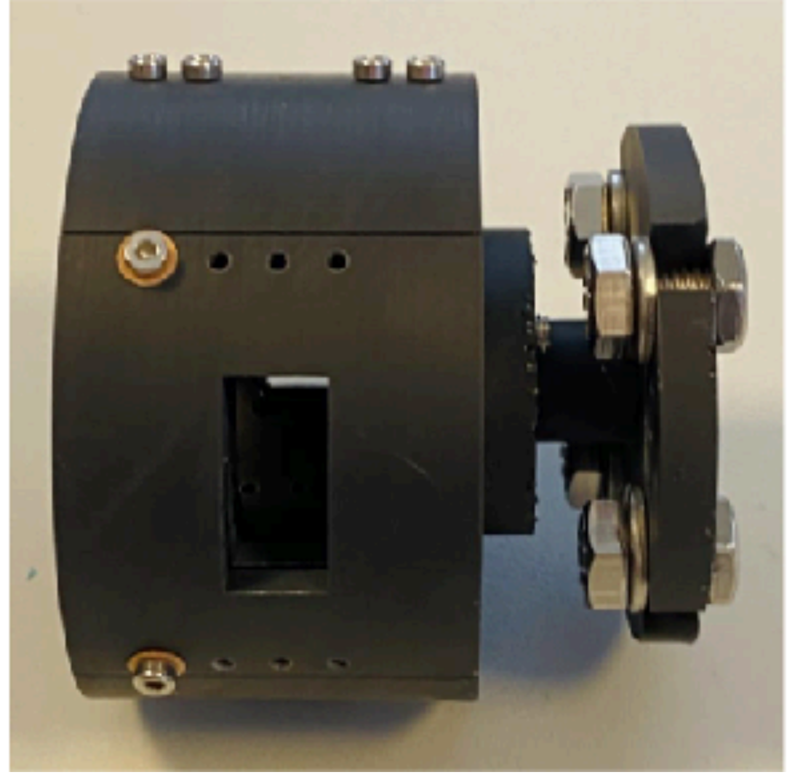
Bent MAPS (2)

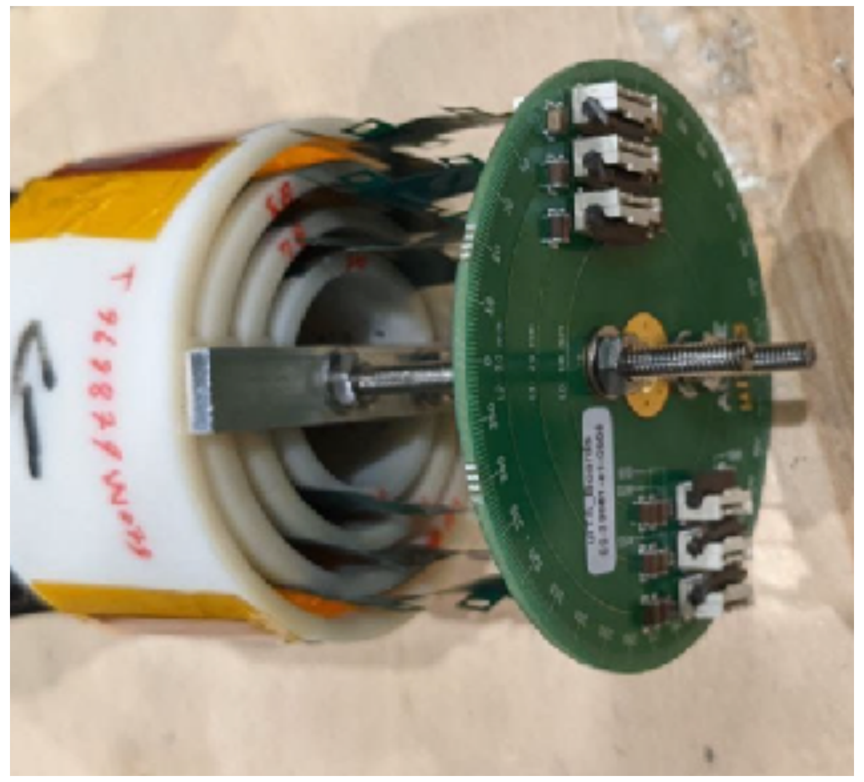
- Functional chips (ALPIDEs) are bent routinely
  - chips continue to work
  - tested at several beam campaigns

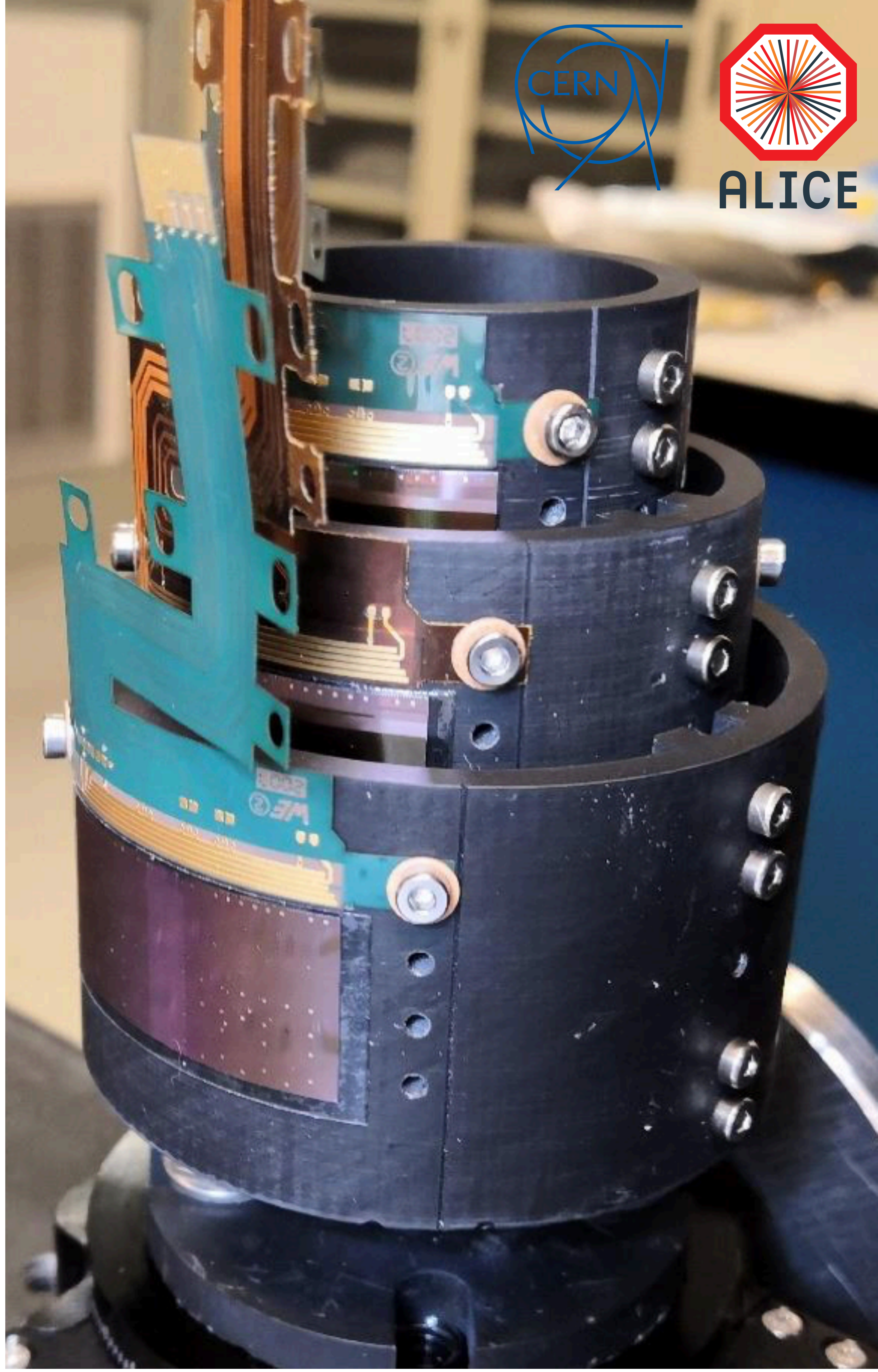
- Complete tracking detectors, called “µITS3” were built and used:
  - 6 ALPIDE chips, bent to the target radii of 18, 24, 30 mm









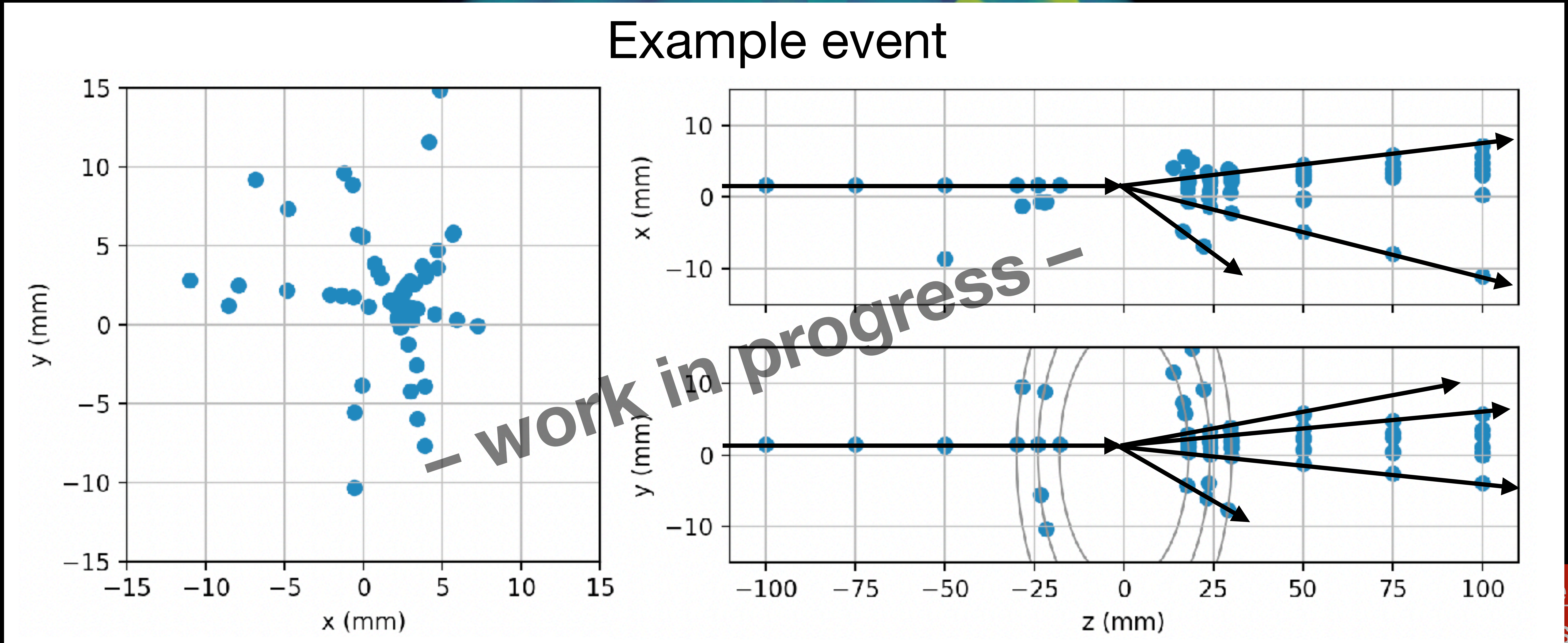


This is a complete detector with unprecedented performance figures

µITS3 X-ray tomography

→ poster by Berkin Ulukutlu

µITS3 X-ray tomography



[few hand-drawn track lines to guide the eye]

sults:
solution
ction efficiency
no effect of bending

→ poster by Berkin Ulukutlu

Bending of wafer-scale sensors

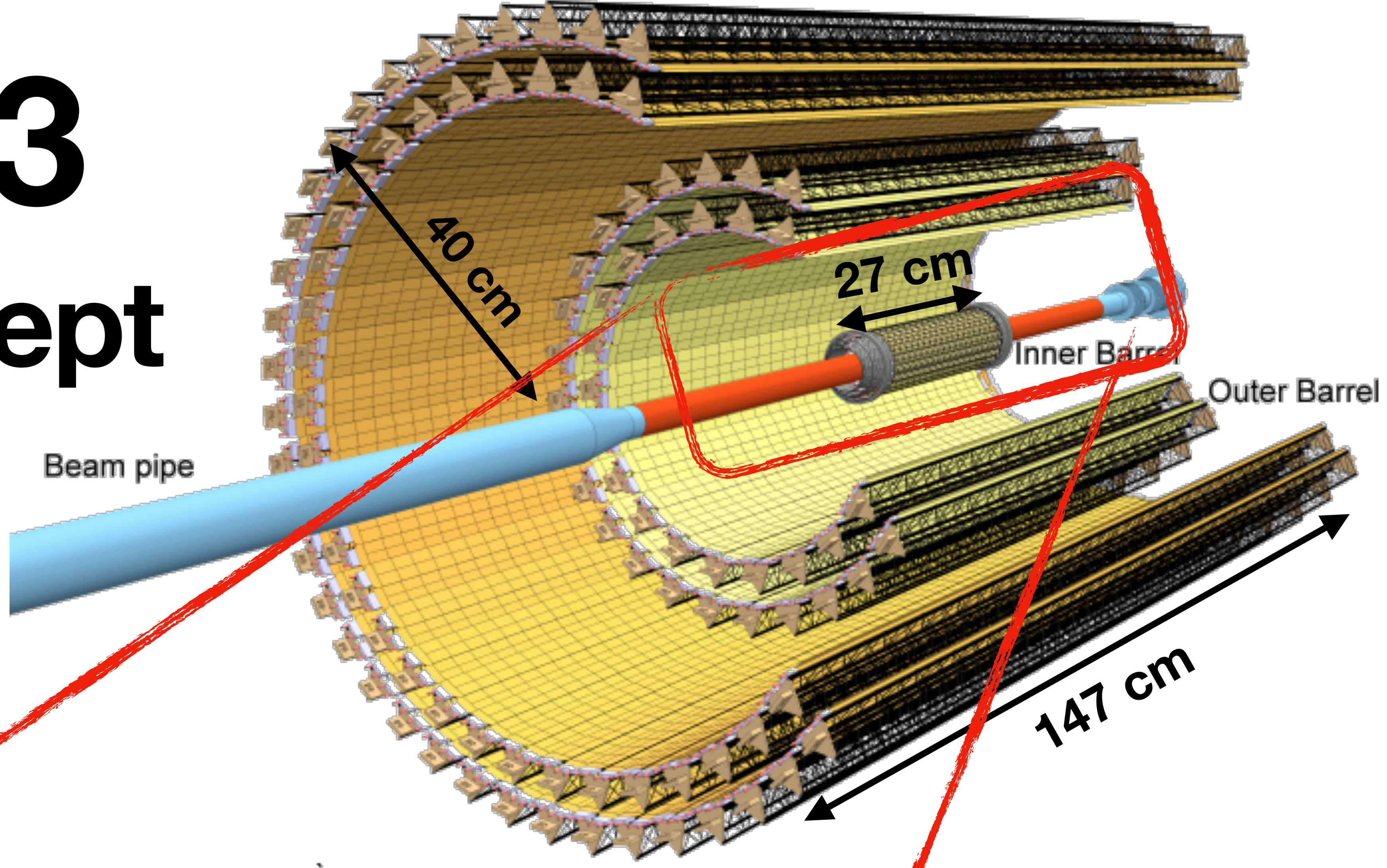
procedure

Bending of fully processed wafers
(48x speedup)

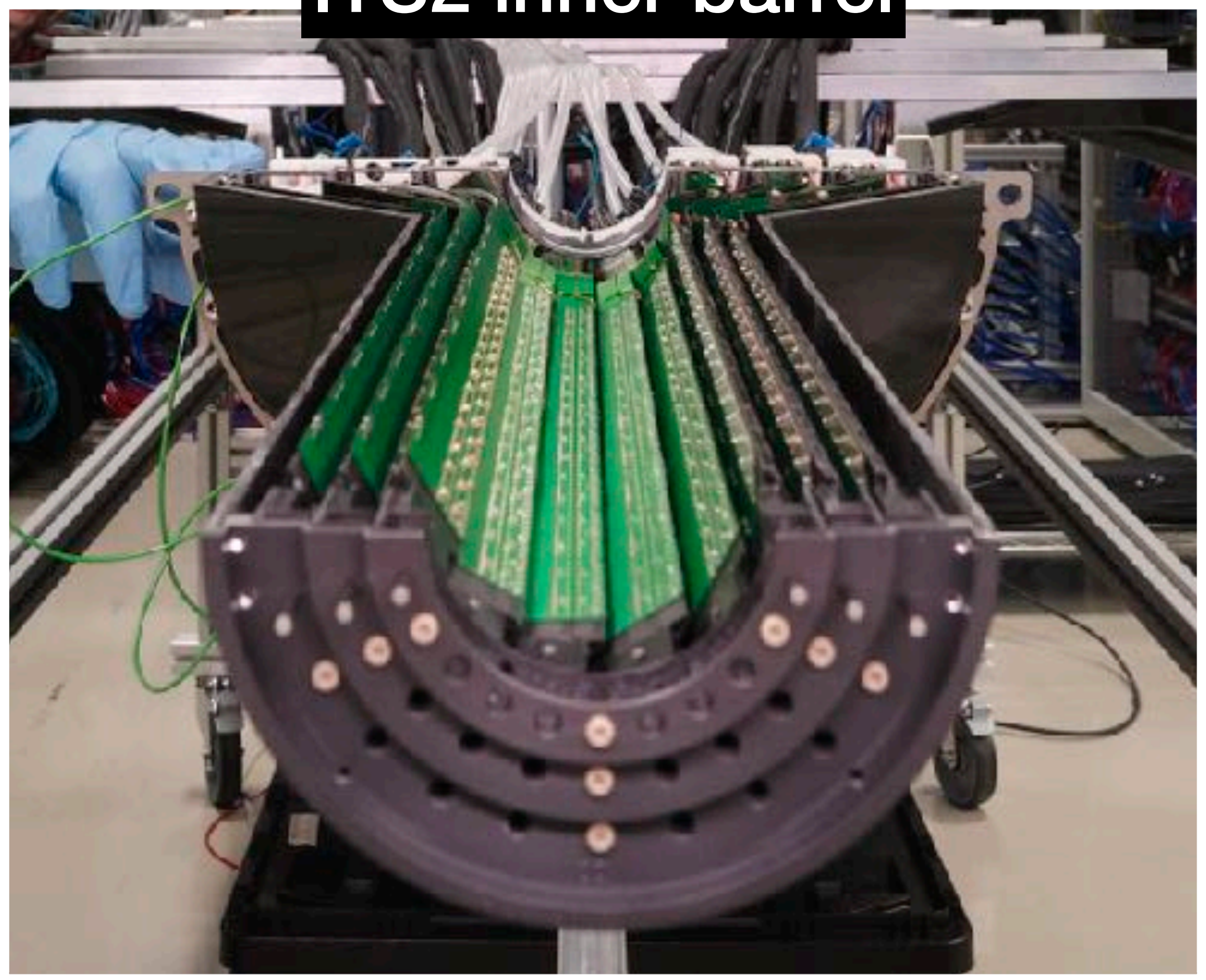
R = 18 mm
50 µm fully processed silicon

→ poster by Anna Vilani

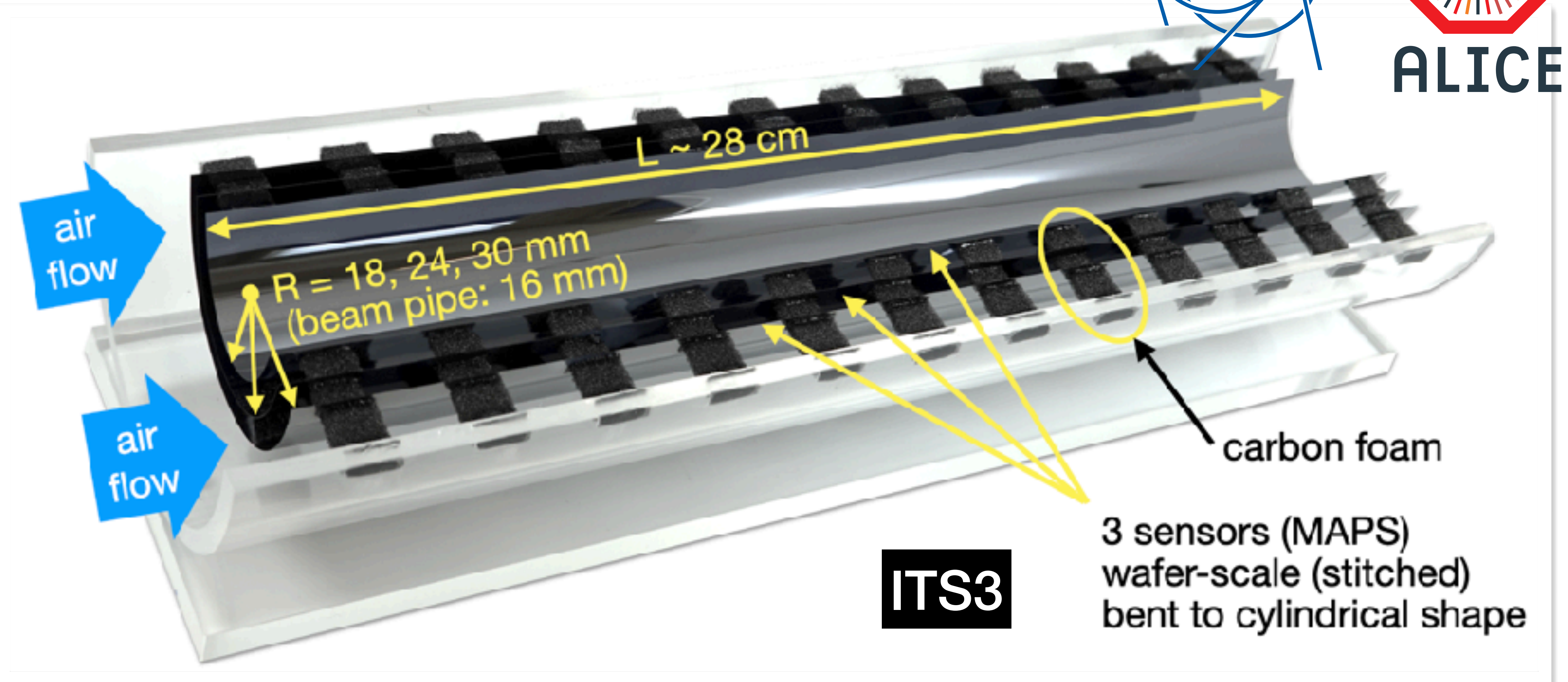
ITS3 concept

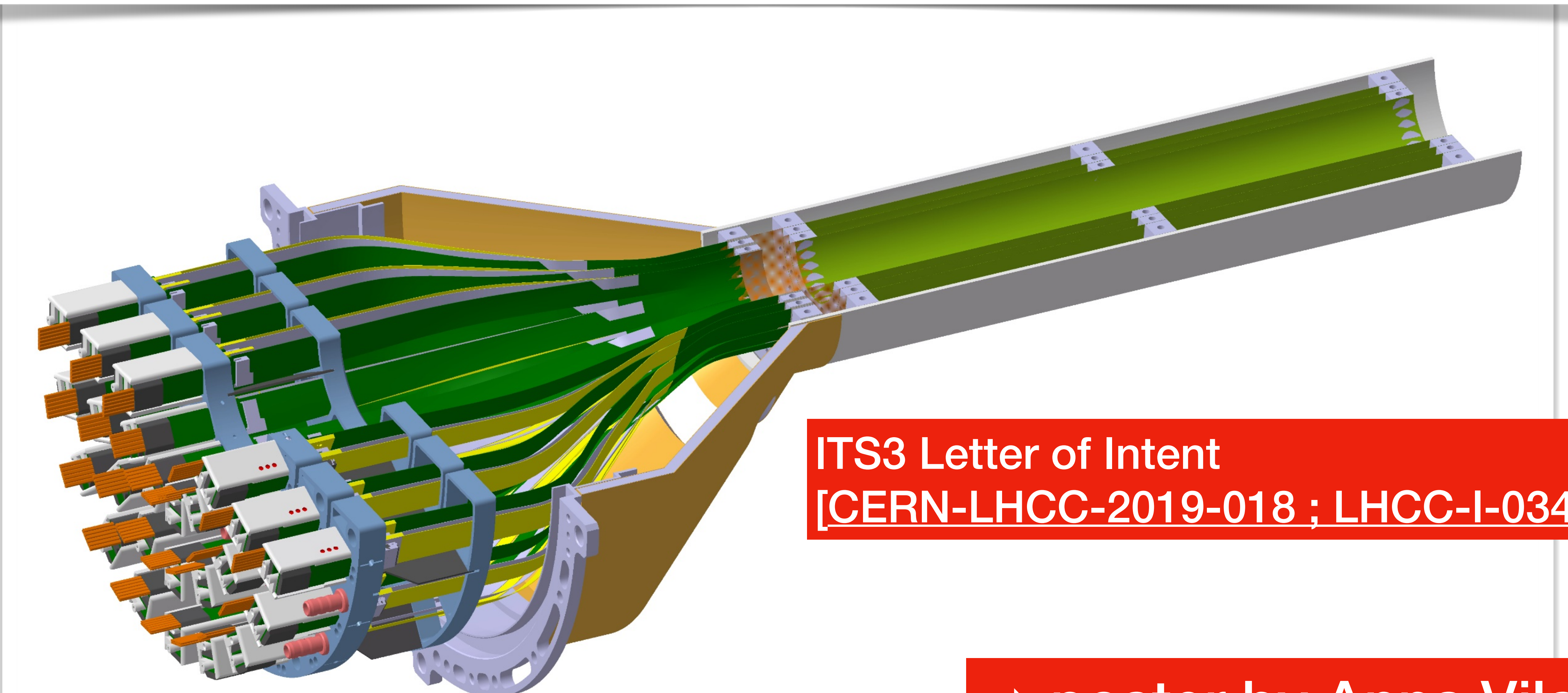


ITS2 inner barrel



LS3 replacement of inner barrel





ITS3 Letter of Intent
[CERN-LHCC-2019-018 ; LHCC-I-034]

→ poster by Anna Vilani

	Run 3				LS3			Run 4				LS4		
2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035

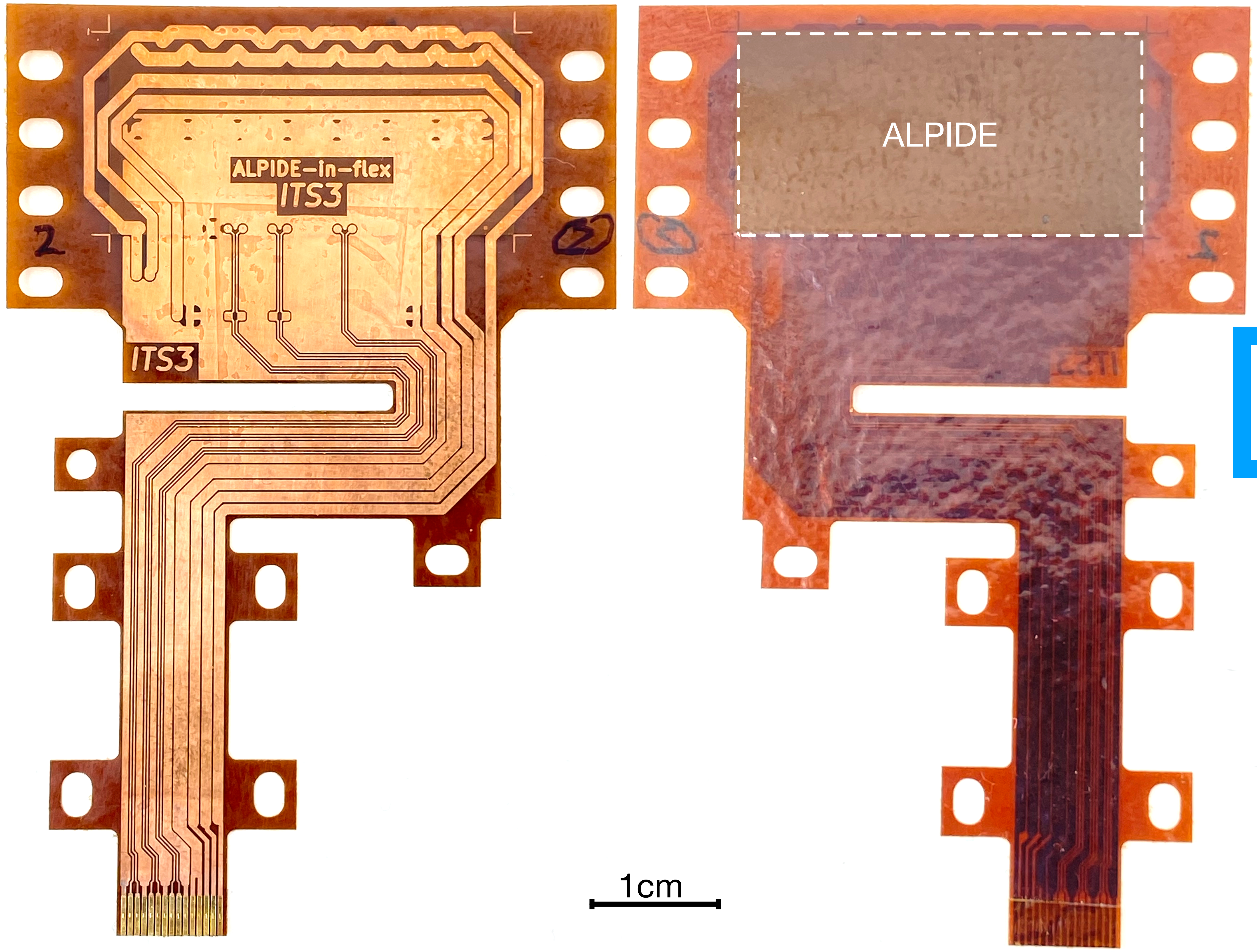
[LHC timeline]

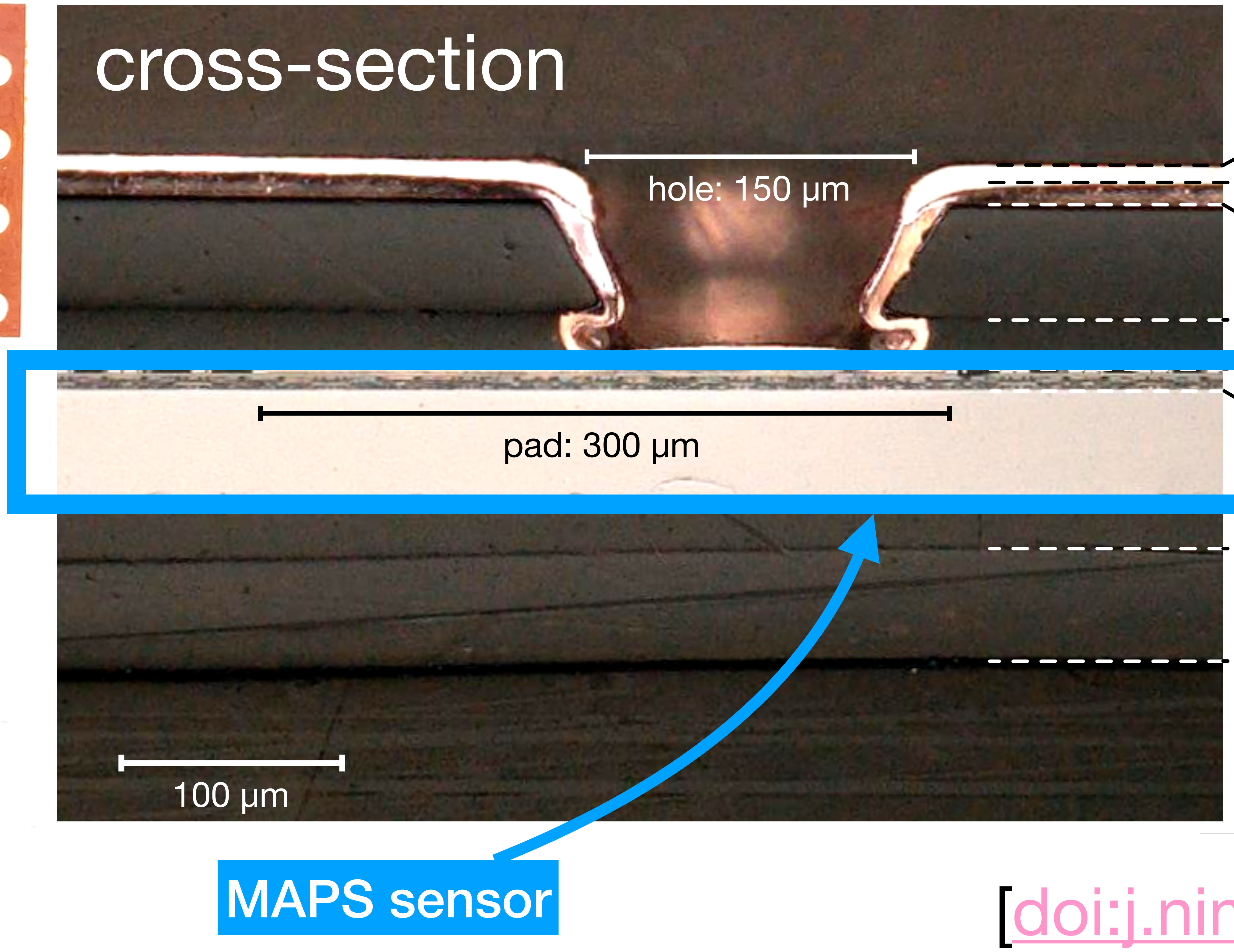
Further future

New modularisation ideas

example: “MAPS foils” — chips within printed circuit boards

- Very thin and robust modules can be built
- Interesting for many applications, especially those looking at larger areas



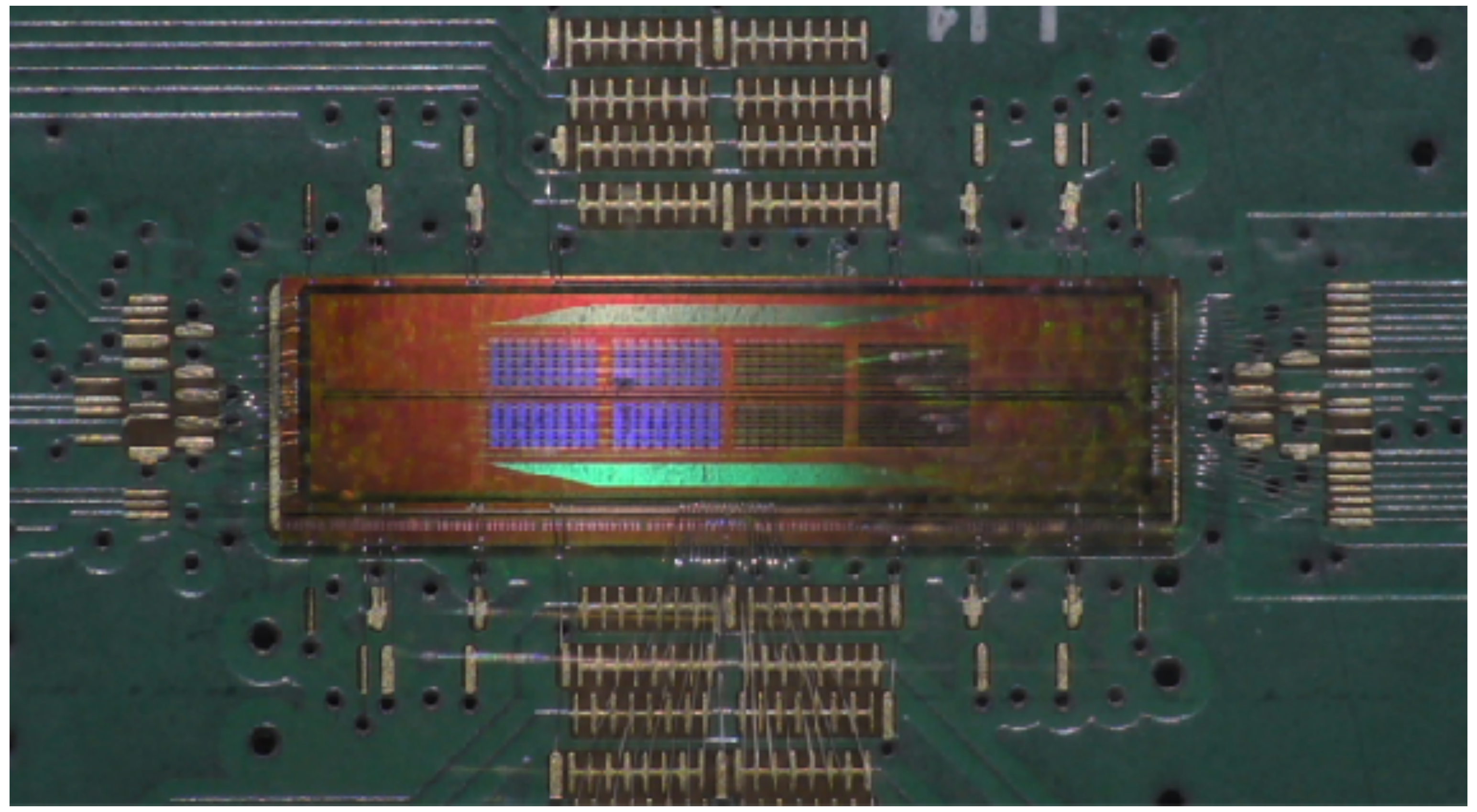


part	thickness
Cu plating	13 µm
Cu gladding	5 µm
Polyimide	45 µm
glue	25 µm
metal stack	10 µm
silicon	45 µm
glue	25 µm
Polyimide	45 µm
total:	**213 µm**

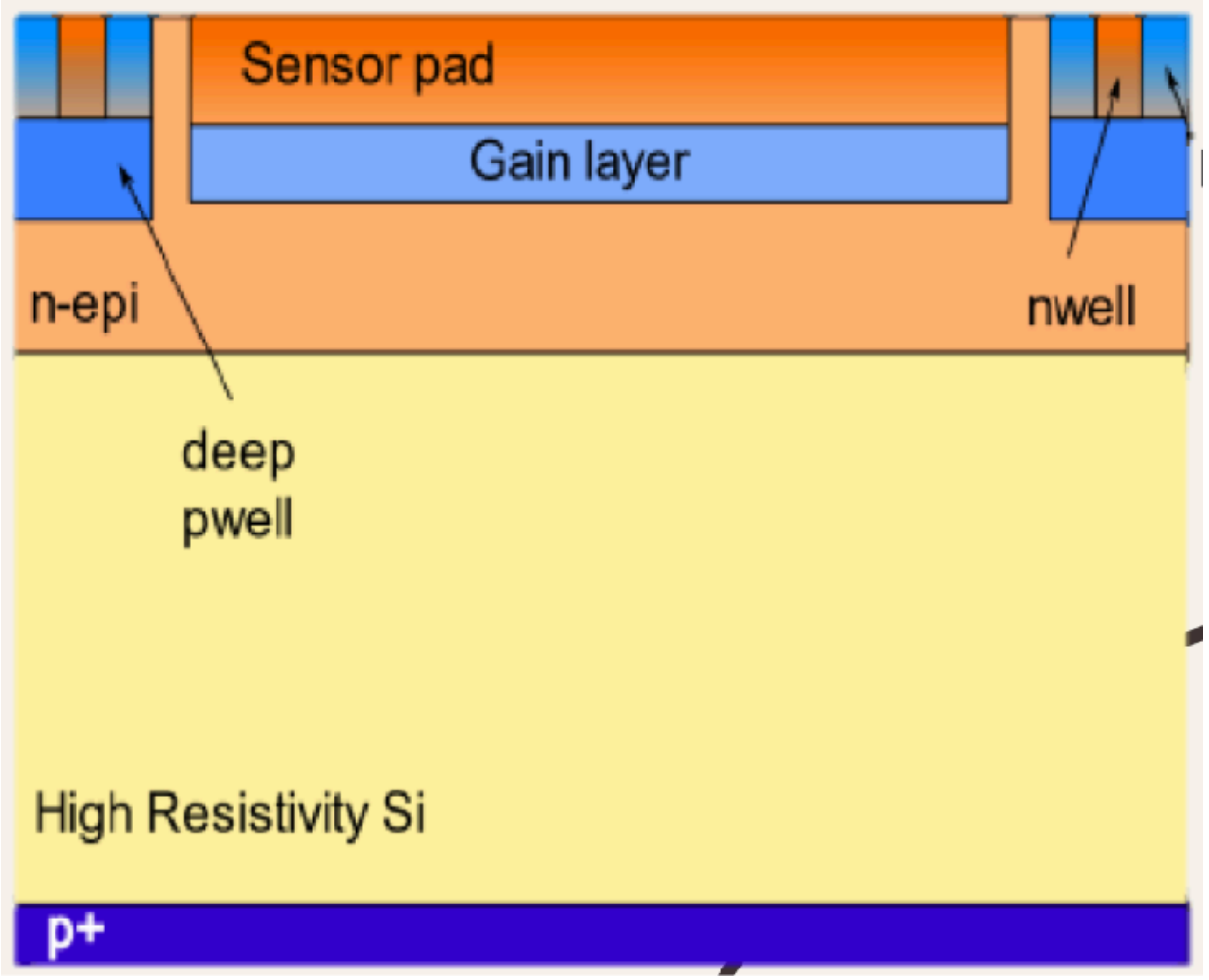
[doi:j.nima.2022.167673]

CMOS with gain

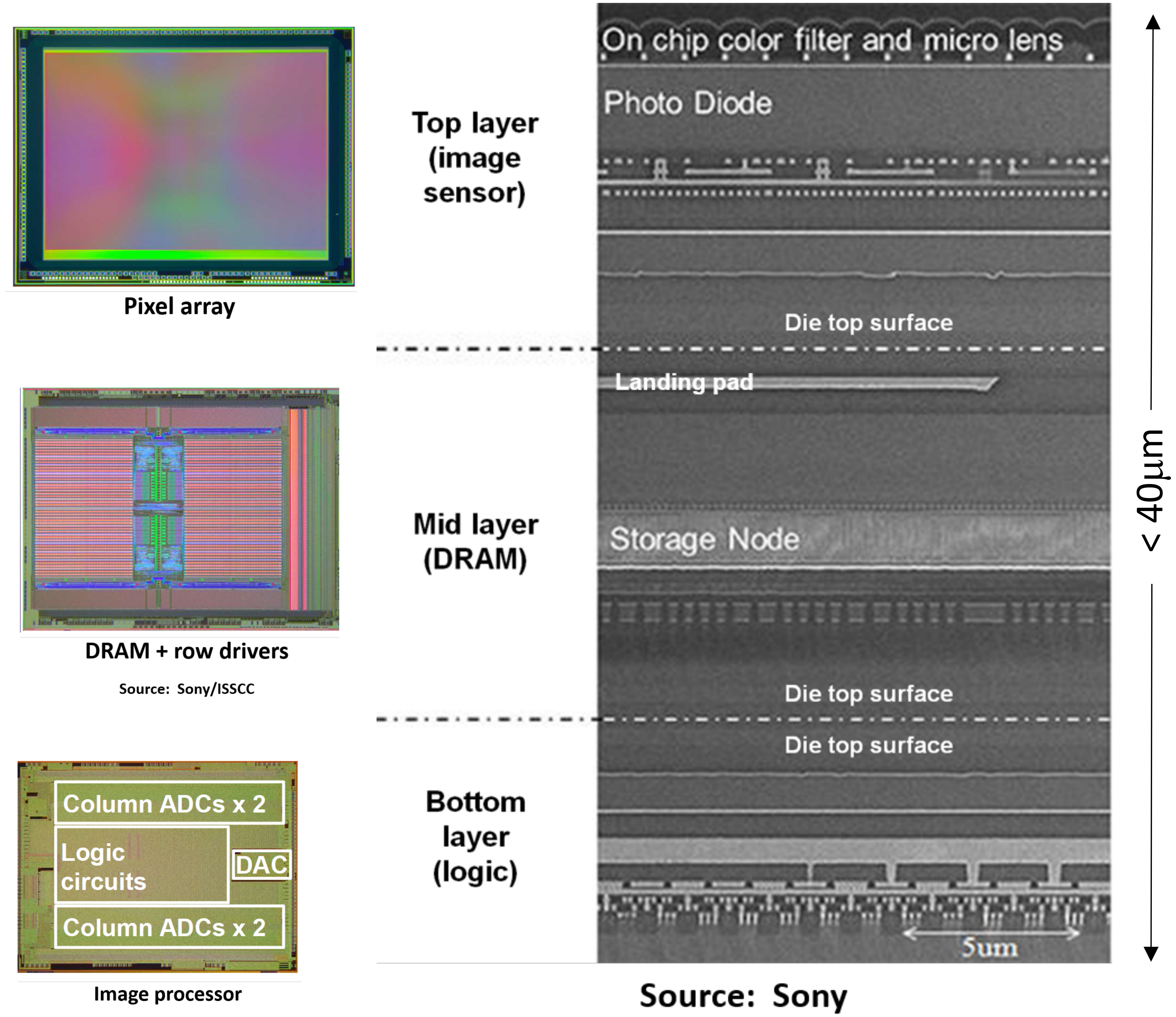
- Adding again layer below the sensor
- Potentially reduced power (larger signal) and increases timing performance
- First prototypes recently became available and are under test right now



[ARCADIA MadPix]



3D integration



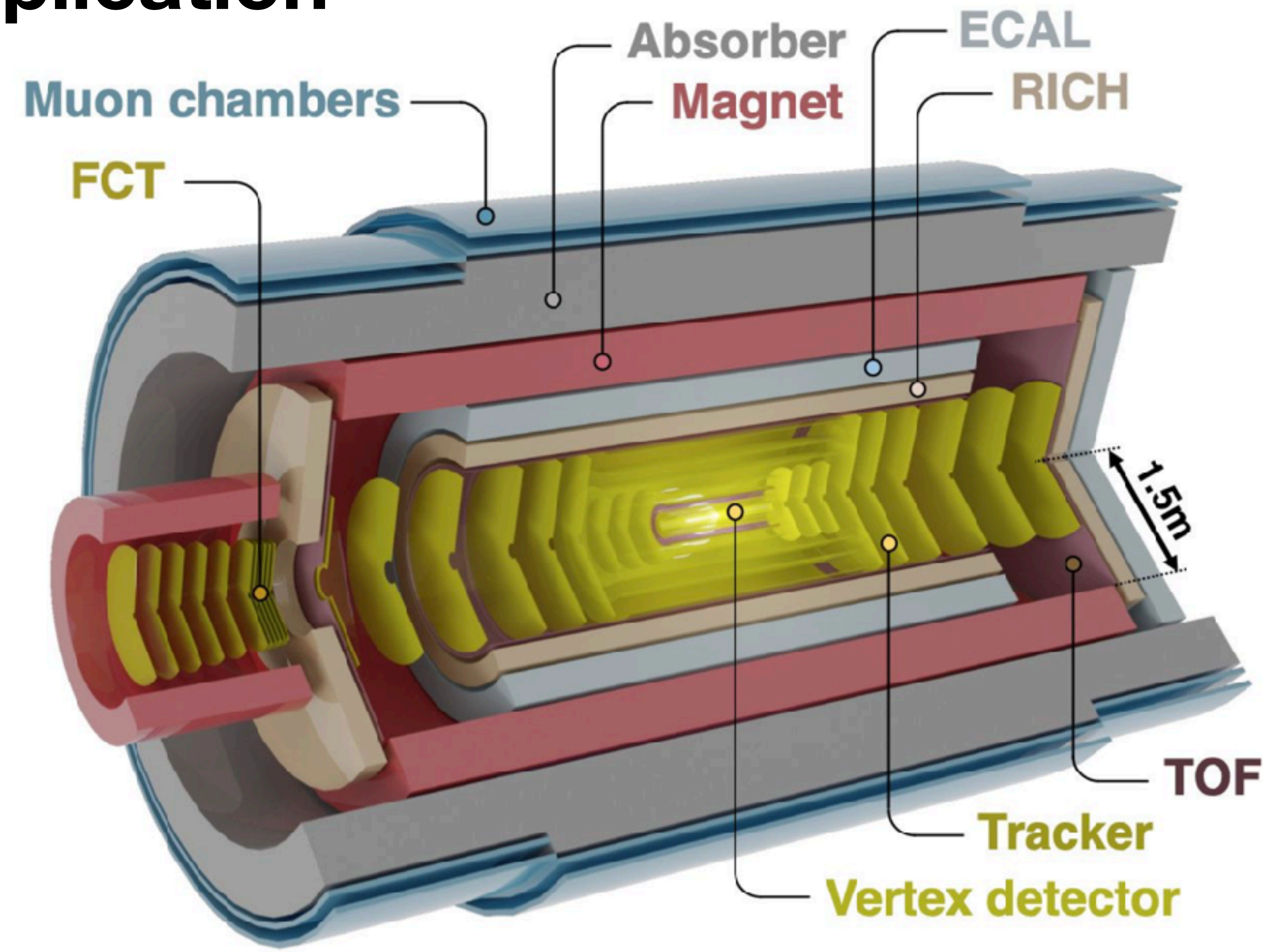
[ISSCC, Feb 2017]

- Industry moves towards stacks of chips
- Resulting stacks are still very thin
- This (again) opens up sever opportunities for us
- Several technologies can be combined (e.g. pixel array from vendor A, readout chip from vendor B)
- Effect on design effort to be seen

ALICE 3 (LHC LS4, 2033-34)

the next concrete large-scale HEP application

- Largely based on CMOS technology
  - ultra-precise (2.5 μm resolution) in-vacuum vertex detector
  - large-area (O(60 m²)) vertex detector
  - time of flight (20 ps)
- Relies on expertise gained with current developments (ALICE ITS2, ITS3)
- Will be a main driver for the technology development for the next decade
- De-facto prototype of an FCC-ee detector



[LHC timeline]

Summary & Outlook

- **CMOS** technology **advances rapidly**
  - as community, we largely benefit from this commercial success
  - significant improvements designs in terms of **integration density, power consumption, radiation hardness, and readout speeds** over last years
  - **commercially** available and easily obtainable in **large quantities**
- **ALICE ITS2: 10 m² MAPS** detector, fully commissioned and operational
  - project-driven development, propelled the technology
- Now pushing the technology further:
  - non-planar geometries: **bending**
  - deeper sub micron technology node: **65 nm**
  - wafer-scale sensors: **stitching**
- CMOS sensors are a technology of choice for many **future** applications

Thank you!