

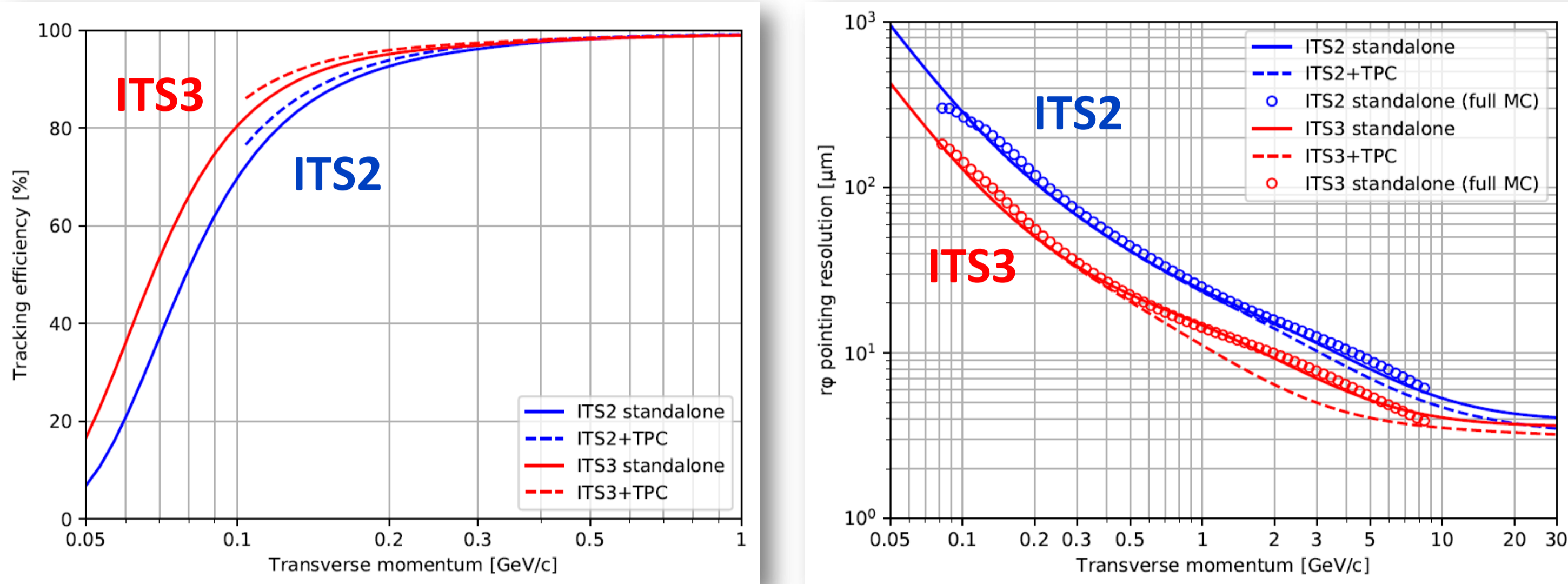
ITS3: The upgrade of the Inner Tracking System of the ALICE Experiment

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1. Physics motivation

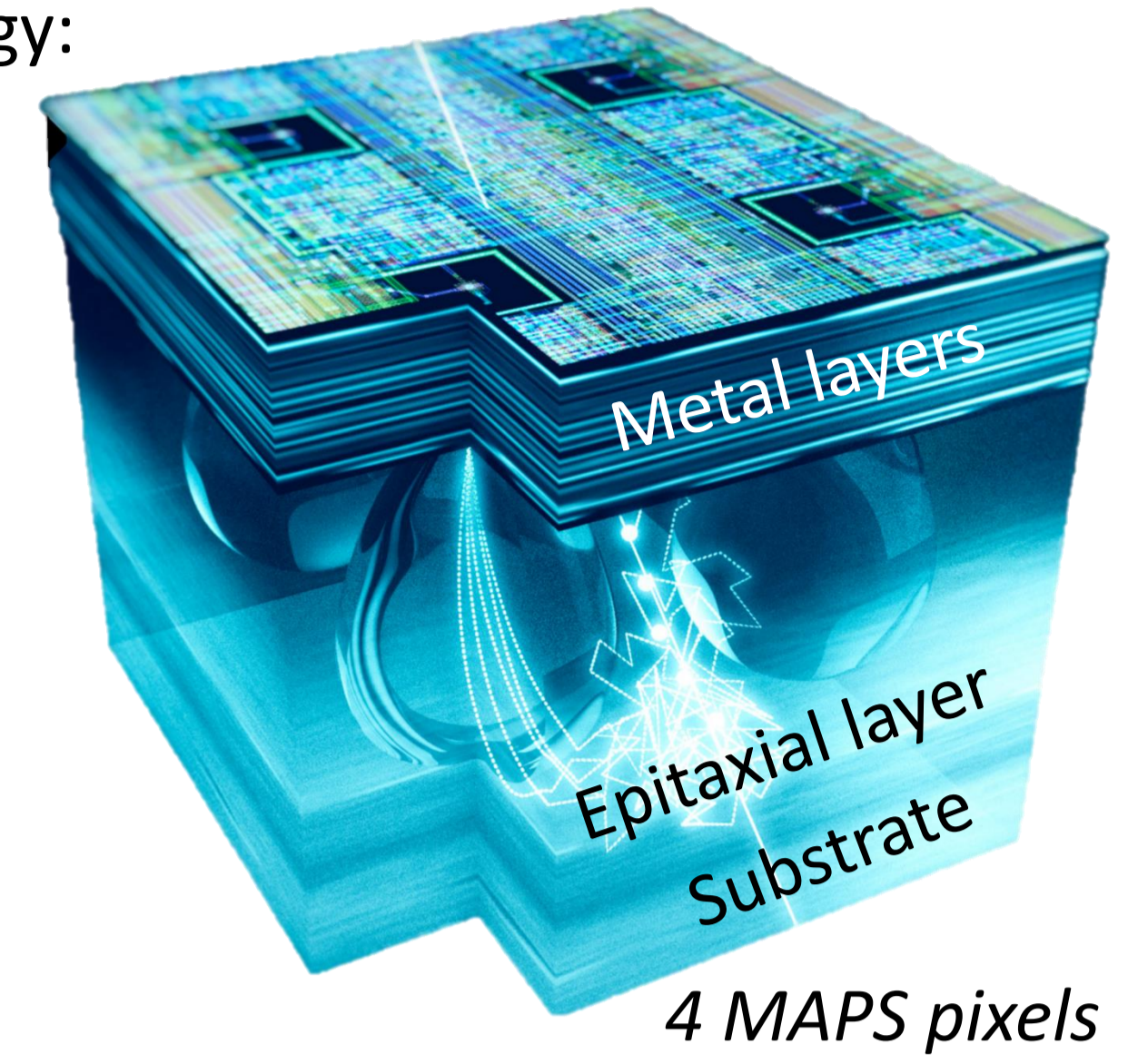
- The innermost layers of the ALICE Inner Tracking System (ITS2) will be replaced with a **new tracker** during LHC Long Shutdown 3 (2026-2028), the **ITS3** [1].
- This upgrade will further improve **tracking efficiency** and **pointing resolution** especially for low momentum particles, thus allowing to improve the precision of **measurements in the heavy-flavour sector** and to bring **another set of fundamental observables** into reach [2].
- E.g. these measurements will be allowed:
 - B_s^0 and Λ_b^0 at low transverse momenta
 - Non-prompt D_s^+ and Ξ_c^+ decays** in heavy-ion collisions



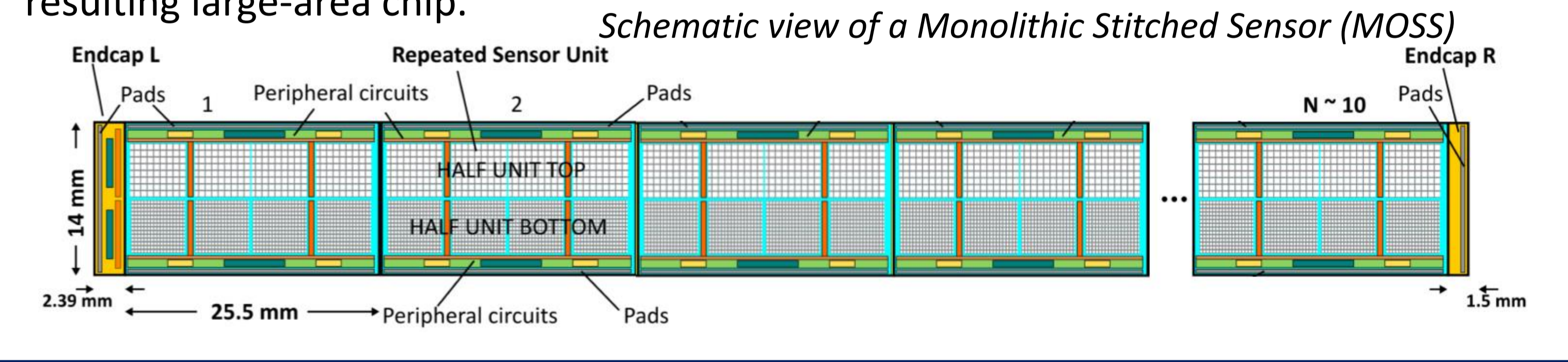
2. Monolithic Active Pixel Sensor (MAPS) technology

The ITS3 will be realized using the MAPS technology:

- Read-out logic and sensitive volume in the **same silicon crystal**
- Complete in-pixel **CMOS circuitry**
- Ultra-thin silicon** ($\leq 50 \mu\text{m}$)
- The Tower Partners Semiconductor Co. [3] **65 nm CMOS imaging process** for MAPS was chosen for the ALICE ITS3. Key advantages:
 - High **radiation hardness**
 - Low **power consumption**
 - 5 μm 2D spatial resolution**
 - Large wafers** ($\varnothing 300 \text{ mm}$)

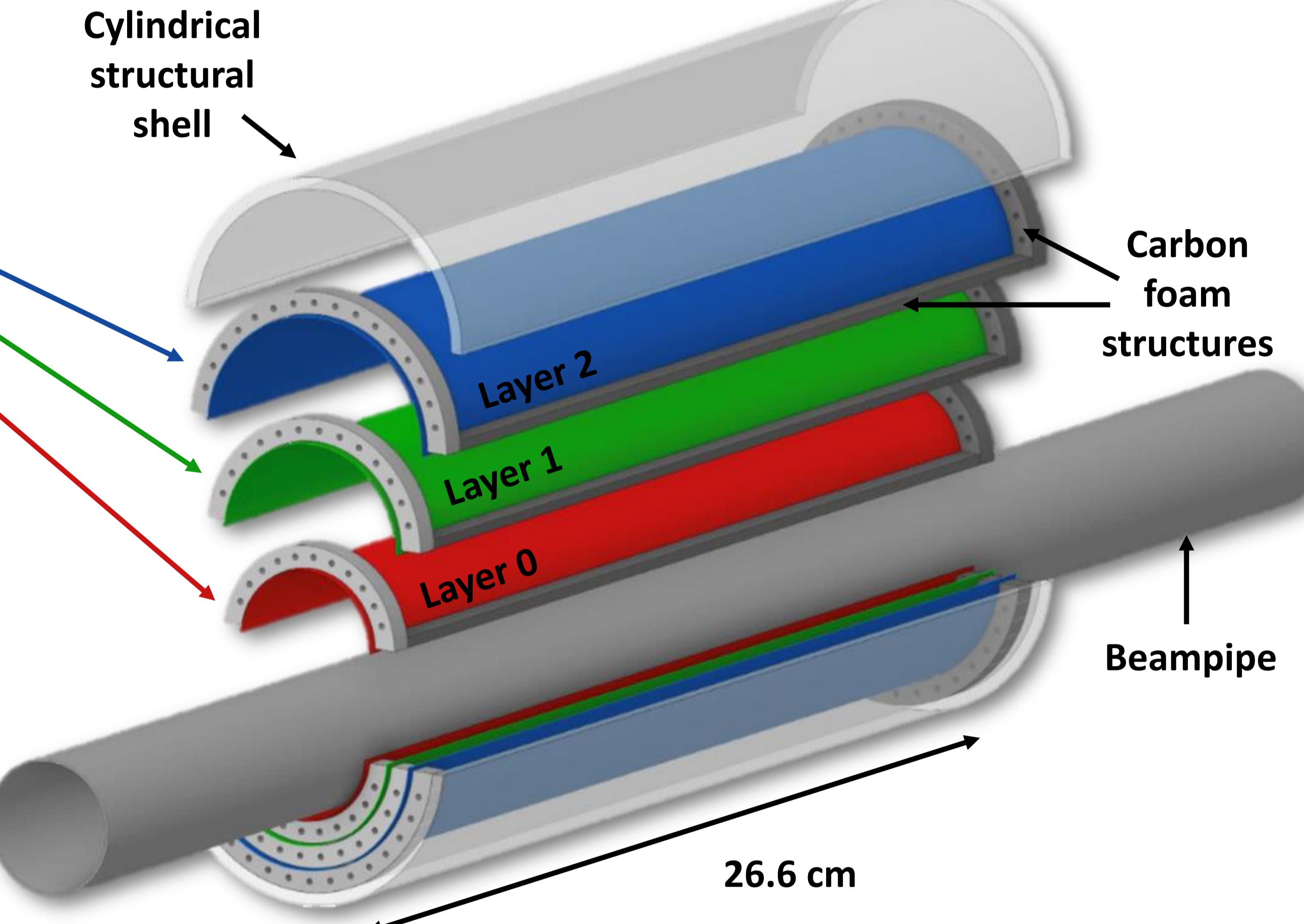
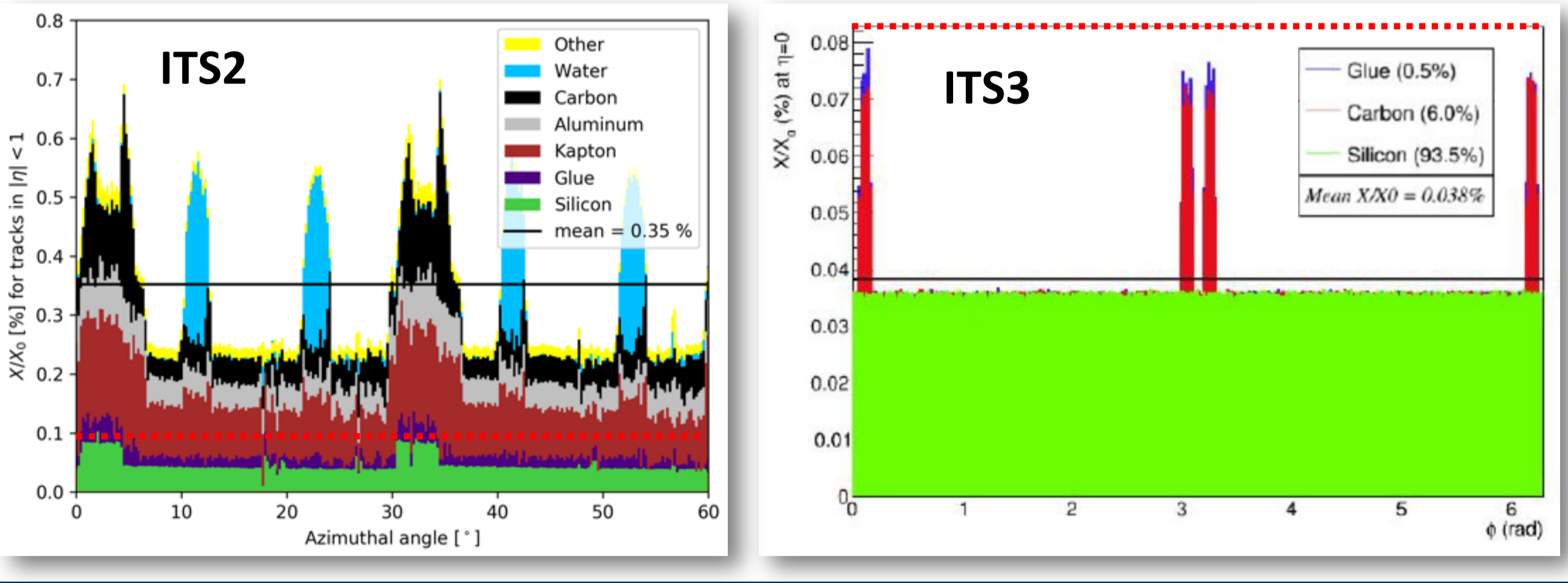
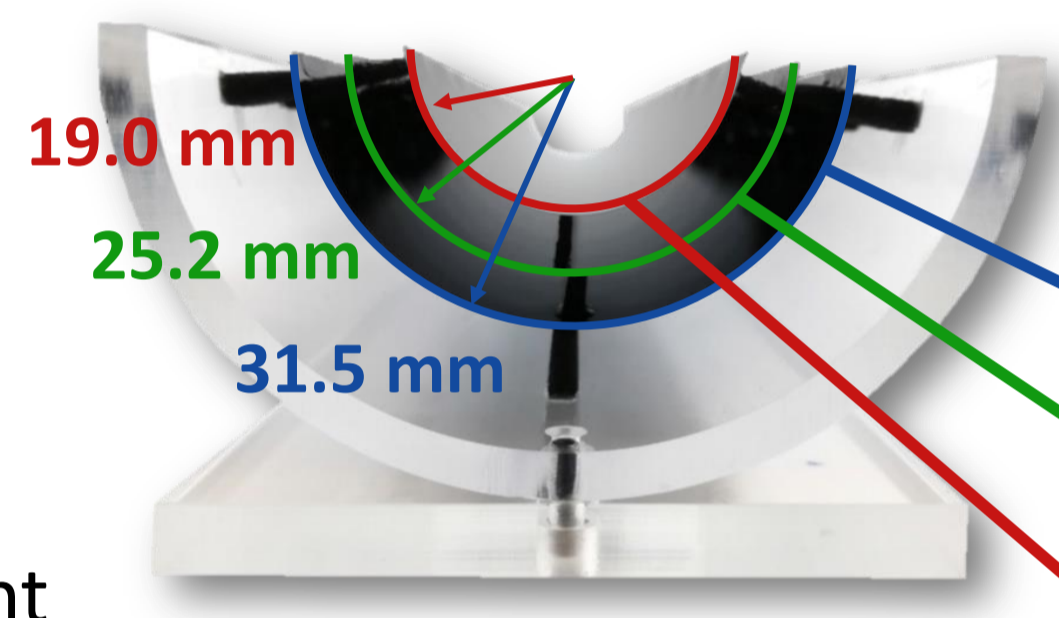


Stitching will be used: repeated identical but functionally independent units, with **in-silicon interconnections** and peripheral structures along the outer edges of the resulting large-area chip.



3. Detector layout

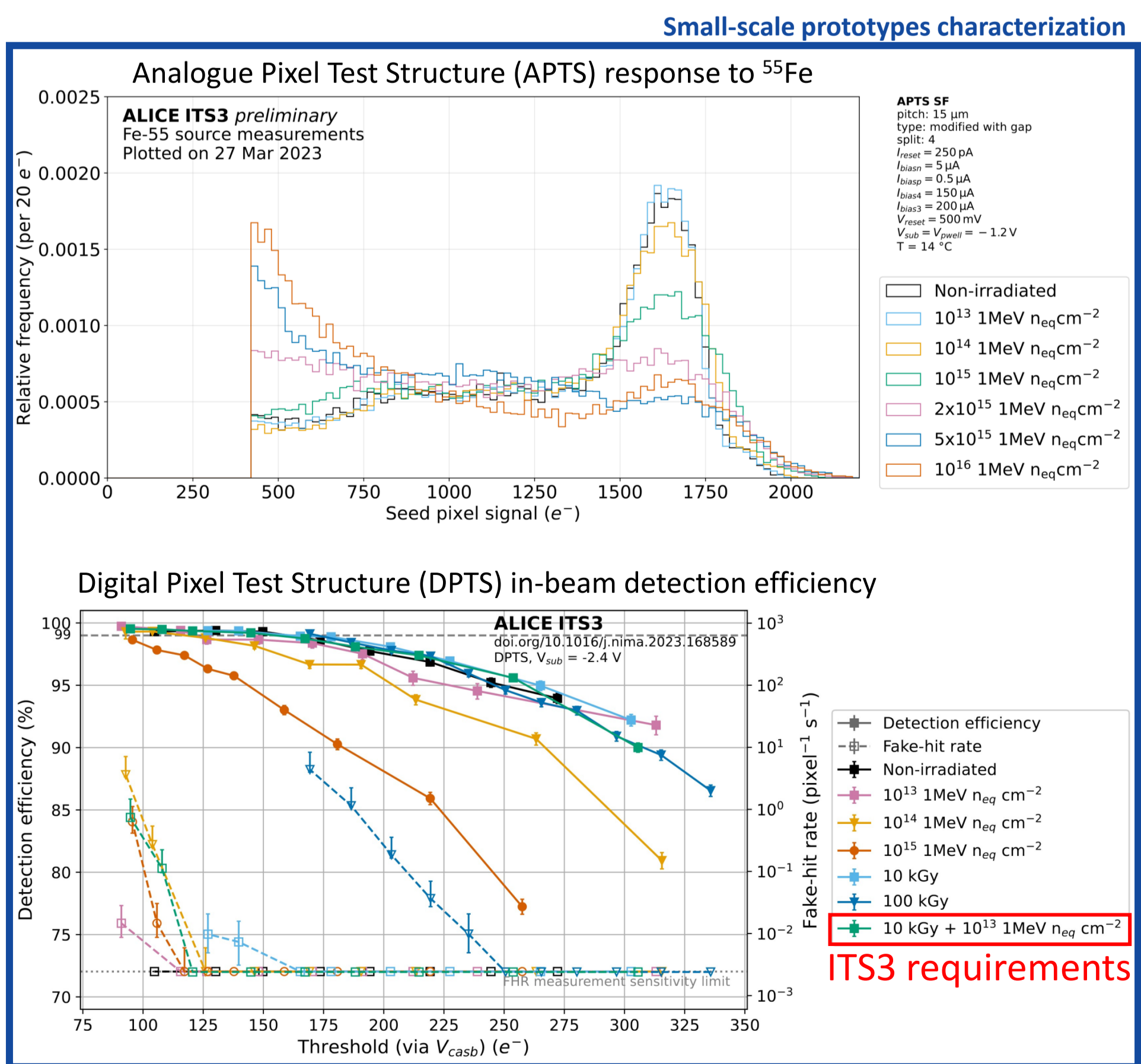
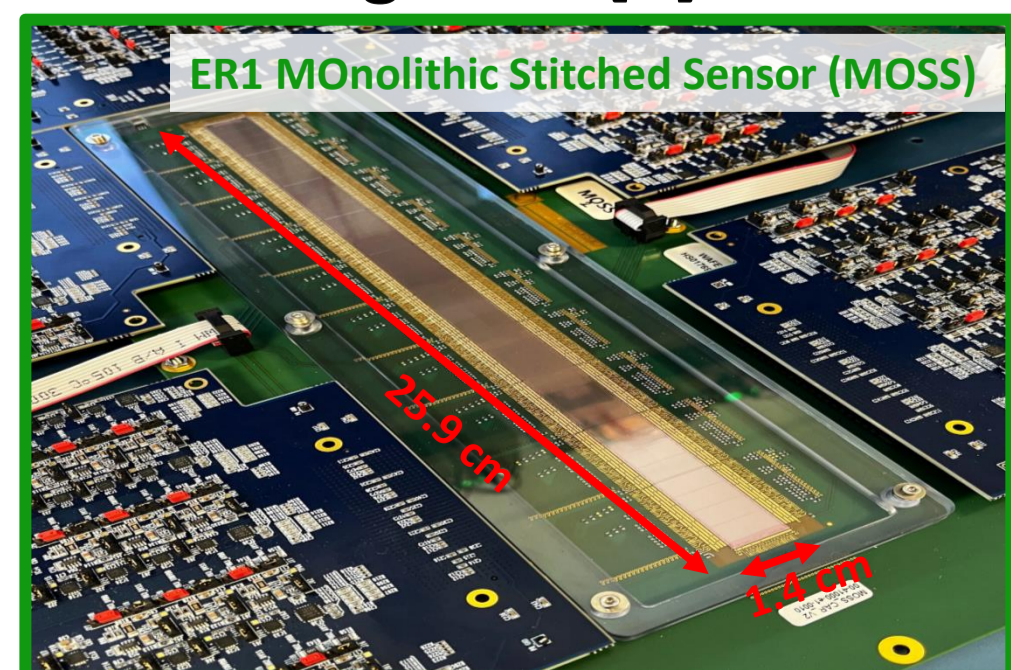
- 3 truly cylindrical **self-supporting** layers
- Each layer made by 2 **flexible MAPS** sensors which:
 - have a **large-area** $O(10 \times 26 \text{ cm}^2)$
 - are **ultra-thin** ($\leq 50 \mu\text{m}$)
- Ultra-light **carbon foam structure** keeps in position the sensors
- Innermost layer at 19 mm** from the interaction point
- Unprecedentedly **low material budget** of 0.07% X_0/layer



4. Sensor qualification

- Characterization of the **small-scale prototypes** realized in the 65 nm technology. First production: Multiple Layer Reticle 1 - MLR1
 - Performance and production yield evaluation** of the **large-area MOlonolithic StItched Sensor (MOSS)**. First production (2023): Engineering Run 1 – ER1
 - Qualification of the **ITS3 final sensor**
- A wide campaign of test is ongoing to qualify both small-scale and large-area prototypes [4, 5].

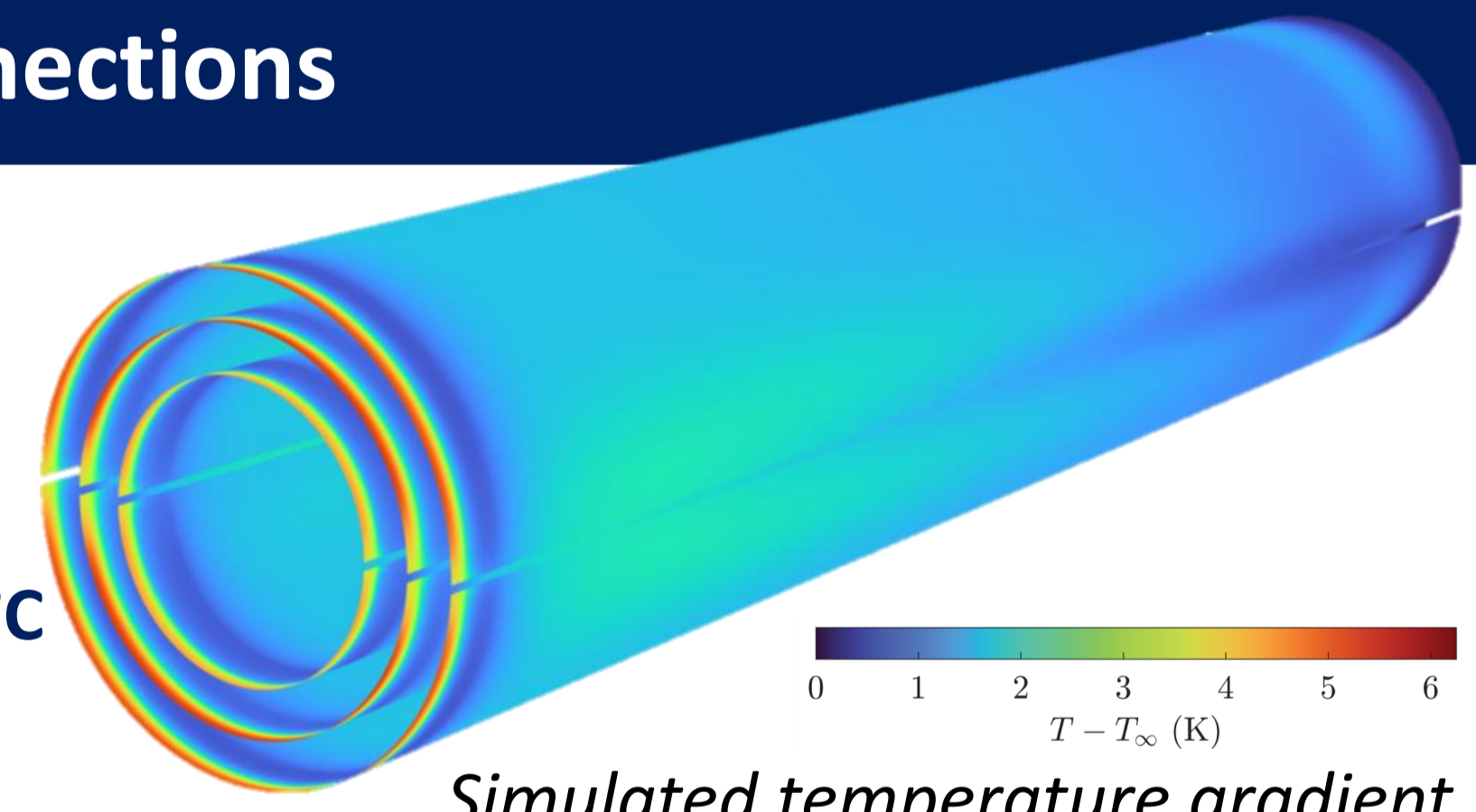
- Laboratory measurements:
 - Definition of the **operating conditions**
 - Response to X-rays:** ^{55}Fe source and fluorescence photons
- In-beam measurements to assess:
 - Detection efficiency**
 - Spatial resolution**
- Bending tests [6]



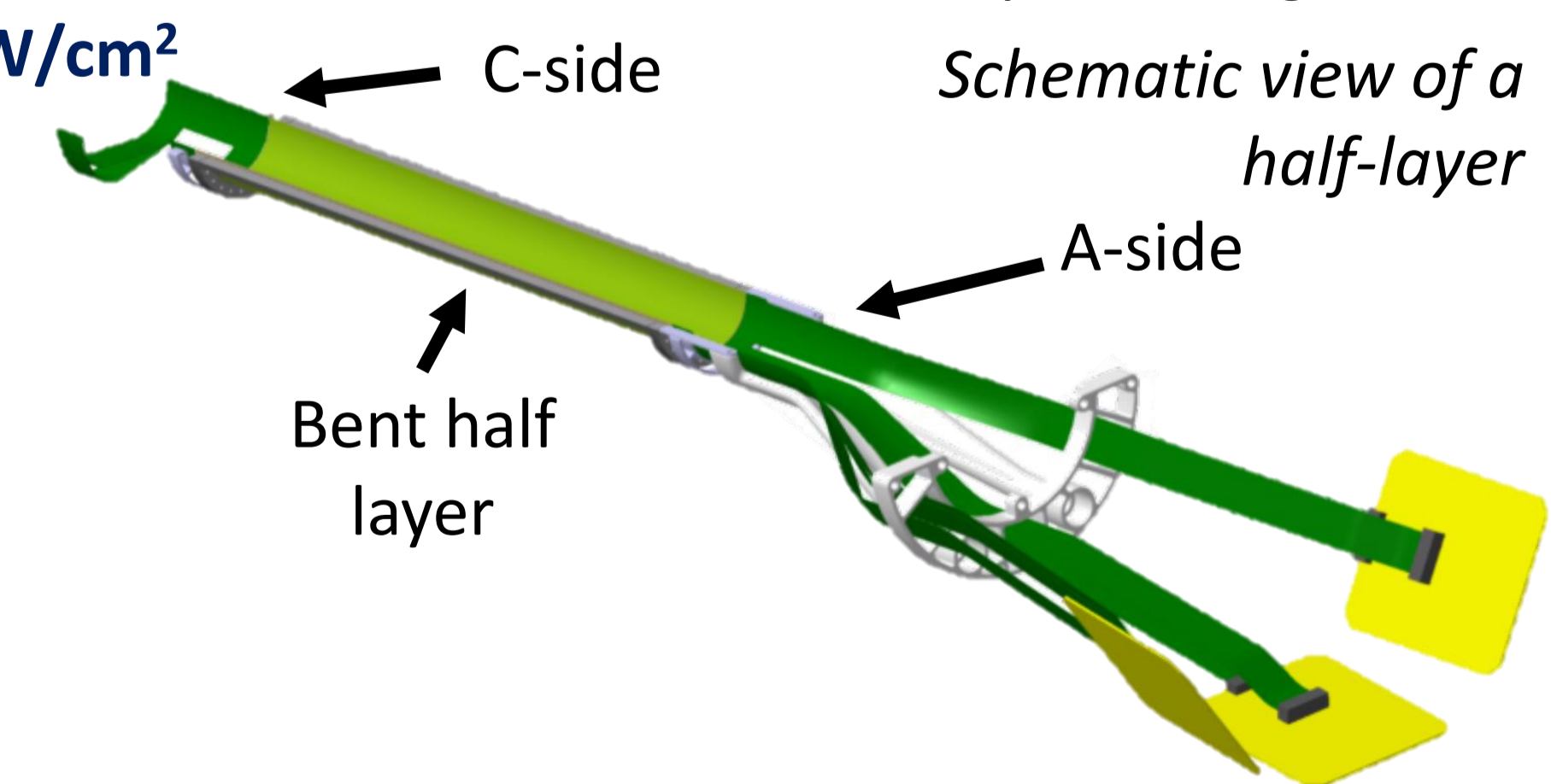
5. Air cooling and interconnections

Air cooling avoids introducing structures in the active region
→ keeps the material budget low

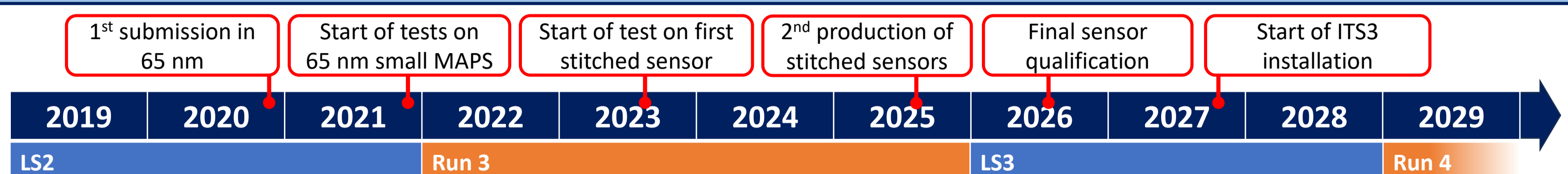
- These requirements must be satisfied:
- Sensor **operating temperature** $< 30^\circ\text{C}$
 - Temperature gradient** in the matrix region $< 5^\circ\text{C}$
 - Sensor **power density** $< 40 \text{ mW/cm}^2$



- The electrical interconnections are on both sides:
- FPC for power on the C-side
 - FPC for power, data and control on the A-side
- Data transmission up to 10 Gb/s



6. Conclusions and outlook



- ITS3 will be installed during LS3 to be ready for LHC Run 4 (2029-2032)
- Sensor qualification on track:
 - Demonstrated operability of bent MAPS
 - Validated 65 nm CMOS process
 - Stitching qualification is ongoing
- Air cooling system and services design is completed, prototyping is ongoing

References
[1] ALICE Collaboration, Letter of Intent for an ALICE ITS Upgrade in LS3, [10.17181/CERN-LHCC-2019-018](https://cds.cern.ch/record/2868015)
[2] Shreyasi Acharya et al., Upgrade of the ALICE Inner Tracking System during LS3: study of physics performance, [http://cds.cern.ch/record/2868015](https://cds.cern.ch/record/2868015)
[3] Tower Semiconductor home page, <https://towersemi.com/>
[4] S. Bugiel et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, <https://doi.org/10.1016/j.nima.2022.167213>
[5] G. Aglieri Rinella, et al., Digital pixel test structures implemented in a 65 nm CMOS process, <https://doi.org/10.1016/j.nima.2023.168589>
[6] ALICE ITS3 project, First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors, <https://doi.org/10.1016/j.nima.2021.166280>