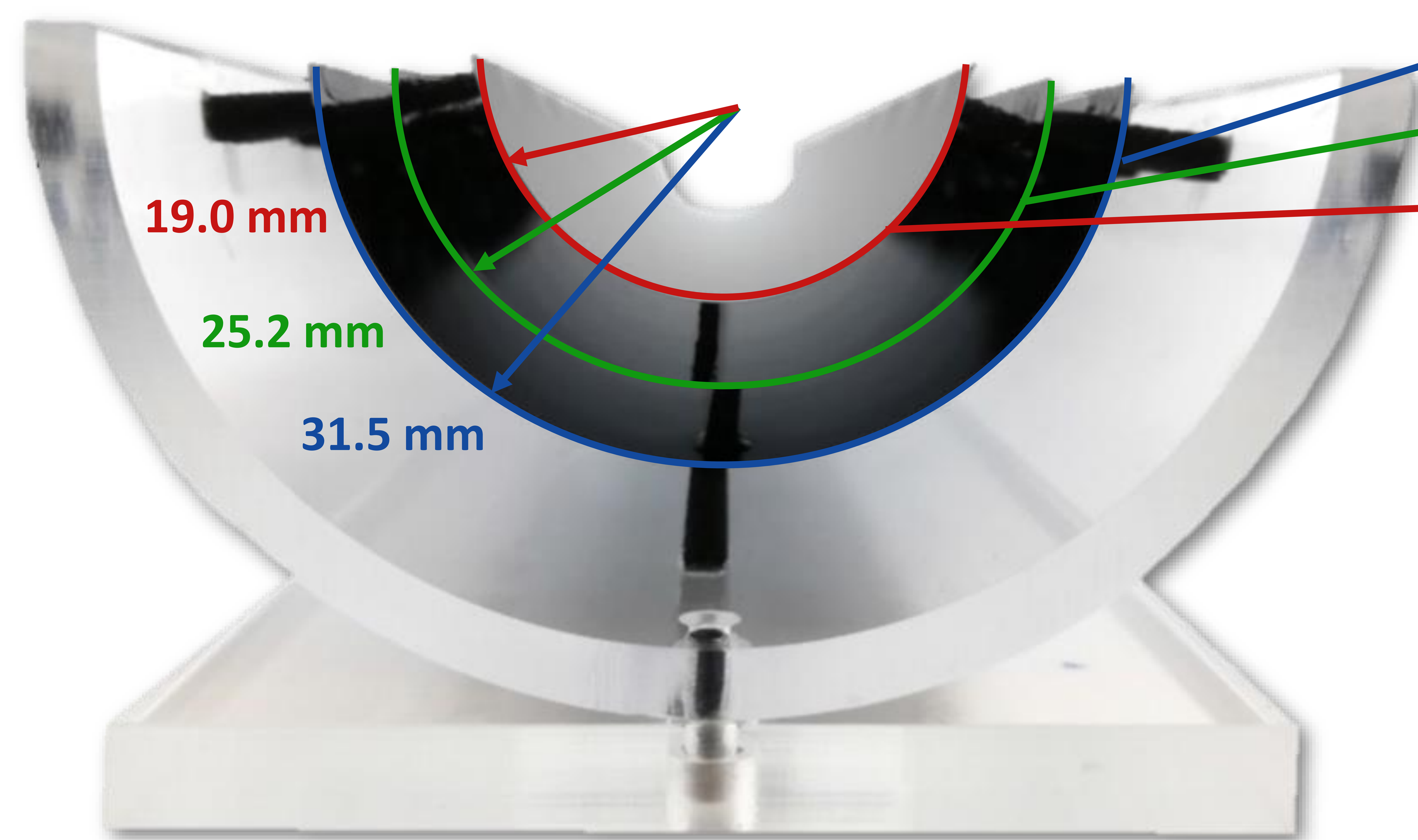
ITS3: The upgrade of the Inner Tracking System of the ALICE Experiment

Anna Villani on behalf of the ALICE Collaboration

60th International Winter Meeting on Nuclear Physics, 22-26 January 2024, Bormio

ITS3: The next ALICE Inner Tracking System

1. Physics motivation
2. Monolithic Active Pixel Sensor (MAPS) technology
3. Detector layout
4. Sensor qualification
5. Air cooling and interconnections



Cylindrical structural shell

Carbon foam structures

MAPS layer 2

MAPS layer 1

MAPS layer 0

Beampipe

26.6 cm

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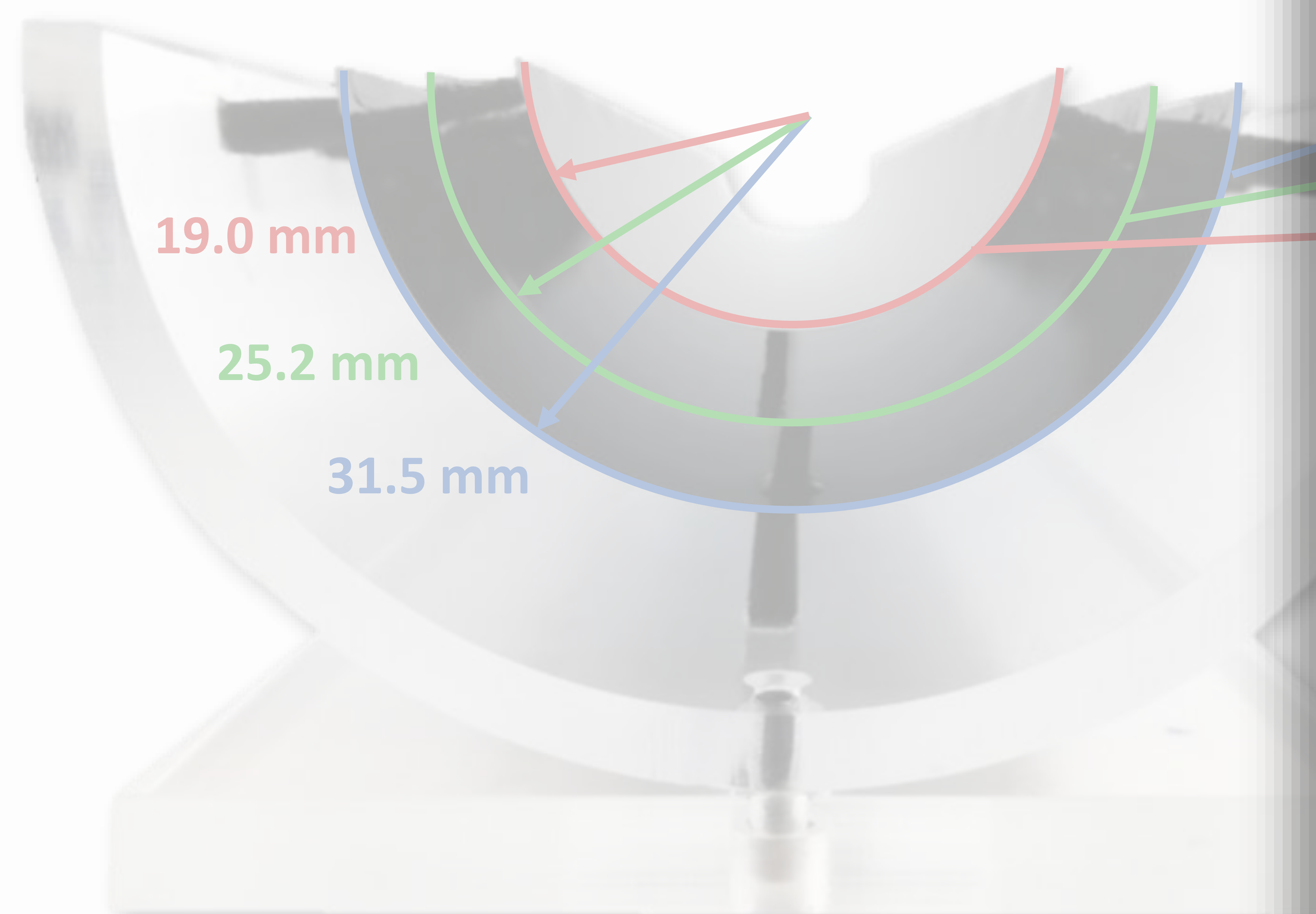

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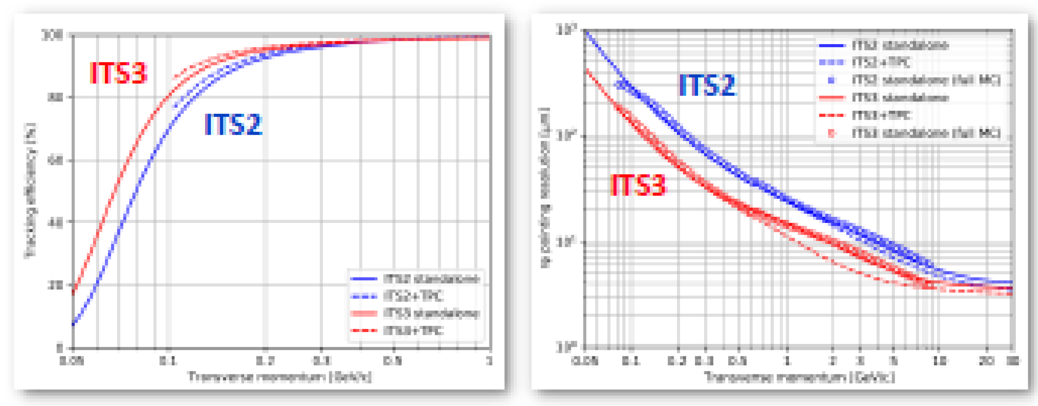
1. Physics motivation

- The innermost layers of the ALICE Inner Tracking System (ITS2) will be replaced with a new tracker during LHC Long Shutdown 3 (2026-2028), the ITS3 [1].
- This upgrade will further improve tracking efficiency and pointing resolution especially for low momentum particles, thus allowing to improve the precision of measurements in the heavy-flavour sector and to bring another set of fundamental observables into reach [2].
- E.g. these measurements will be allowed:
  - B^0_s and Λ^0_b at low transverse momenta
  - Non-prompt D^+_s and Ξ^+_c decays in heavy-ion collisions



2. Monolithic Active Pixel Sensor (MAPS) technology

The ITS3 will be realized using the MAPS technology:

- Read-out logic and sensitive volume in the same silicon crystal
- Complete in-pixel CMOS circuitry
- Ultra-thin silicon O(≤50 μm)

The Tower Partners Semiconductor Co. [3] 65 nm CMOS imaging process for MAPS was chosen for the ALICE ITS3. Key advantages:

- High radiation hardness
- Low power consumption
- 5 μm 2D spatial resolution
- Large wafers (Ø 300 mm)

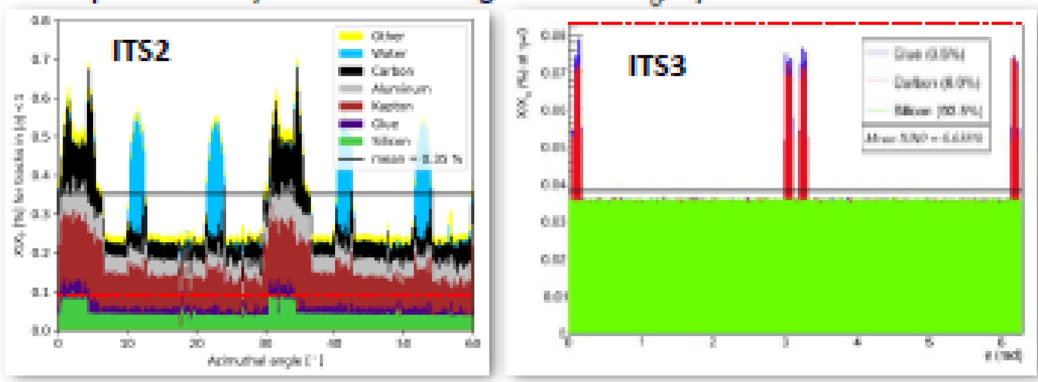
4 MAPS pixels

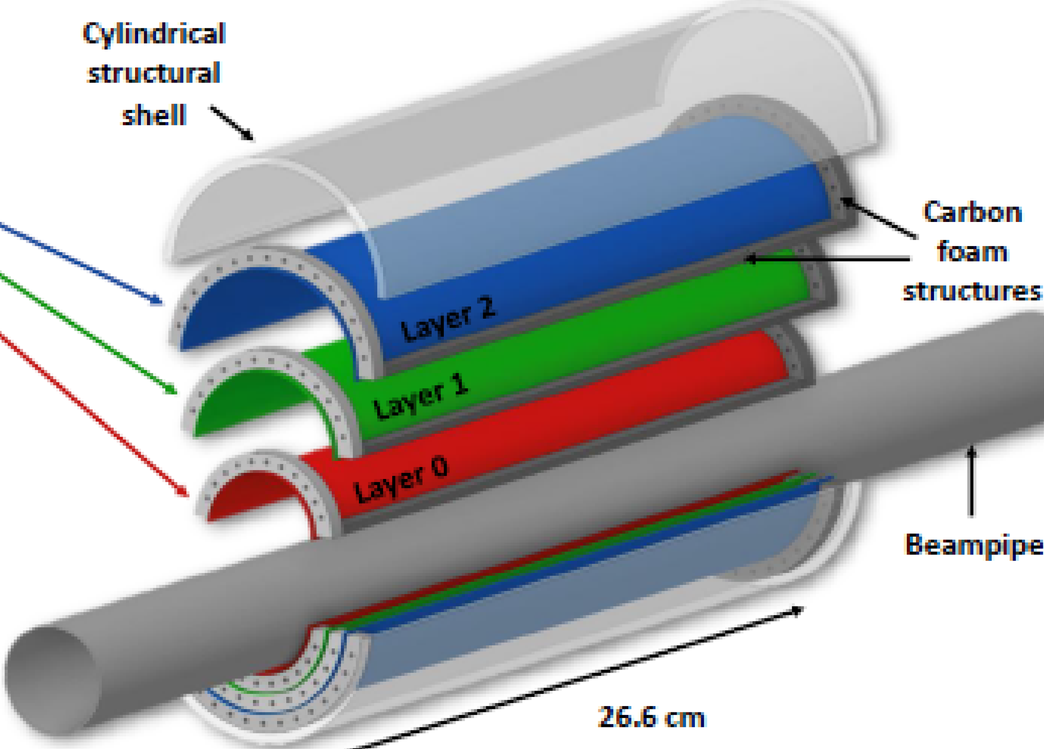
Stitching will be used: repeated identical but functionally independent units, with in-silicon interconnections and peripheral structures along the outer edges of the resulting large-area chip.

Schematic view of a Monolithic Stitched Sensor (MOSS)

3. Detector layout

- 3 truly cylindrical self-supporting layers
- Each layer made by 2 flexible MAPS sensors which:
  - have a large-area O(10×26 cm²)
  - are ultra-thin (≤50 μm)
- Ultra-light carbon foam structure keeps in position the sensors
- Innermost layer at 19 mm from the interaction point
- Unprecedentedly low material budget of 0.07% X_0/layer



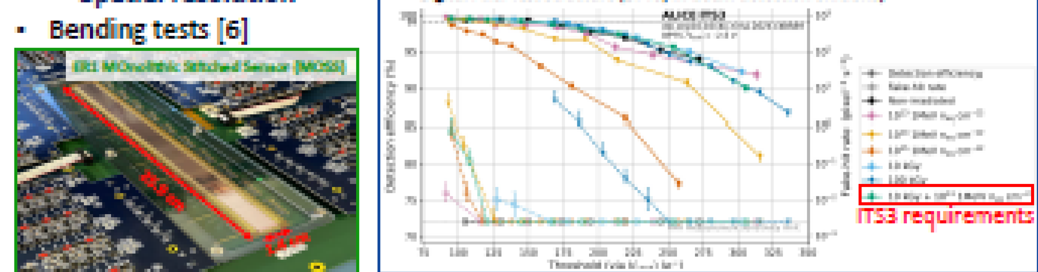


4. Sensor qualification

1. Characterization of the small-scale prototypes realized in the 65 nm technology. First production: Multiple Layer Reticle 1 - MLR1
2. Performance and production yield evaluation of the large-area MOnolithic Stitched Sensor (MOSS). First production (2023): Engineering Run 1 – ER1
3. Qualification of the ITS3 final sensor

A wide campaign of test is ongoing to qualify both small-scale and large-area prototypes [4, 5].

- Laboratory measurements:
  - Definition of the operating conditions
  - Response to X-rays: ^{55}Fe source and fluorescence photons
- In-beam measurements to assess:
  - Detection efficiency
  - Spatial resolution
- Bending tests [6]



5. Air cooling and interconnections

Air cooling avoids introducing structures in the active region
→ keeps the material budget low

These requirements must be satisfied:

- Sensor operating temperature <30°C
- Temperature gradient in the matrix region <5°C
- Sensor power density < 40 mW/cm²

Simulated temperature gradient

The electrical interconnections are on both sides:

- FPC for power on the C-side
- FPC for power, data and control on the A-side

Data transmission up to 10 Gb/s

Schematic view of a half-layer

C-side
A-side
Bent half layer

6. Conclusions and outlook

2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029

- ITS3 will be installed during LS3 to be ready for LHC Run 4 (2029-2032)
- Sensor qualification on track:
  - Demonstrated operability of bent MAPS
  - Validated 65 nm CMOS process
  - Stitching qualification is ongoing
- Air cooling system and services design is completed, prototyping is ongoing

References
[1] ALICE Collaboration, Letter of Intent for an ALICE ITS Upgrade in LS3
[2] Upgrade of the ALICE Inner Tracking System during LS3: study of physics performance
[3] Tower Semiconductor home page
[4] … Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology
[5] … Digital pixel test structures implemented in a 65 nm CMOS process
[6] ALICE ITS3 project, First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors