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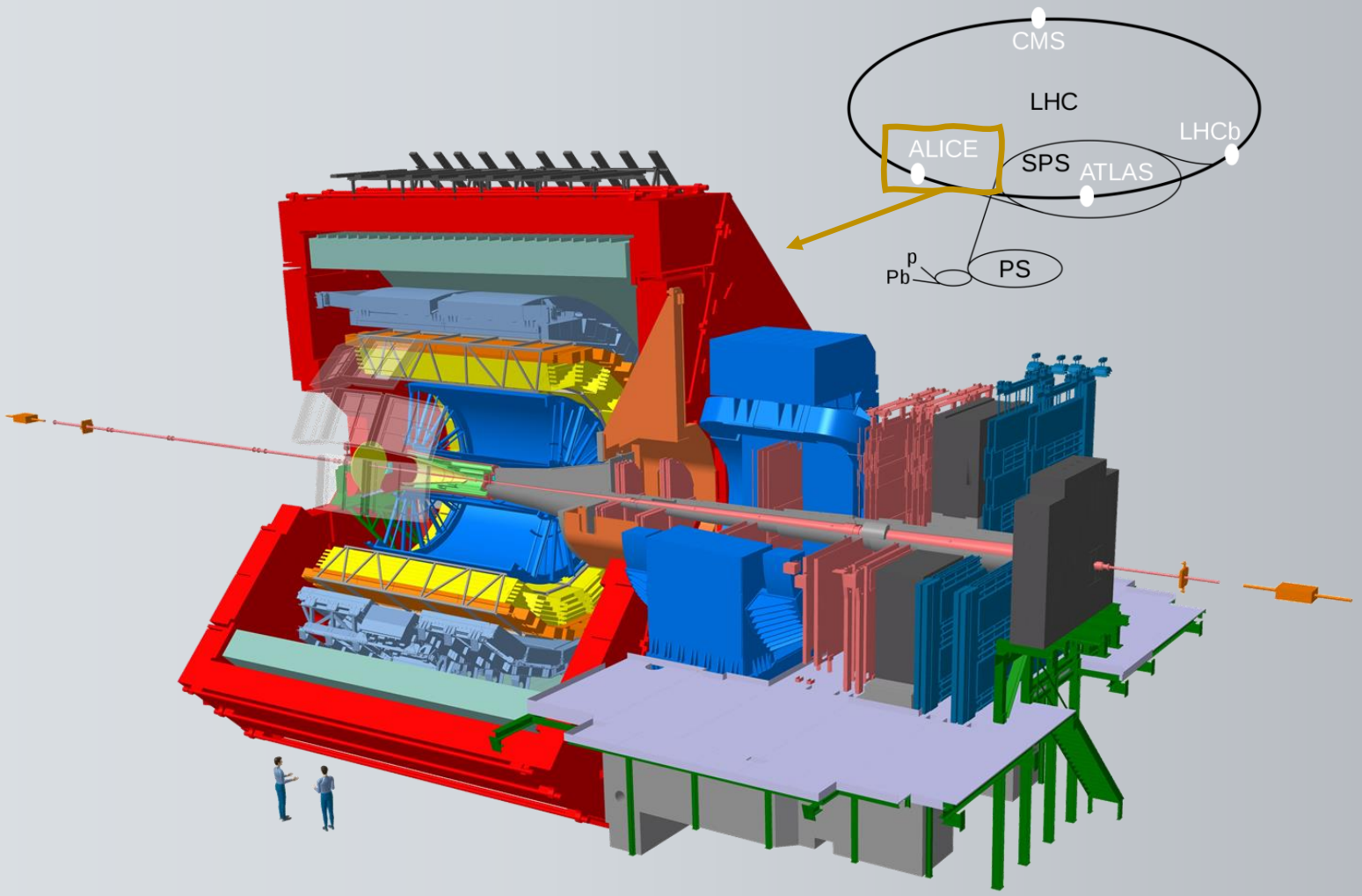
THE ITS3 UPGRADE OF THE ALICE INNER TRACKING SYSTEM

Paola La Rocca *
on behalf of the ALICE Collaboration

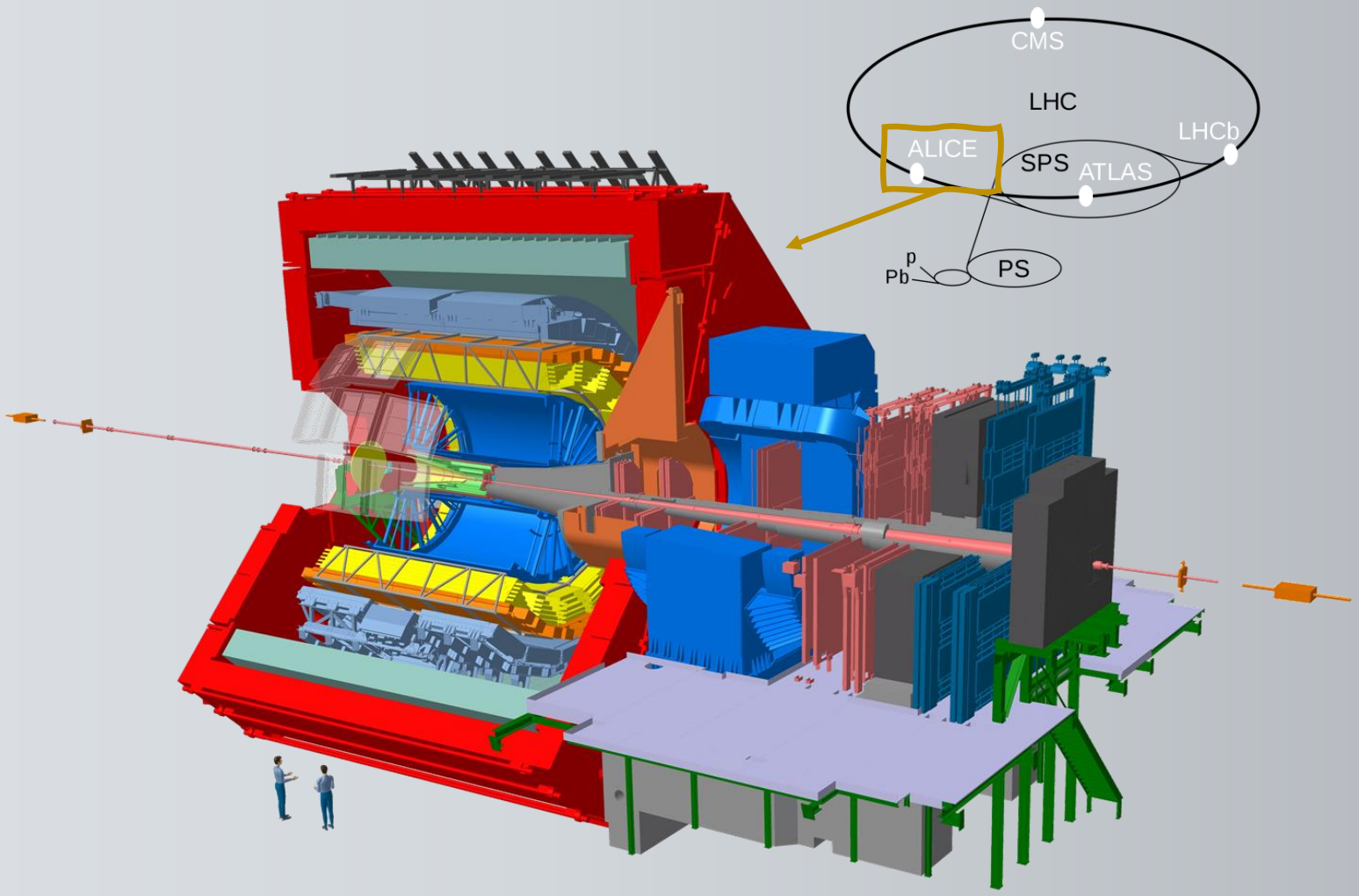
* INFN and University Catania

The ALICE experiment



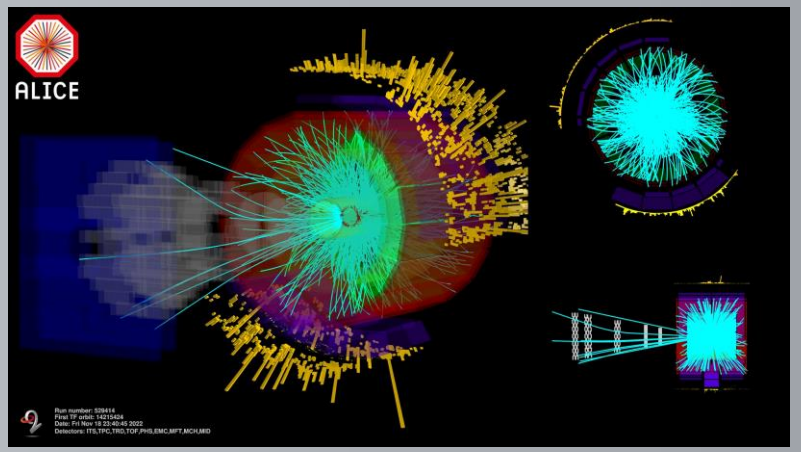
Study of quark-gluon plasma (**QGP**) in the collisions of nuclei at the LHC

The ALICE experiment

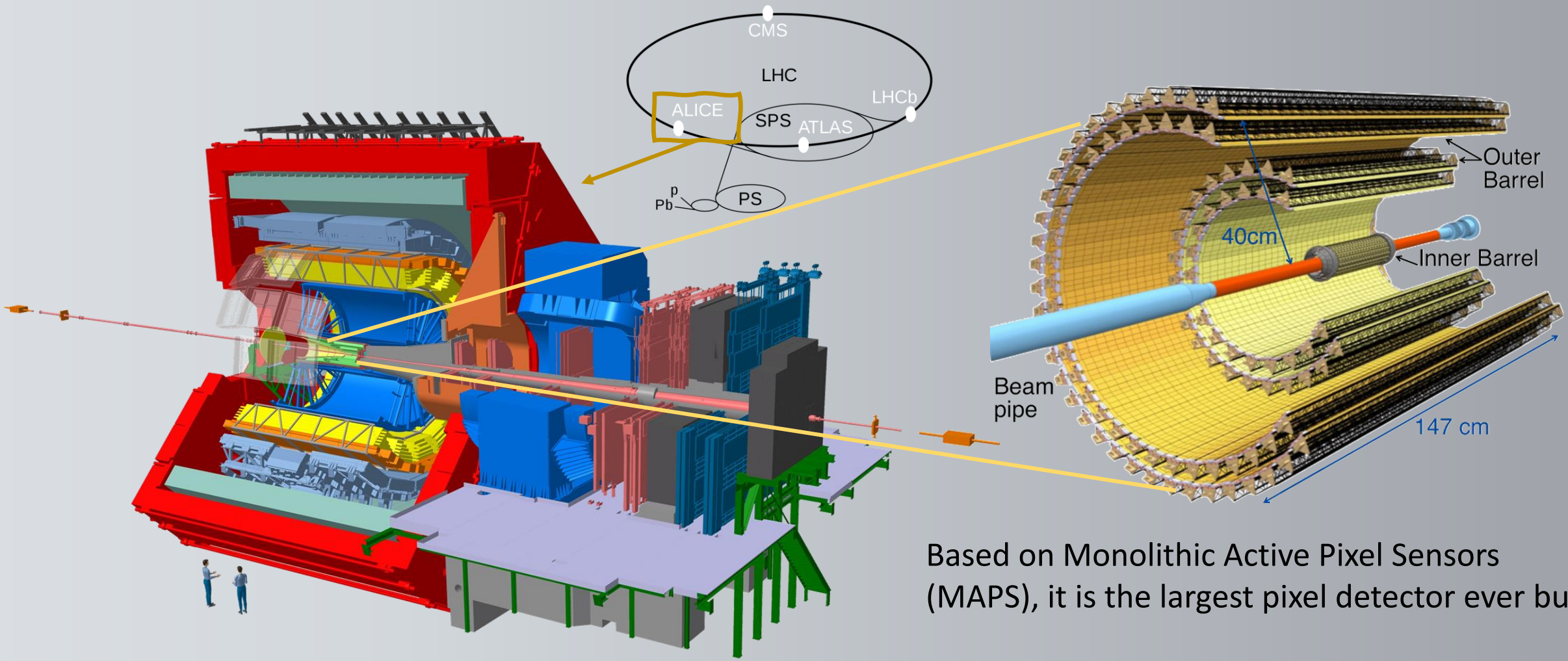


Study of quark-gluon plasma (**QGP**) in the collisions of nuclei at the LHC

- Thousands of particles produced in each event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum ($\lesssim$1 GeV/c) particle reconstruction

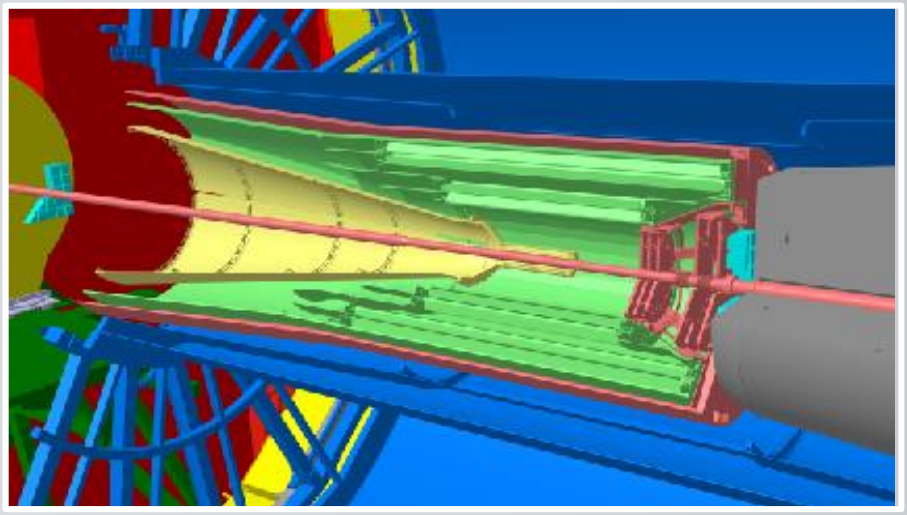


Current Inner Tracking System (ITS2)



Based on Monolithic Active Pixel Sensors (MAPS), it is the largest pixel detector ever built

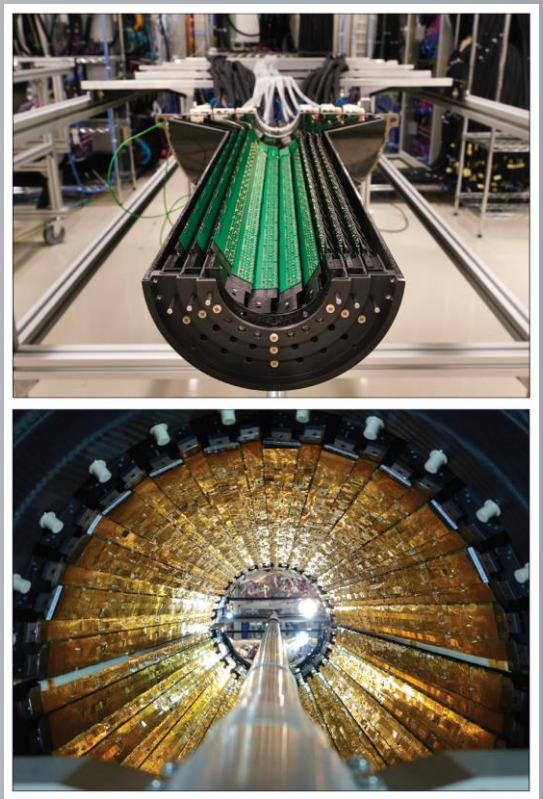
Current Inner Tracking System (ITS2)



- Result of ~ 10 years of R&D and C&I
- Installed during the LHC LS2

7 layers:
all MAPS 10 m², 24k chips, 12.5 Giga-pixels

Inner-most layer:
radial distance: 23 mm
material: $X/X_0 = 0.35\%$
Pixel size : 29 × 27 µm²
Rate capability: 100 kHz (Pb-Pb)
Cooling: water
Run 3/4



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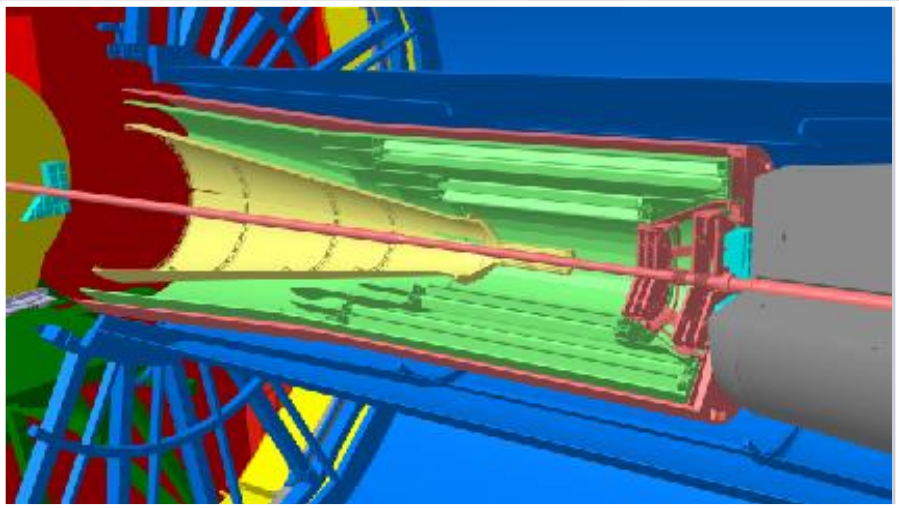

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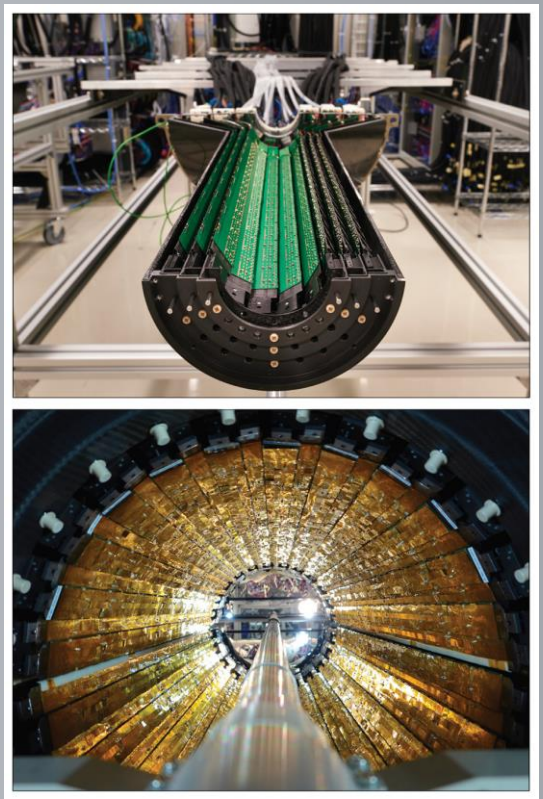
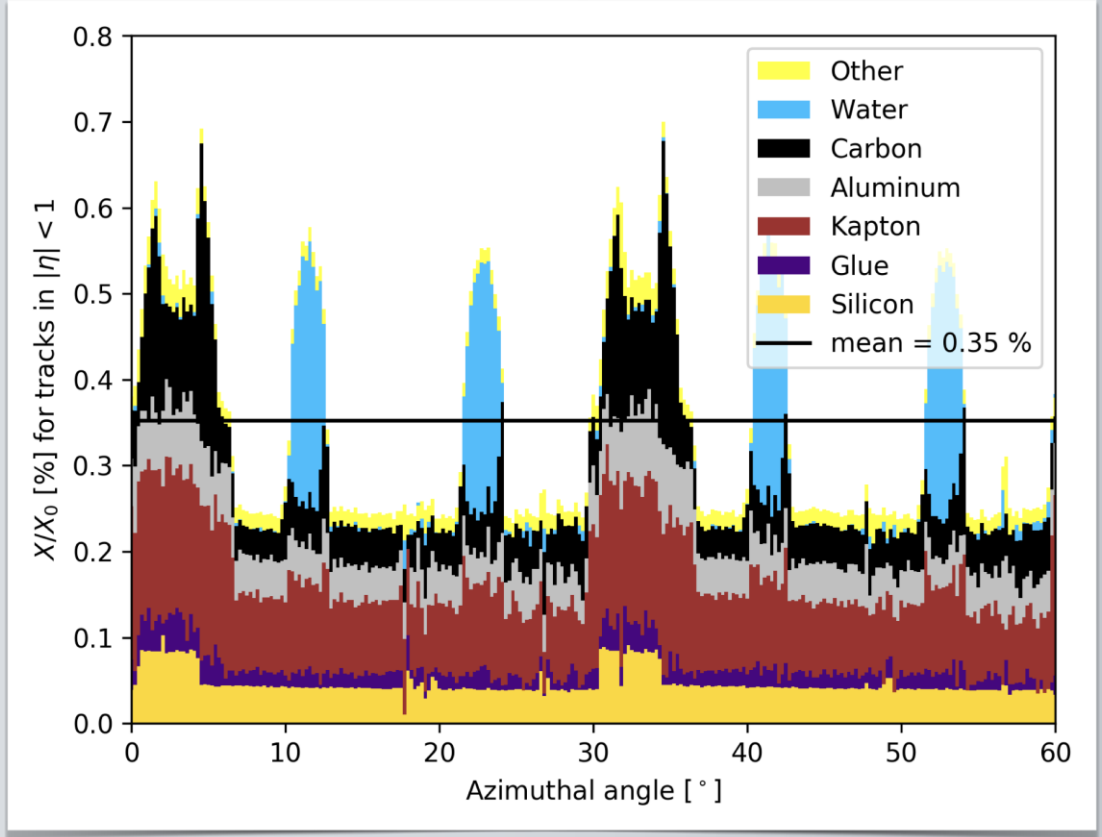


Further improvements?
ITS3: upgrade of the ITS2 innermost layers, to be installed during LHC LS3

Further improvements still possible?

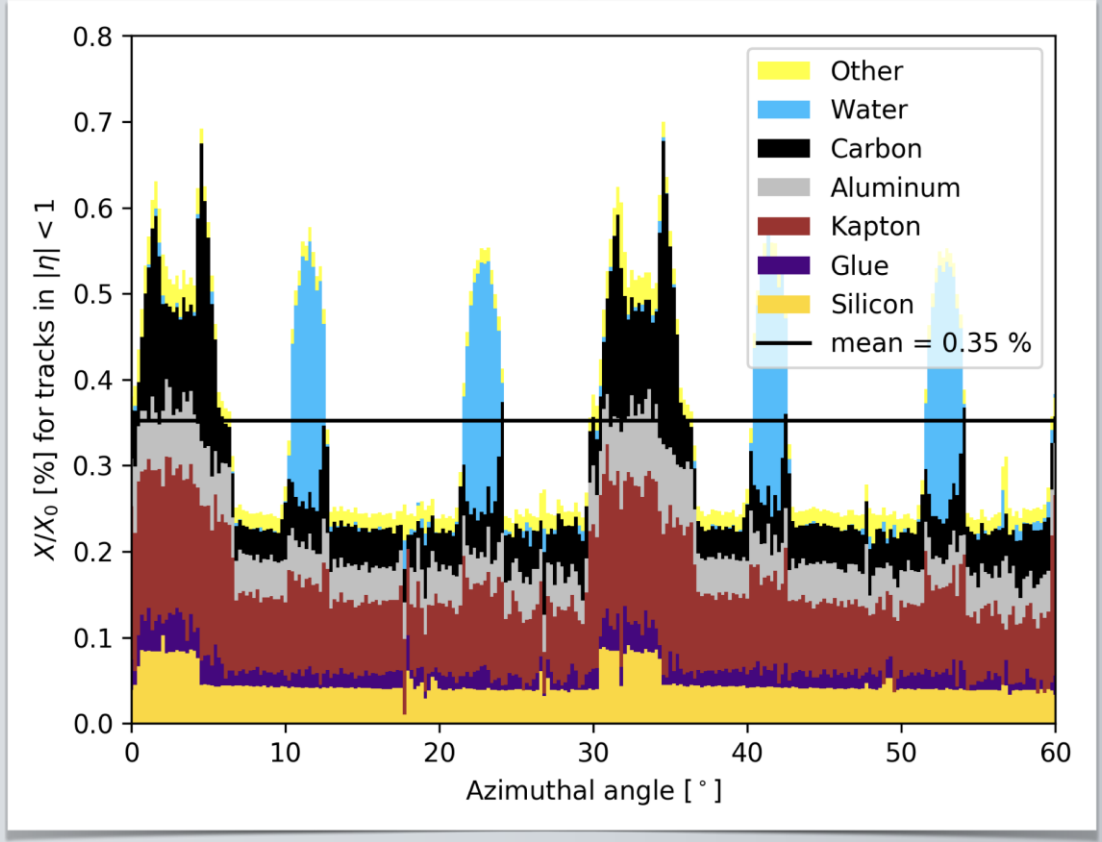
The ITS2 Inner Barrel is ultra-light (0.35% X_0 per layer) but…



- Most of the material comes from passive components (such as water cooling, carbon and kapton support structures, and aluminum wires)
- Lot of irregularities
- Silicon contributes only about 15% of the total material budget

Further improvements still possible?

WHAT IF…



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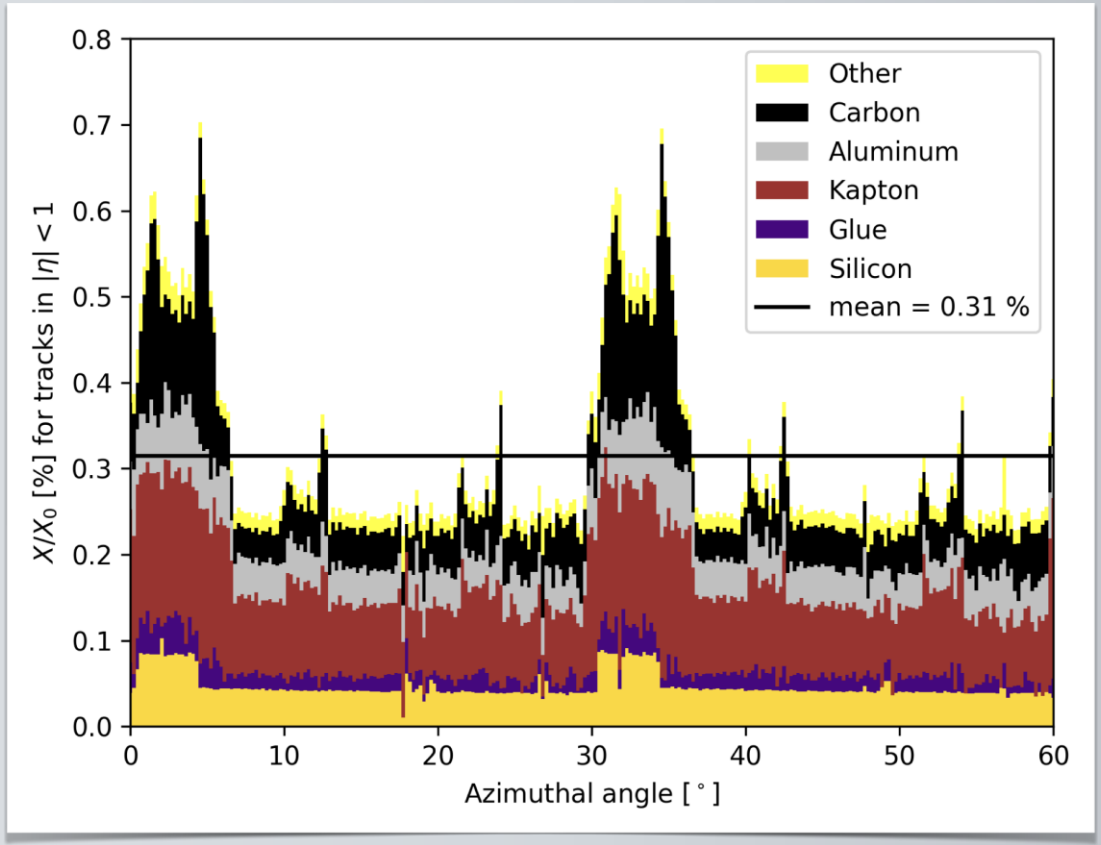

Water cooling is removed

- Possible if power consumption stays below 20 mW/cm^2
- Air cooling
- 0.31% X_0 per layer

Further improvements still possible?

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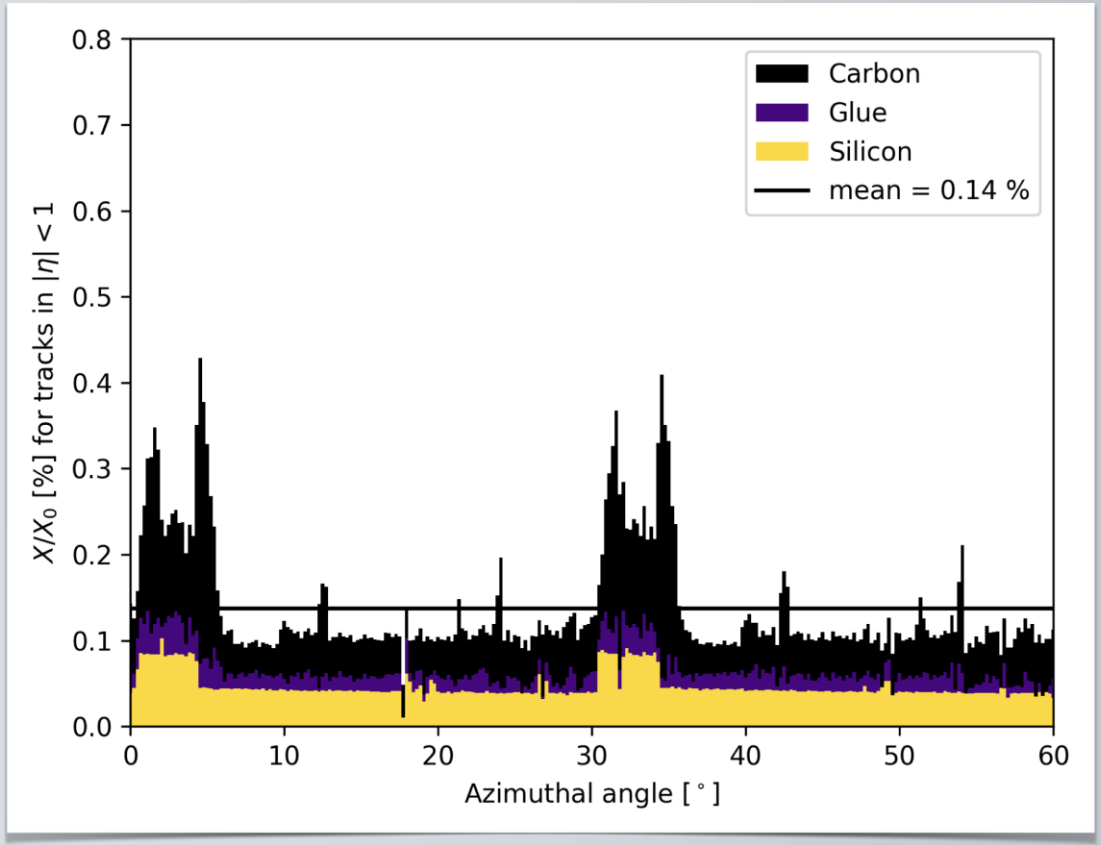

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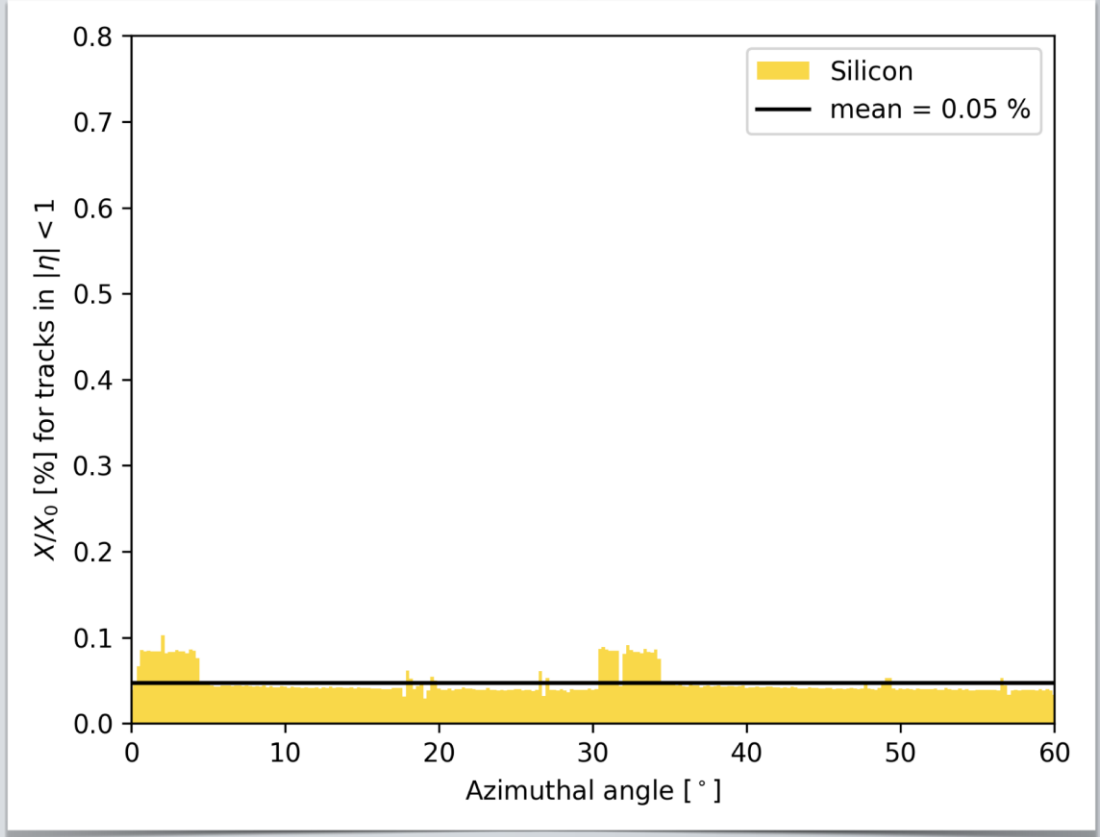
Circuit boards (power and data) are removed

- Possible if integrated on Silicon sensors
- 0.14% X_0 per layer

Further improvements still possible?

WHAT IF…



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Circuit boards (power and data) are removed

- Possible if integrated on Silicon sensors
- 0.14% X_0 per layer

Mechanical structure is removed

- Stability due to bent Silicon wafers
- 0.05% X_0 per layer

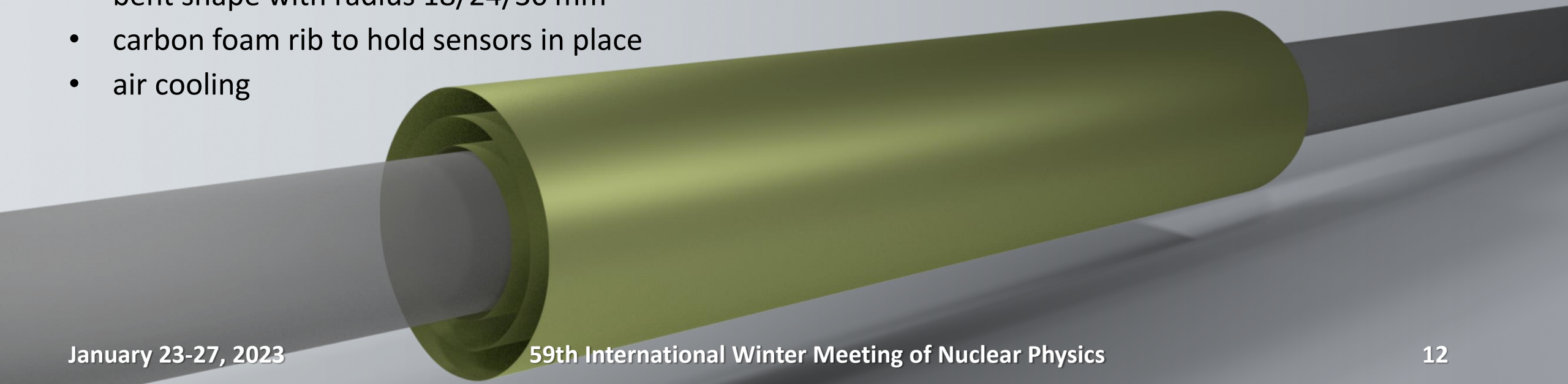
The ITS3 Project

Replace inner 3 layers of ITS2 with ITS3, by employing wafer-scale bent sensors

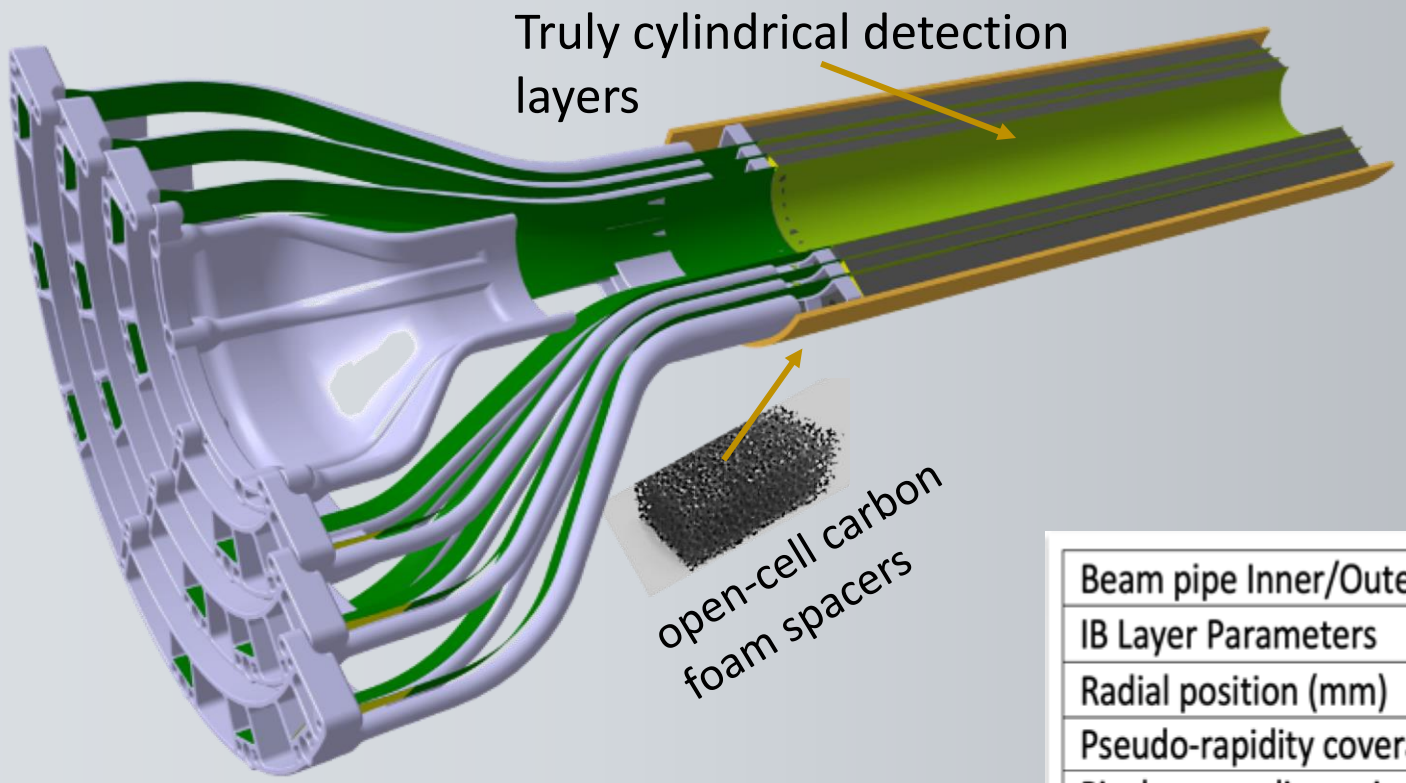
- Reduction of material budget (~ factor 7) and homogenous material distribution
- First layer closer to the interaction point

KEY INGREDIENTS:

- 300 mm wafer-scale sensors, fabricated using stitching
- thinned down to 20-40 µm (0.02-0.04% X_0) → flexible
- bent shape with radius 18/24/30 mm
- carbon foam rib to hold sensors in place
- air cooling



ITS3 specifications and layout

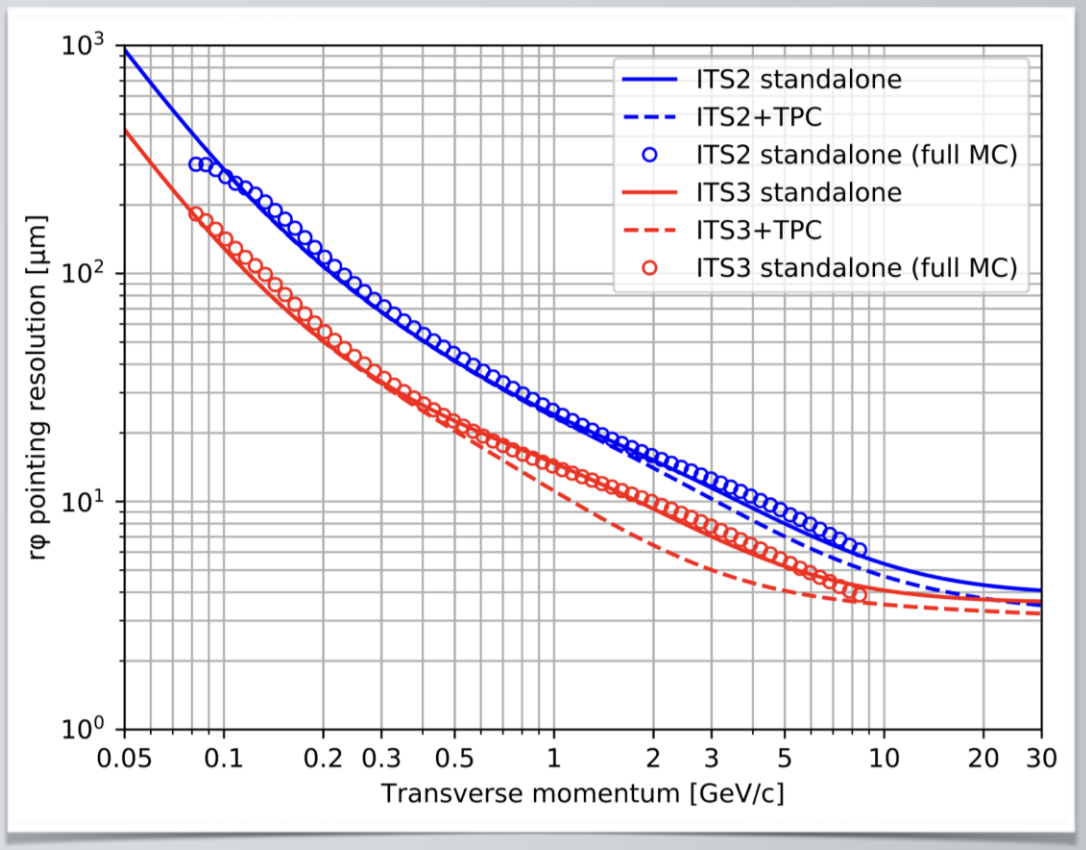


The whole detector will consist of six sensors (2 halves x 3 layers) and barely anything else (current ITS IB: 432 sensors)

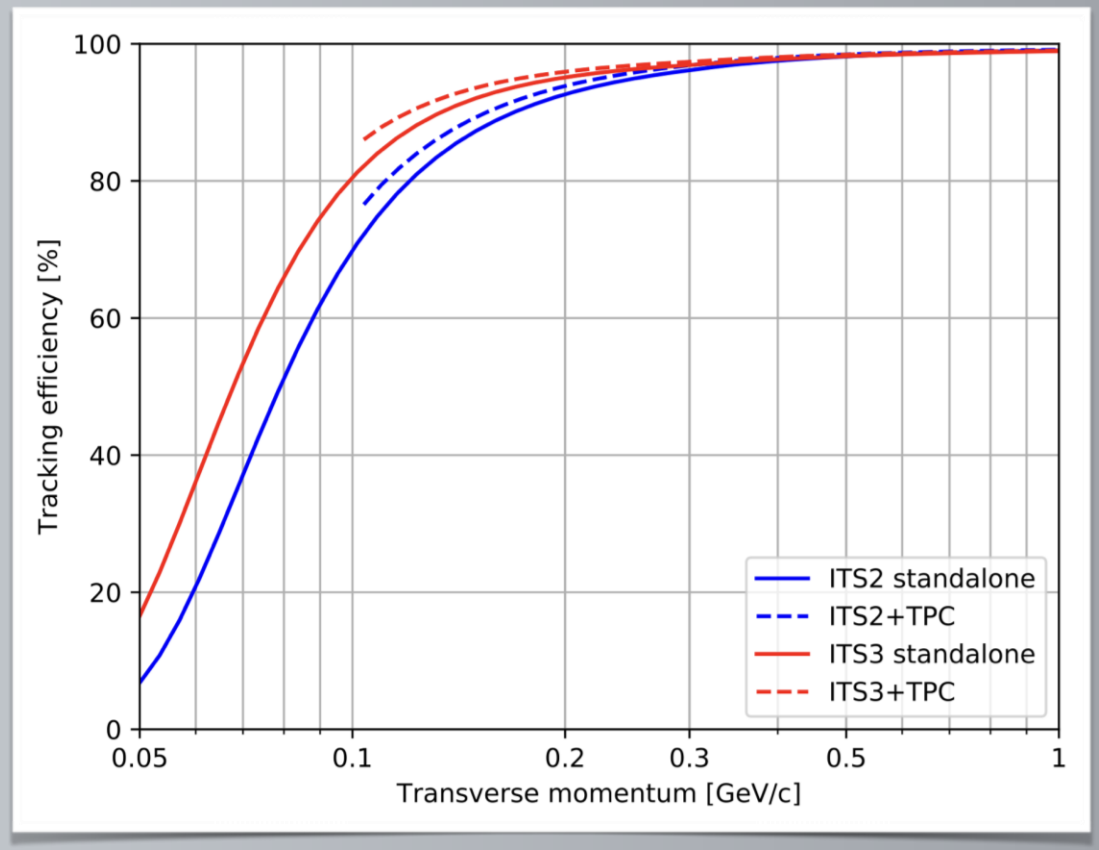
R&D started in Dec 2019

Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (20 x 20)		

ITS3 performance



Improvement of factor 2 for $p_T \approx 1$GeV/c



Large improvement for low transverse momenta

ITS3 impact on physics

Low momentum charm and beauty hadrons

- Better secondary vertex reconstruction, increased efficiency also helps in multi-prong decays

Low-mass dielectrons

- Less conversion, better low-pT standalone efficiency to reconstruct and reject conversions, better rejection of charm-decay electrons

Beauty-strange mesons

- Exclusive reconstruction of B^0_S, non-prompt D^+_S

Beauty baryons (non-prompt Λ^0_C, exclusive reconstruction of Λ^0_B)

Charm strange and multi-strange baryons (Ξ^0_C (cds), Ξ^+_C (cus), Ω^0_C (css))

Searches for light charm hypernuclei

- Bound state of a Λ^+_c and a neutron (c-deuteron), bound state of a Λ^+_c and a deuteron (c-triton)

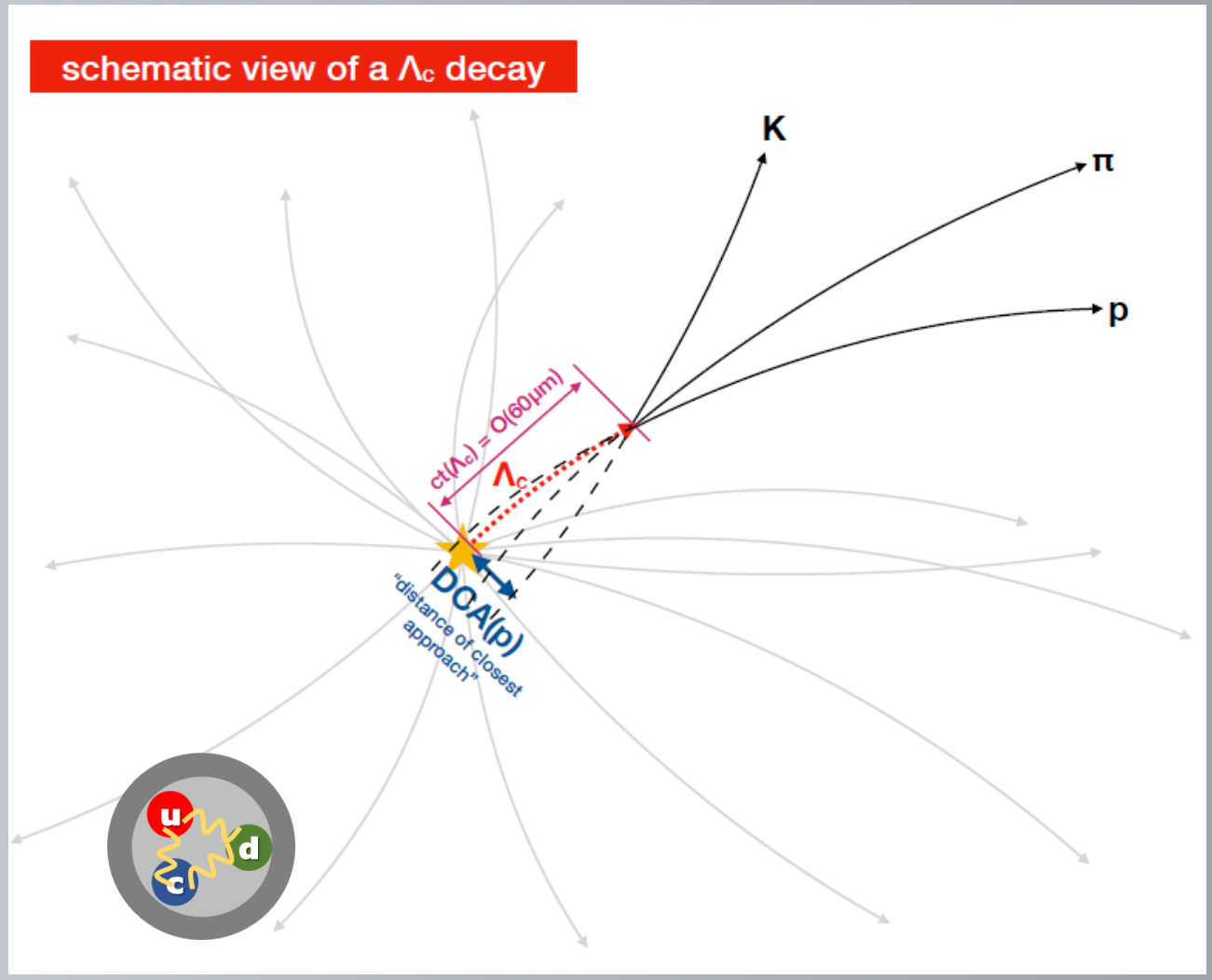
Measurement of Lamba-c (Λ_c)

In heavy-ion collisions the production of charm and beauty baryons is expected to be significantly enhanced:

- recombination with light-flavour quarks present inside QGP
- hadron-mass-dependent radial collective flow

However current results have limited statistical precision!

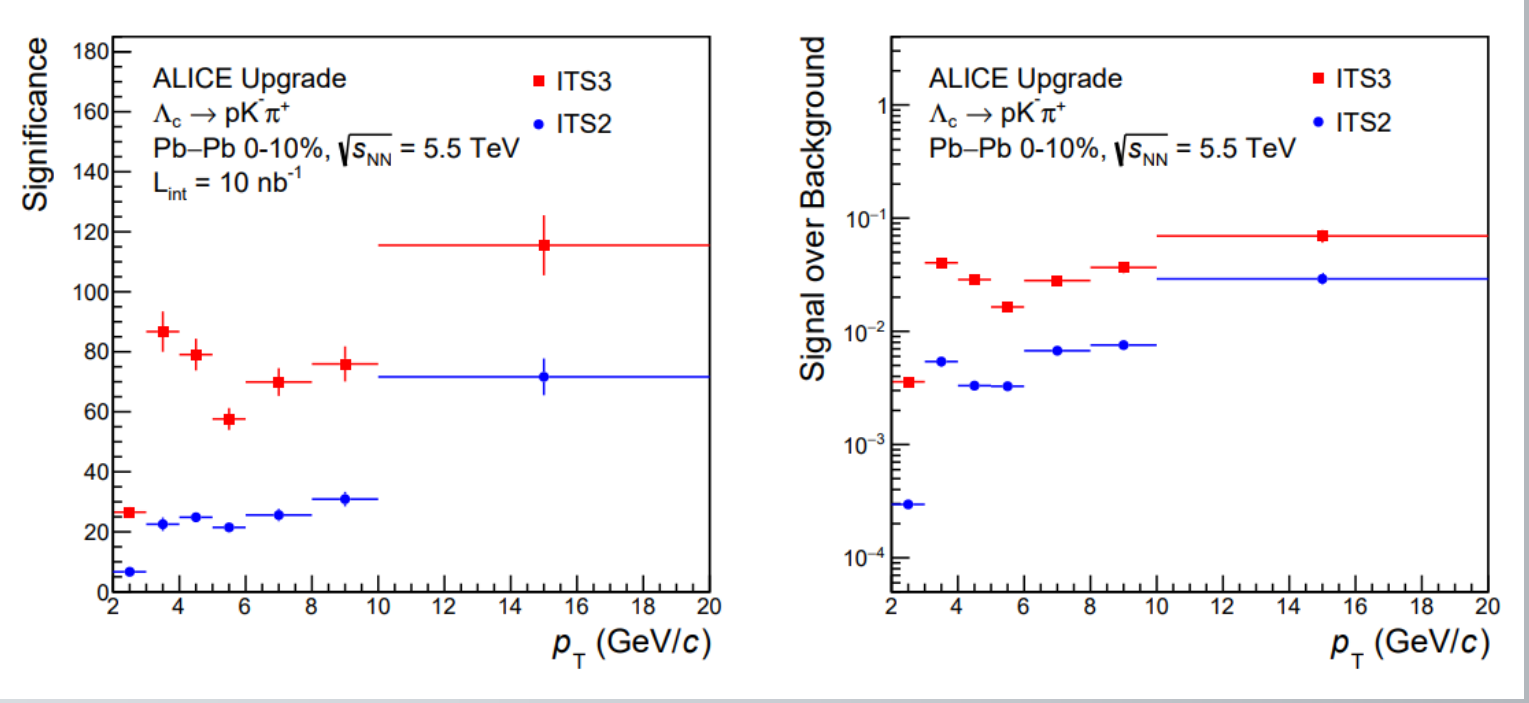
The measurement requires very precise tracking and impact parameter resolution



Measurement of Lamba-c (Λ_c)

Large improvement (wrt to ITS2) of significance (factor 4) and *S/B* ratio (10), thanks to:

- better pointing resolutions → larger rejection of the combinatorial background
- larger efficiency for the signal selection



- Precise measurement of Λc/D ratio at low p_T
- Λc production → total cc cross section

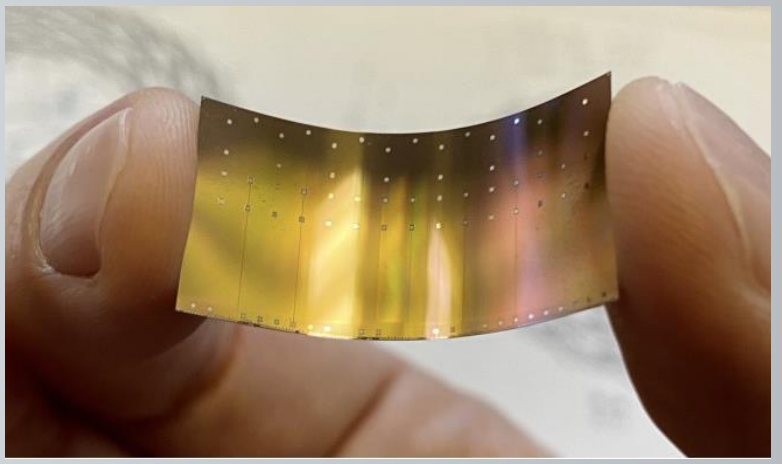
BENCHMARK FOR ITS3

R&D activities

- to reduce the power consumption below 20 mW/cm^2 (airflow cooling)
- to integrate power and data buses on the chip (no passive circuit boards)
- to rely on the stiffness of large size, bent silicon wafers (no mechanical structure)

Design of a new chip

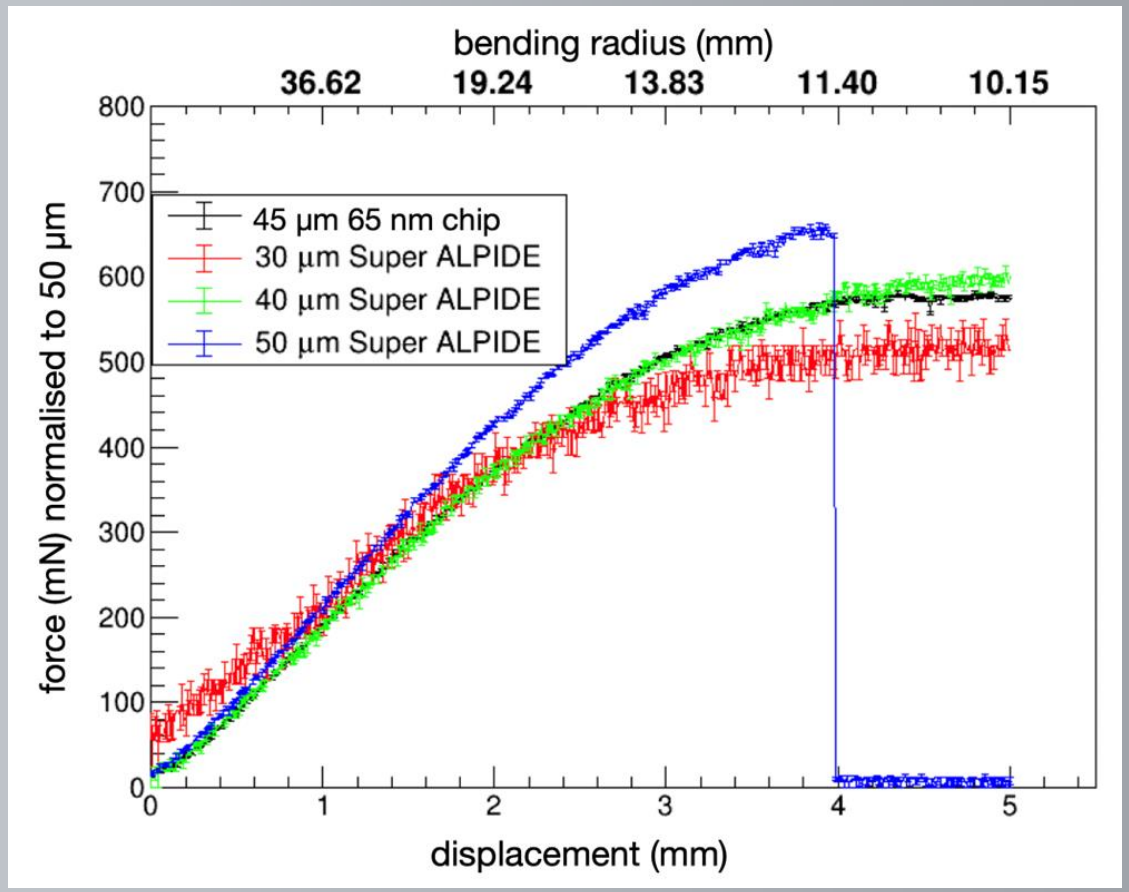
Sensor bending and light support development



Bending MAPS

ALPIDE CHIP BENDING

- MAPS of ~50 µm thickness are quite flexible
- The bending force scales with thickness to the third power → large benefit from going even a bit thinner
- The breaking point moves to smaller bending radii when going thinner
- Project target for thicknesses and bending radii are in a “not breaking” regime



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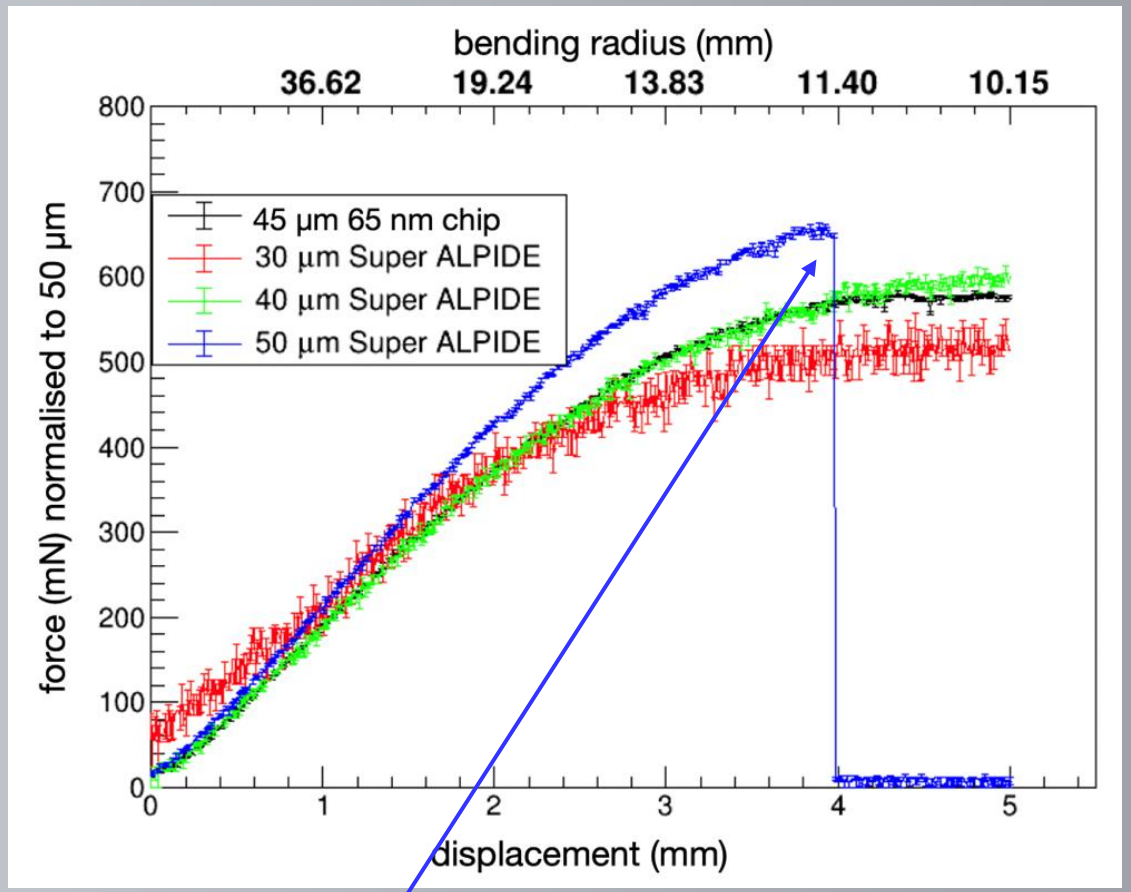
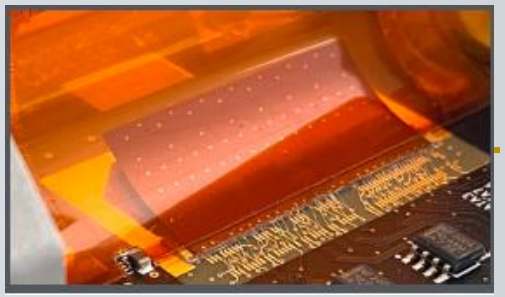


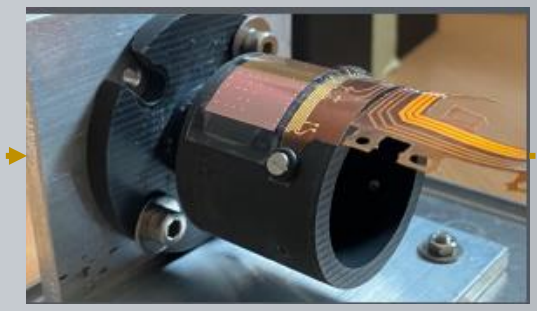
Bending MAPS

Beam test campaigns on bent ALPIDEs:

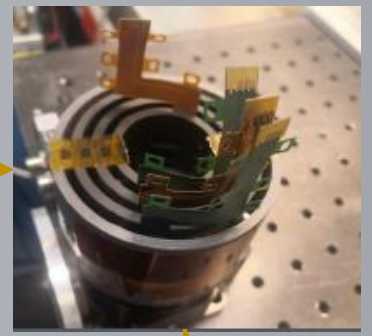
1. First bent chip (DESY, Jun 2020)



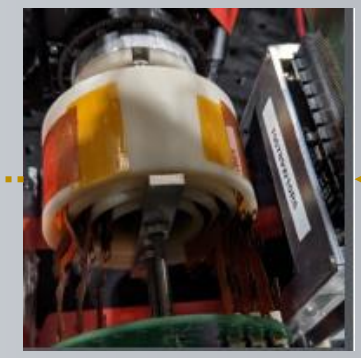
2. Bent chip on cylinder (DESY, Aug/Dec 2020)



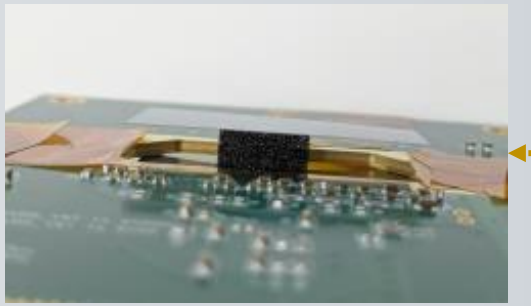
3. Bent chips at all radii, carbon foam (DESY, Apr 2021)



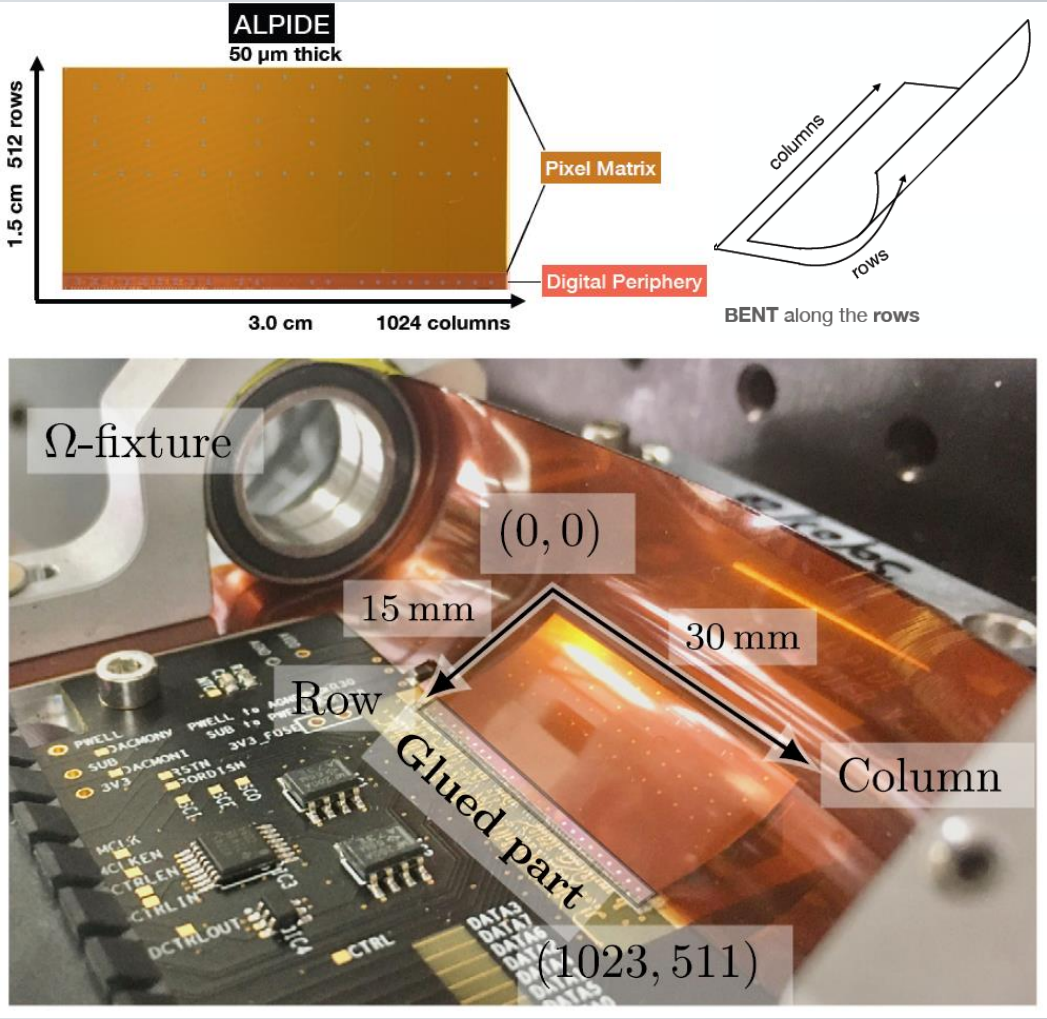
4. µITS3 with 6 ALPIDE + target (SPS, Jul 2021)



5. Carbon foam (DESY, Sep 2021)



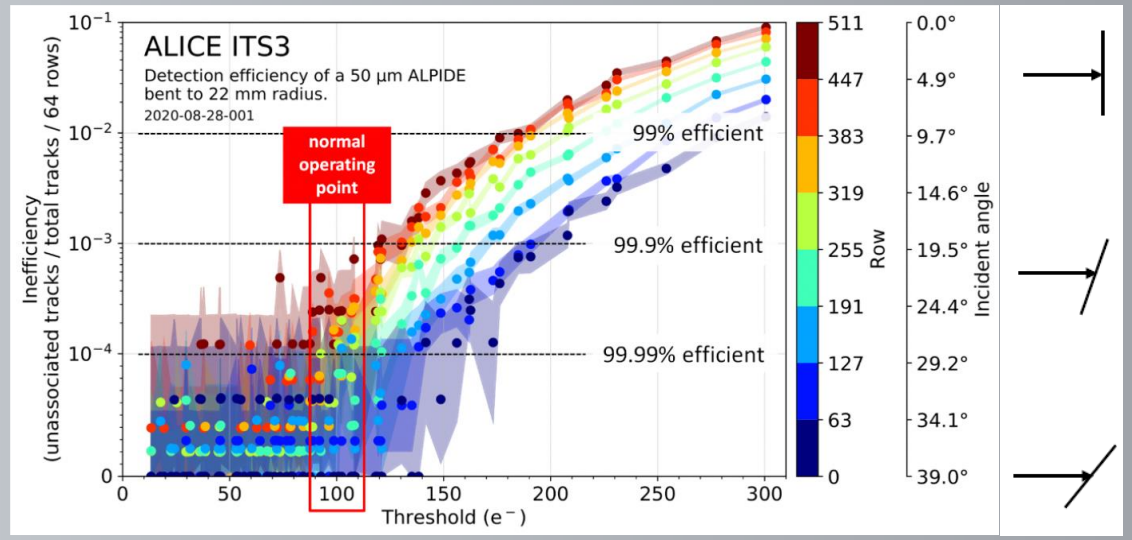
Bending MAPS



DESY, June 2020

Laboratory and test beam measurements

- Chip performance doesn't change after bending
- Efficiency above 99.9% at a threshold of 100 e- (normal operating point), consistent with flat ALPIDE

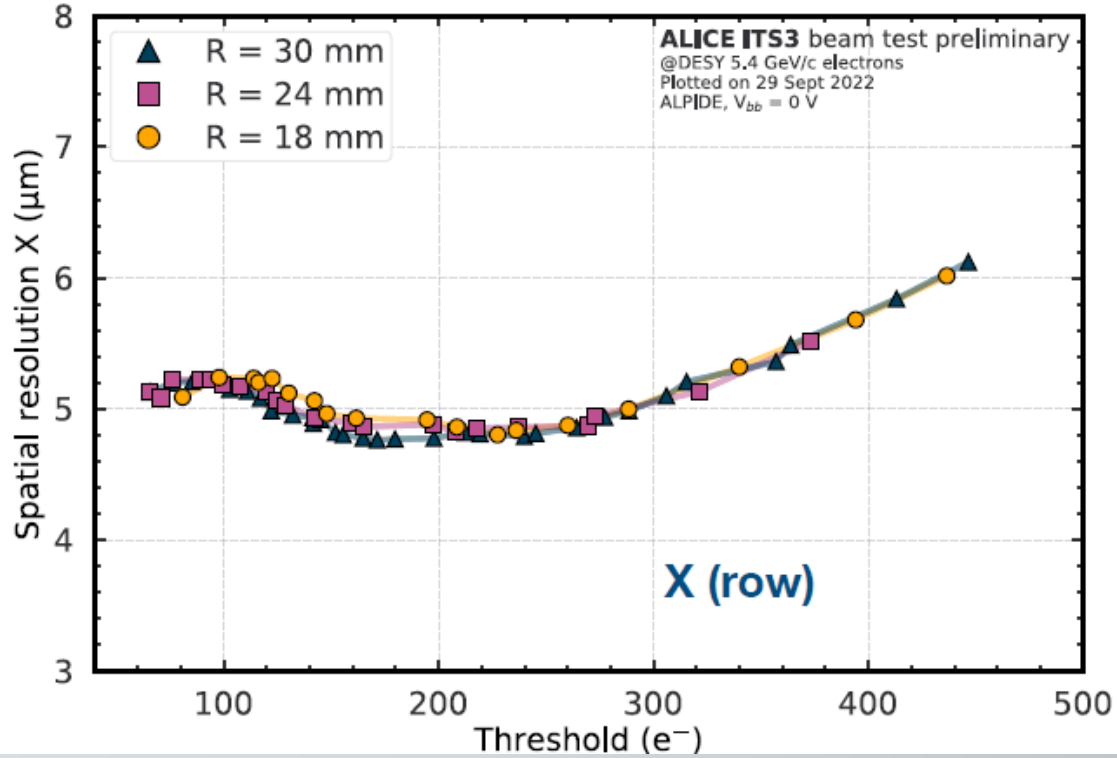


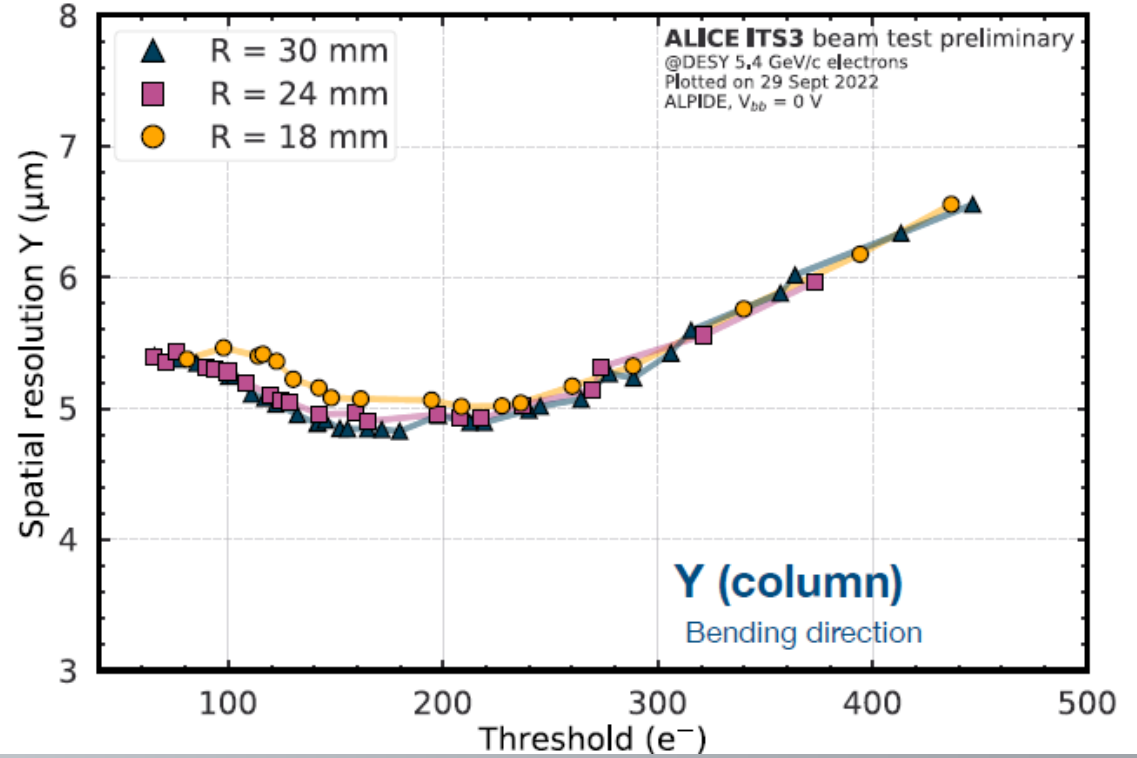
10.1016/j.nima.2021.166280

Bending MAPS

- No effects on bending radius observed
- Spatial resolution (~5 µm) and efficiency (> 99.99%) consistent with flat ALPIDE
- Results also match results where the chip was bent along the other direction

DESY, Apr 2021

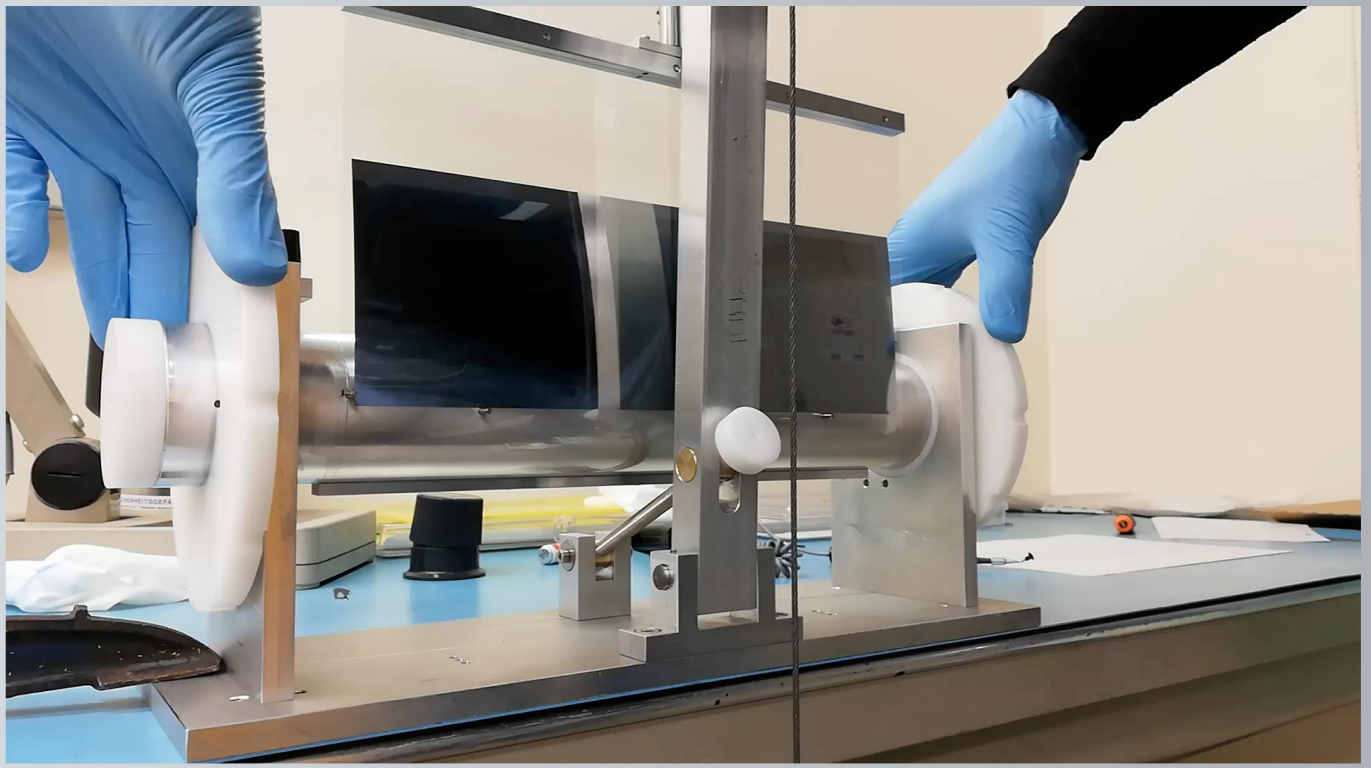




Integration and cooling

WAFER-SCALE SILICON BENDING

Developed procedure allows silicon bending in a repeatable reliable way



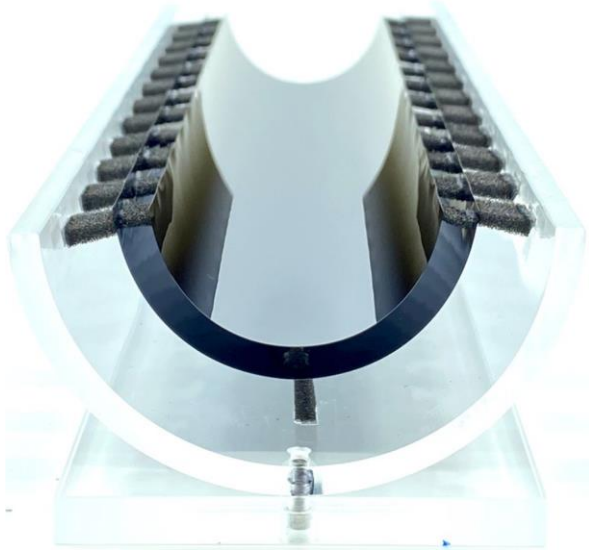
Integration and cooling

LAYER ASSEMBLY

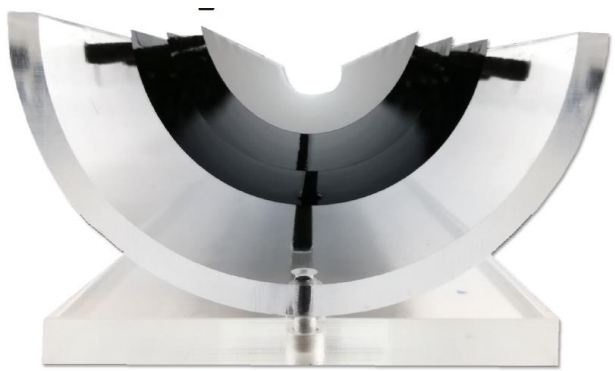
Developed procedure allows silicon bending in a repeatable reliable way

Detailed analysis of the impact of the carbon foam support wedges → local deformations of <100 µm

Layer 2



Layer 2 + 1

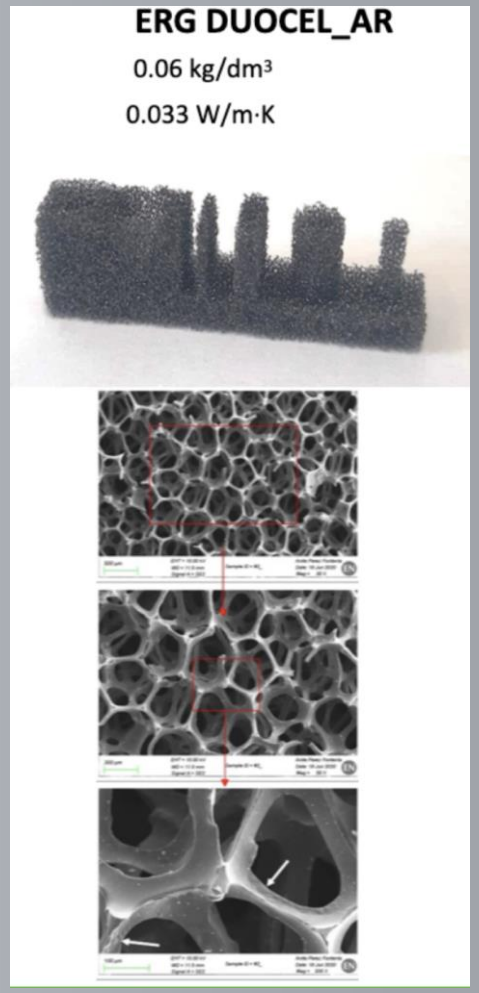


Layer 2 + 1 + 0

Integration and cooling

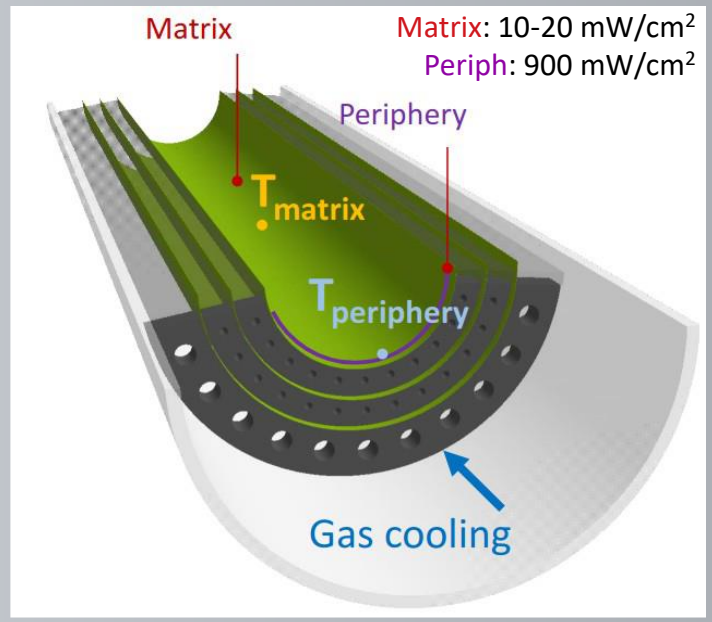
CARBON FOAM SUPPORT STRUCTURE

- Different foams were characterized for machinability and thermal properties
- Baseline is ERG DUOCEL_AR, which also features the largest radiation length



COOLING STUDIES: wind tunnel

- Tests with model and heaters
- Different power & air speed (between 2 and 8 m/s)
- Thermal and mechanical properties are studied on estimated power consumption
- Carbon foam radiator are key for heat removal at periphery
- Air cooling is feasible with margin



Development of the sensor

ITS2: 180 nm CIS process by Tower Semiconductor (aka “TowerJazz”)

- Partially depleted epitaxial layer
- Optimised the process to reach full depletion (ITS2 side project)

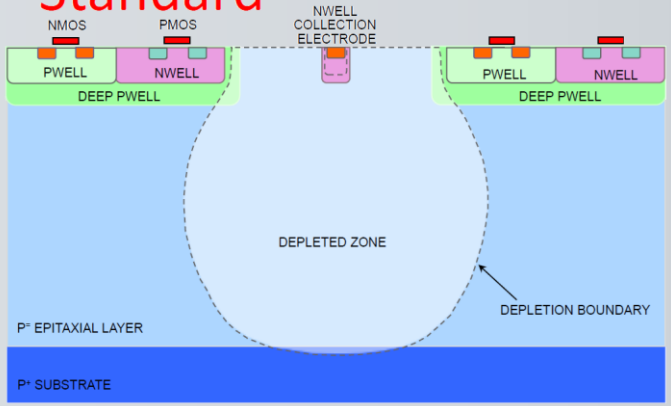
ITS3: 65 nm CIS by Tower Partners Semiconductor (TPSCo)

- Possible use of fully depleted sensors
- Larger wafers: 300 mm instead of 200 mm, single “chip” is enough to equip an ITS3 half-layer
- Smaller structure sizes: potentially
  - lowering power consumption
  - improving spatial resolution
  - reducing charge collection time
  - increasing in-pixel circuitry

Development of the sensor

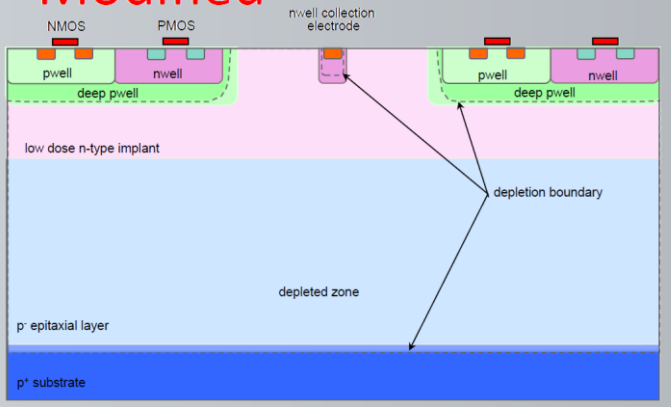
Process modifications for full depletion

Standard



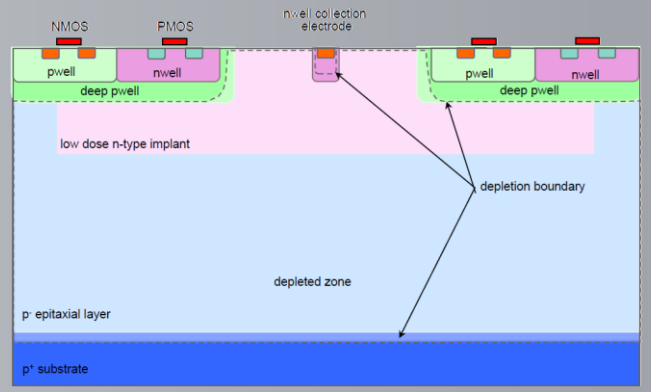
- No fully depleted
- Signal charge outside the depleted area collected primarily by diffusion
- Tolerance to NIEL well beyond 10^{13} 1 MeV n_{eq}/cm^2

Modified



- Fully depleted thanks to a low dose blanket deep high energy n-type implant
- Signal charge collected by drift
- Charge collection time reduced
- NIEL tolerance increased

Modified with gap

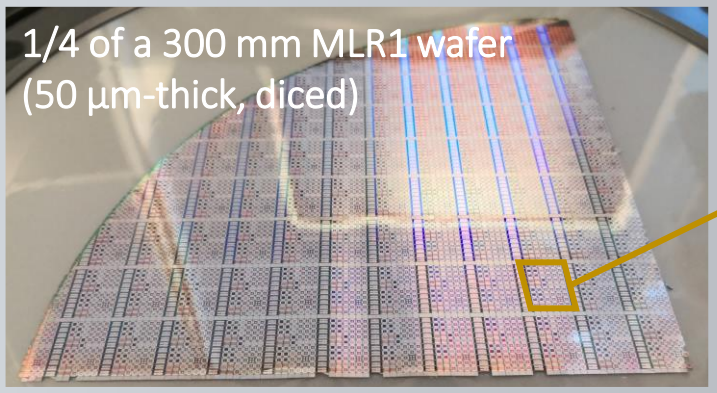


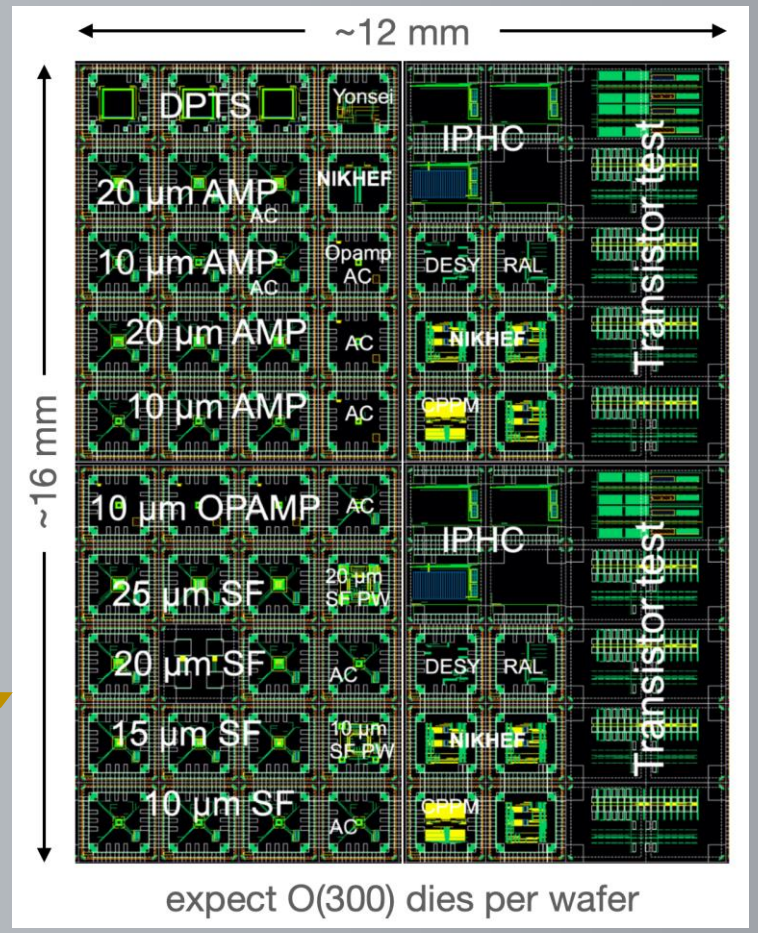
- Gap in the deep n-implant to increase the lateral electric field at the pixel borders
- Higher detection efficiency and improved timing performance at the corners

Development of the sensor

FIRST TEST SUBMISSION: MLR1

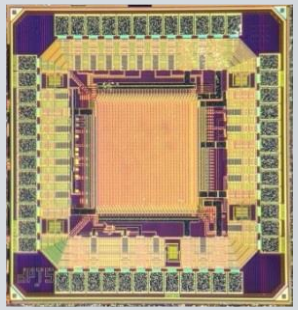
- Submitted in December 2020
- TowerJazz 65 nm
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation hardness
- Contains many test chips (transistor test structures, DACs, analog pixel matrices, digital pixel matrices, …)
- Characterization ongoing since September 2021 (lab and beam tests, many groups involved)





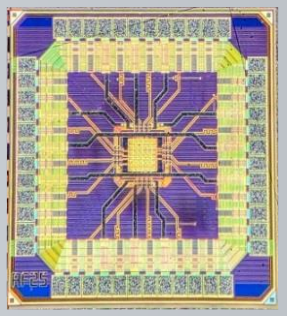
Development of the sensor

3 EXPLORATORY CHIPS



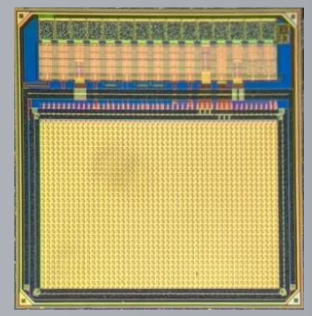
DPTS
(Digital Pixel Test Structure)

- 32 × 32 pixel matrix
- Asynchronous digital readout
- Time over Threshold information
- Pitch: 15 × 15 μm^2



APTS
(Analogue Pixel Test Structure)

- 6x6 pixels (central 4x4 read out)
- Two types of output drivers (SF/OpAmp)
- 10, 15, 20, 25 µm pitches

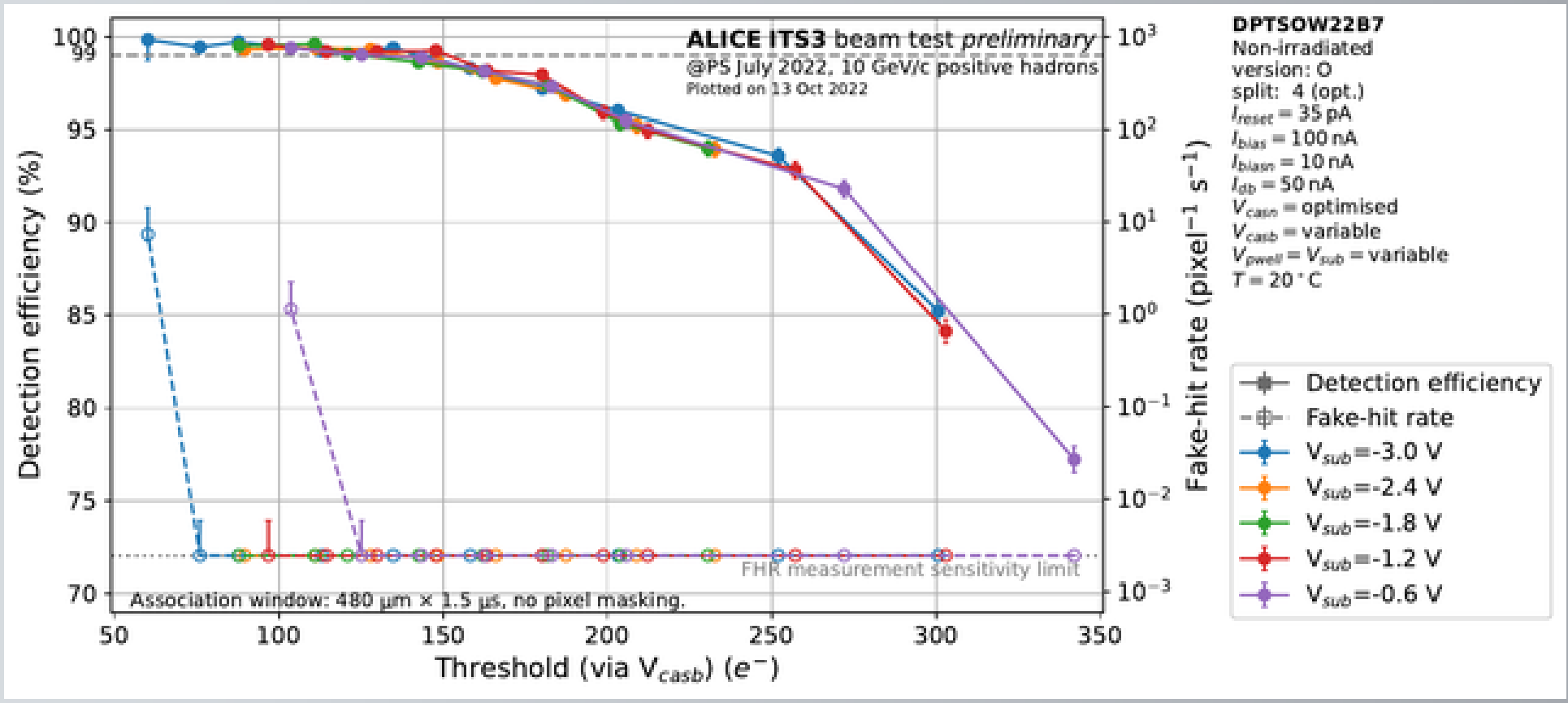


CE65
(Circuit Exploratoire 65 nm)

- 64 × 32 with 15 µm pitch
- 48 × 32 with 25 µm pitch
- Analog Rolling shutter readout
- 3 in pixel architectures

Development of the sensor

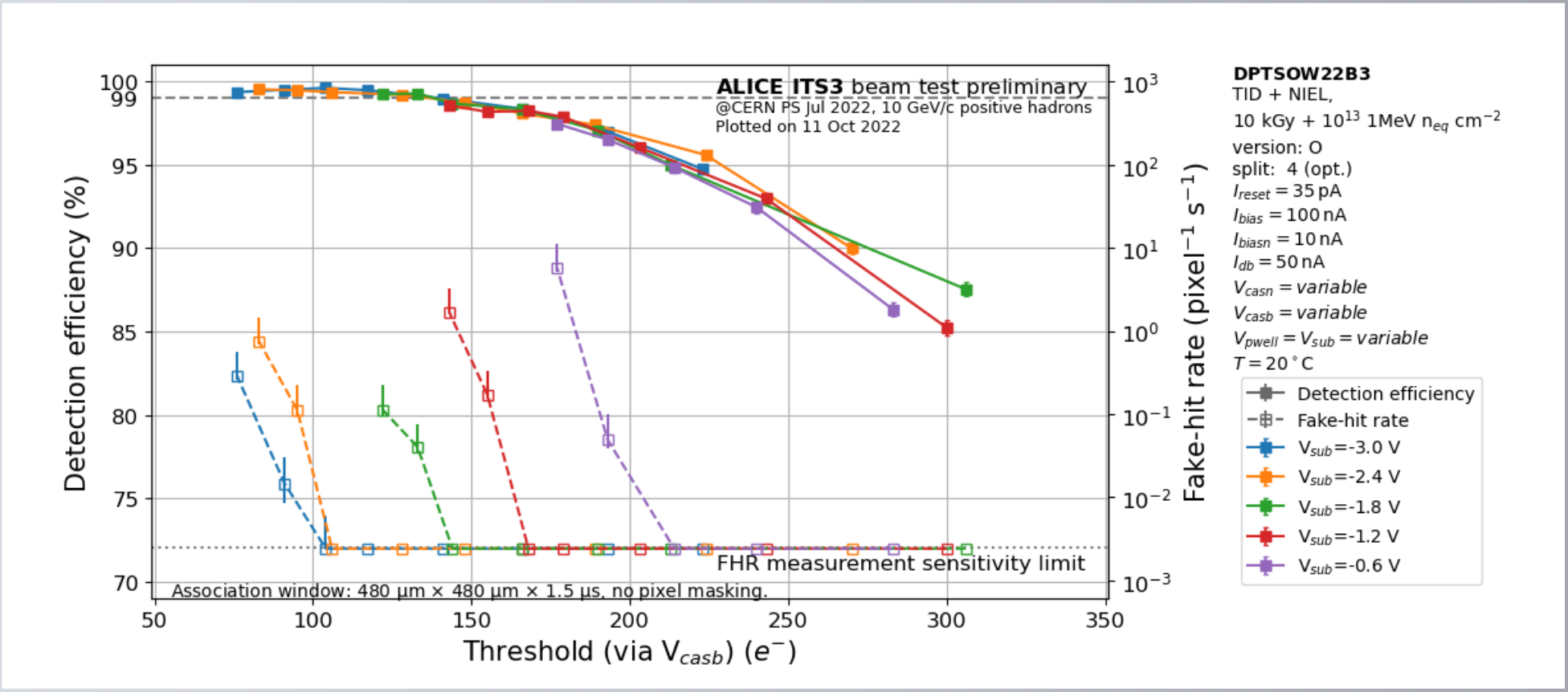
Non irradiated DPTS: Excellent efficiency and low fake hit rate



Development of the sensor

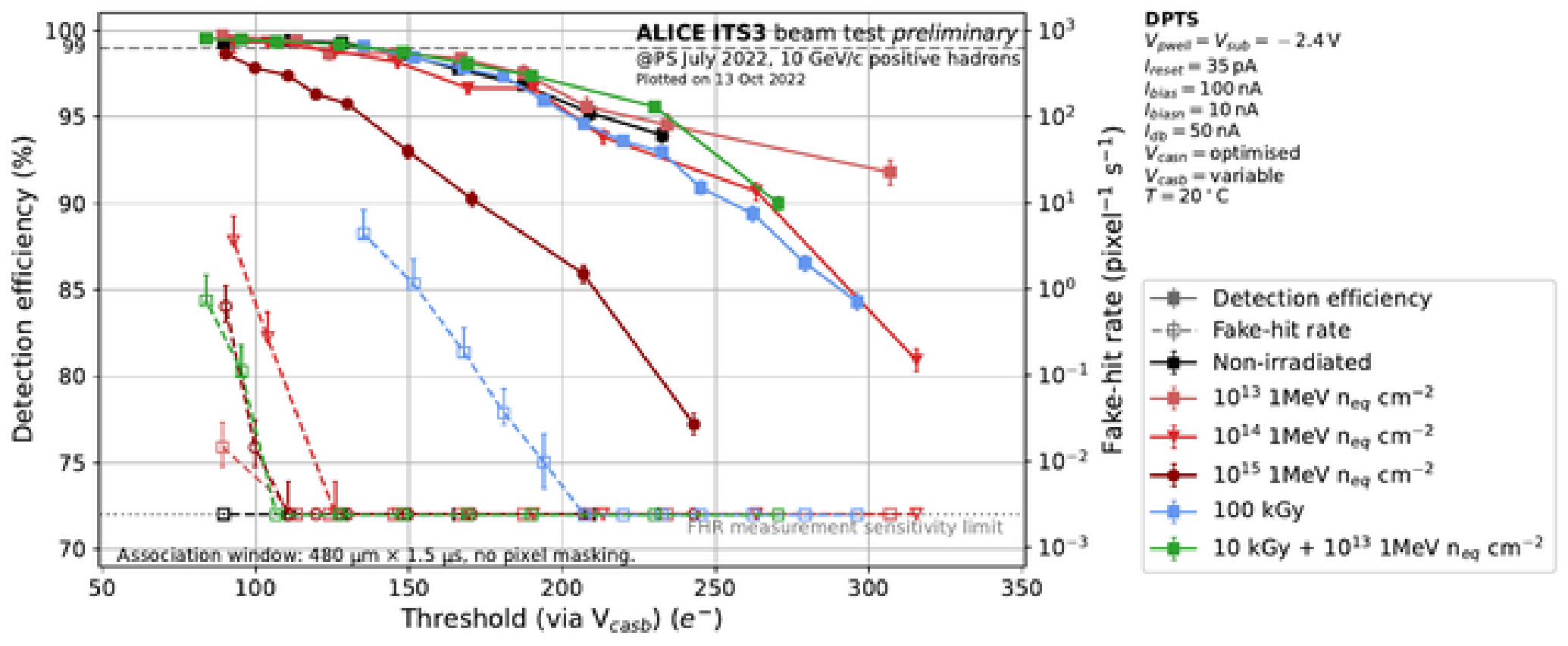
DPTS after 10 Mrad + 10^{13} n eq /cm^2: larger fake hit rate, but has margin

Target value for ITS3



Development of the sensor

Good performance even at higher irradiation levels

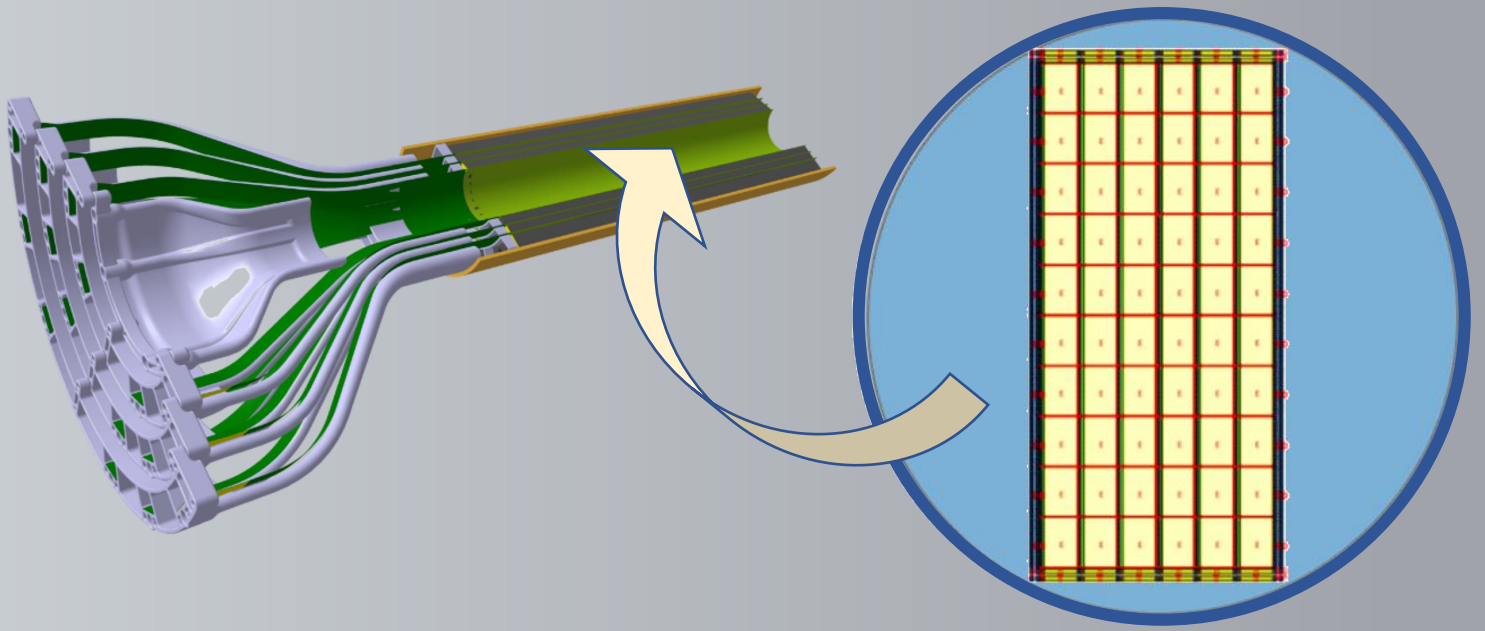


Next steps

- **STITCHING** and power/signal distribution on large structures (ER1)
  - Stitching used to connect metal traces for power distribution and long range on-chip interconnect busses for control and data readout
  - Pixel matrix repeated multiple times to create a single structure 280 mm long
  - An entire half-layer in one wafer

- **TDR** (end of 2023)

- **INSTALLATION** during LHC LS3 (2027)



Wafer (ϕ = 300 mm)

Conclusions

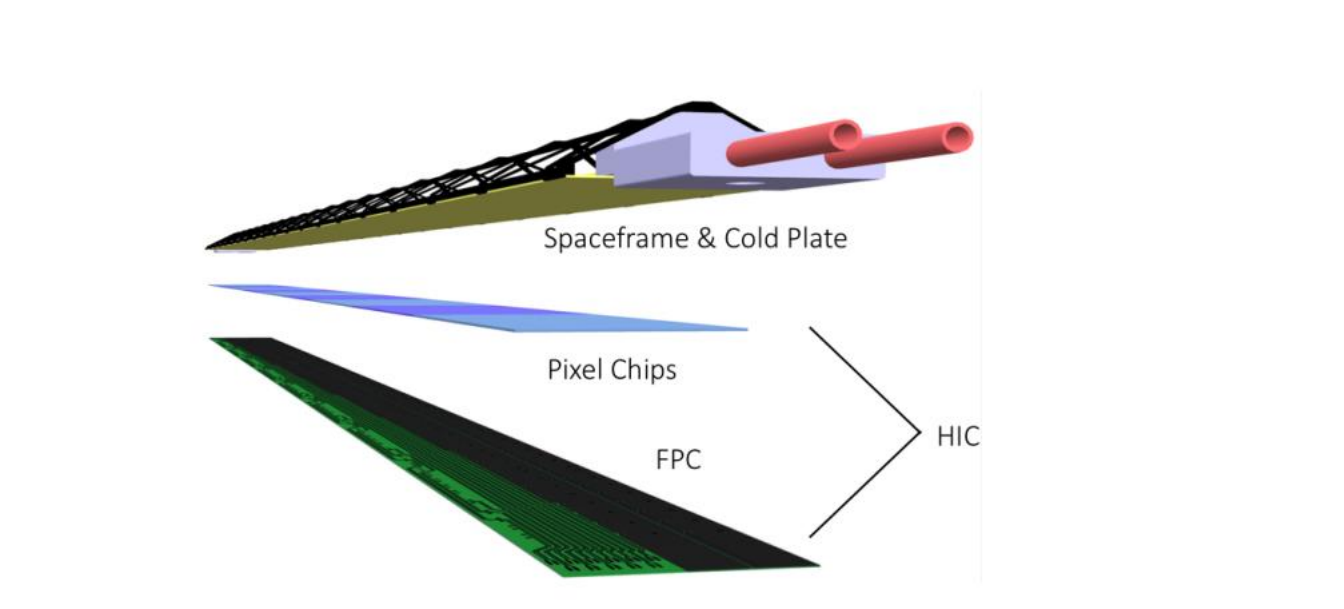
- **ITS3 replaces the 3 innermost layers of ALICE ITS2** by a bent, wafer scale MAPS detector which reduces material budget by factor of 7 compared to ITS2

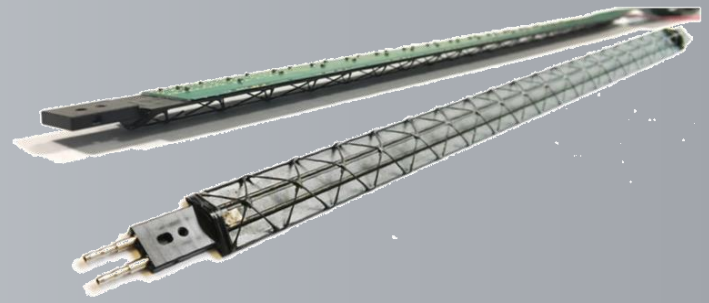
- **Major milestones have been passed such as:**
  - Full size mechanical integration prototypes exist
  - Air cooling concept verified by full size mockup
  - Bending of thinned sensors verified
  - Tower Partners Semiconductor 65nm technology qualified
  - Building blocks and basic pixel matrices efficient
  - Successful beam characterisation of pixel sensor

Backup

Schematic layout of the ITS2 IB stave

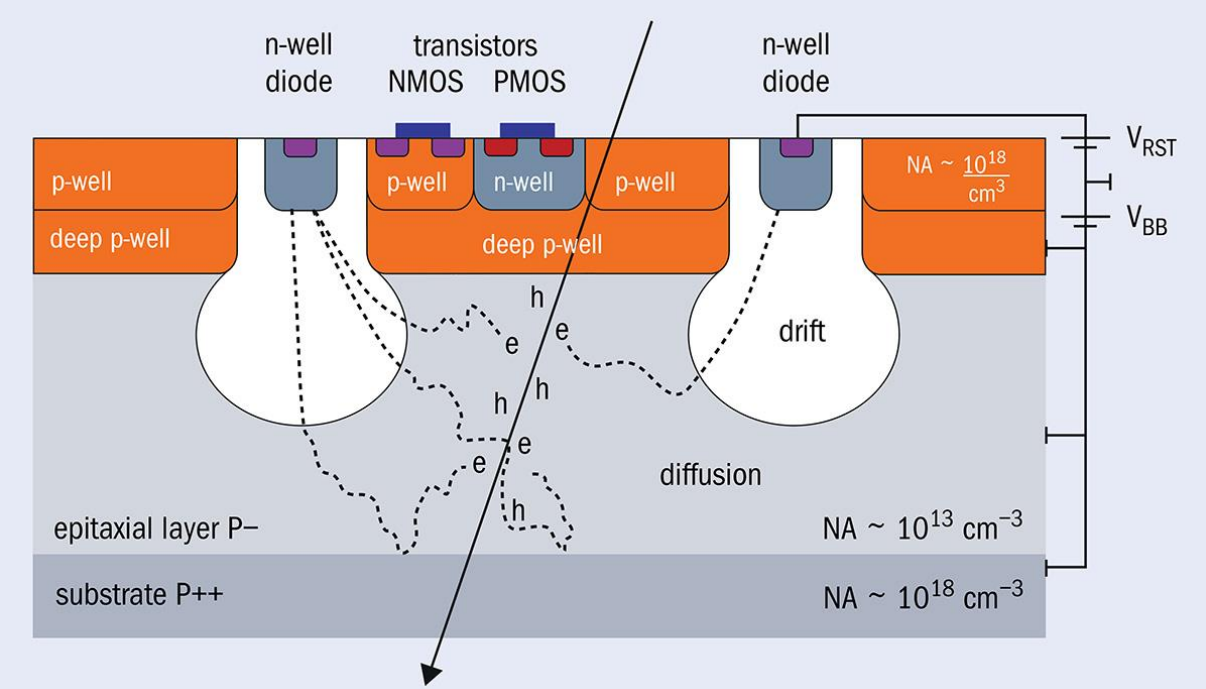
- carbon fibre support structure (spaceframe)
- water cooling circuit (colplate)
- hybrid integrated circuit (HIC) with 9 chips on a Flexible Printed Circuit (FPC)





The ALPIDE sensor

MAPS: sensor collecting the charge signal and readout circuit hosted in the same substrate of silicon



Partially depleted epitaxial layer

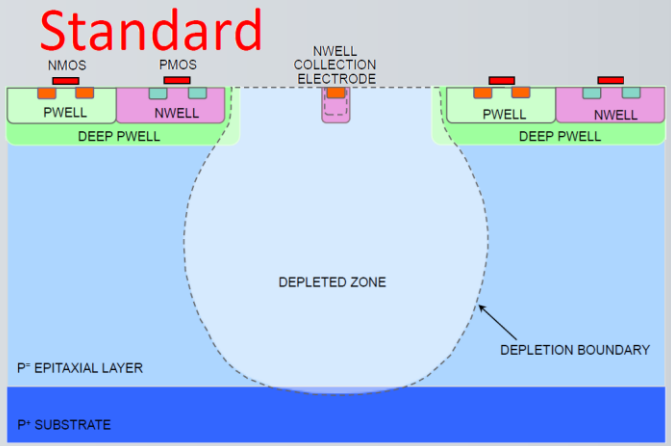
- 180nm CMOS process provided by Towerjazz
- Sensors are thinned down to 50 (IN) -100 (OB) micrometers → material budget reduced
- Chip area: 15x30 mm^2, half a million pixels
- Power consumption <40 mW/cm^2
- Spatial resolution ~ 5 micrometer

Further developments to obtain a fully depleted MAPS (ITS2 "side project")

- Higher radiation tolerance
- Faster charge collection

Development of the sensor

Process modifications for full depletion

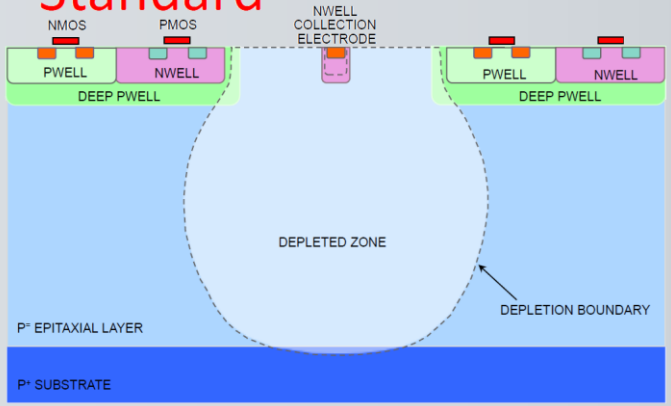


- No fully depleted
- Signal charge outside the depleted area collected primarily by diffusion
- Tolerance to NIEL well beyond 10^{13} 1 MeV n_{eq}/cm^2

Development of the sensor

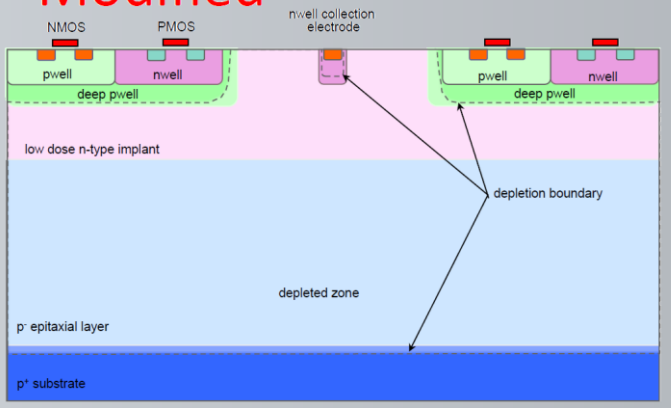
Process modifications for full depletion

Standard



- No fully depleted
- Signal charge outside the depleted area collected primarily by diffusion
- Tolerance to NIEL well beyond 10^{13} 1 MeV n_{eq}/cm^2

Modified

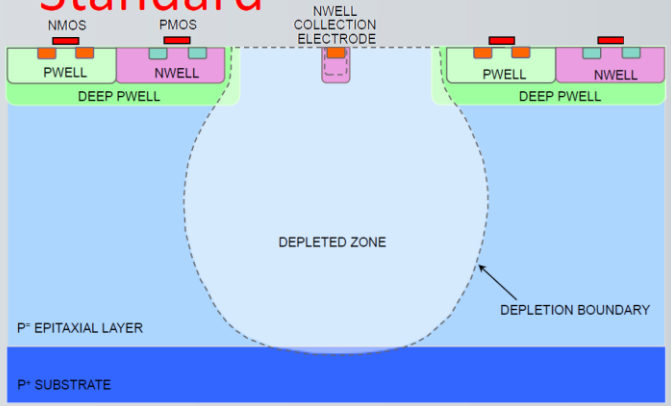


- Fully depleted thanks to a low dose blanket deep high energy n-type implant
- Signal charge collected by drift
- Charge collection time reduced
- NIEL tolerance increased

Development of the sensor

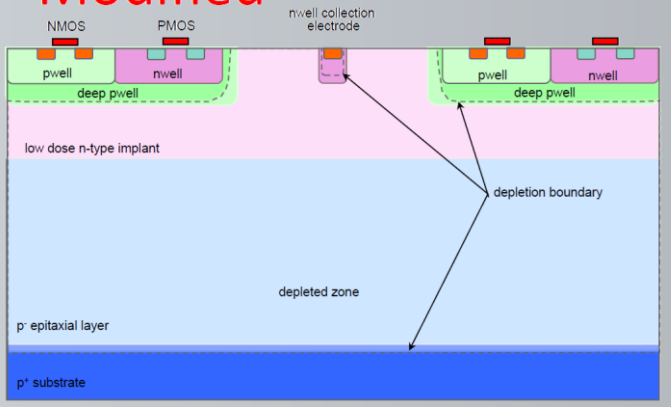
Process modifications for full depletion

Standard



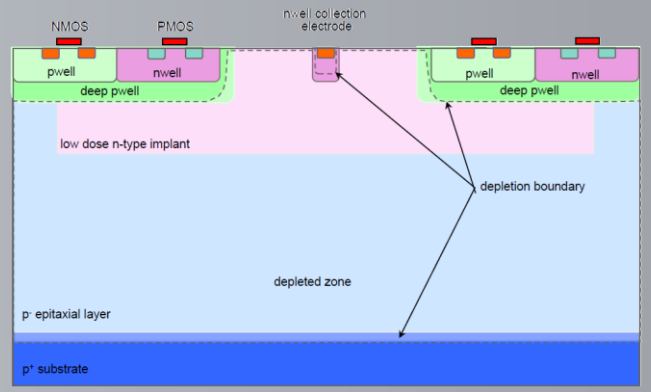
- No fully depleted
- Signal charge outside the depleted area collected primarily by diffusion
- Tolerance to NIEL well beyond 10^{13} 1 MeV n_{eq}/cm^2

Modified



- Fully depleted thanks to a low dose blanket deep high energy n-type implant
- Signal charge collected by drift
- Charge collection time reduced
- NIEL tolerance increased

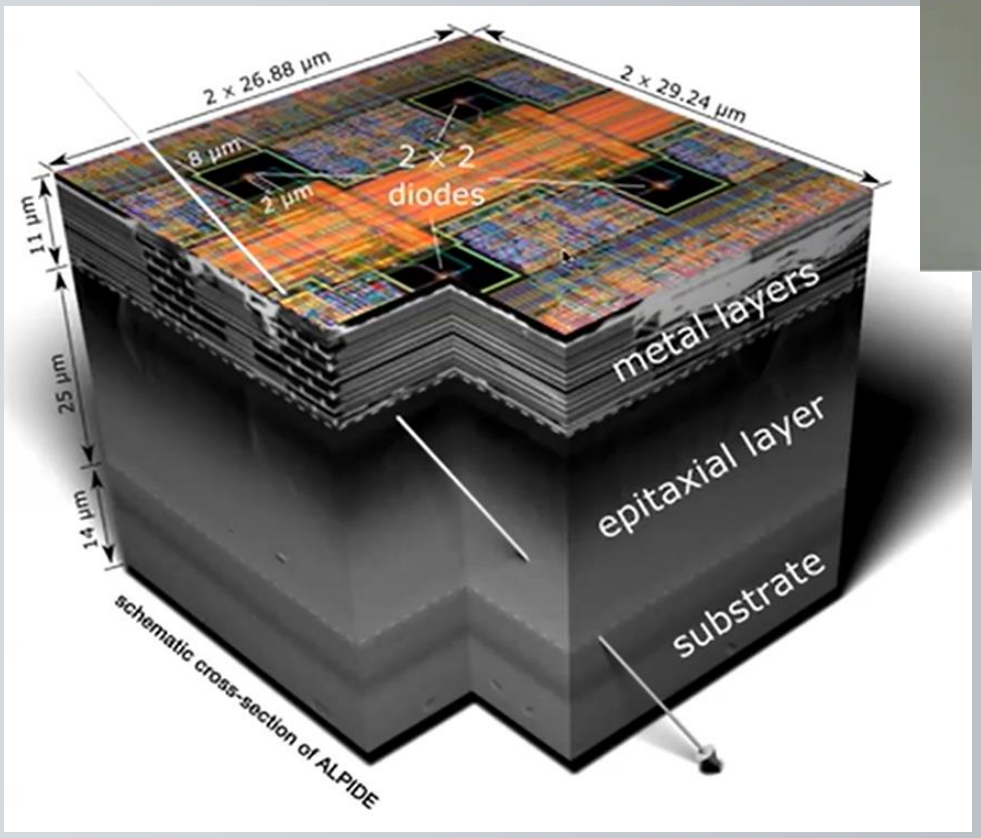
Modified with gap



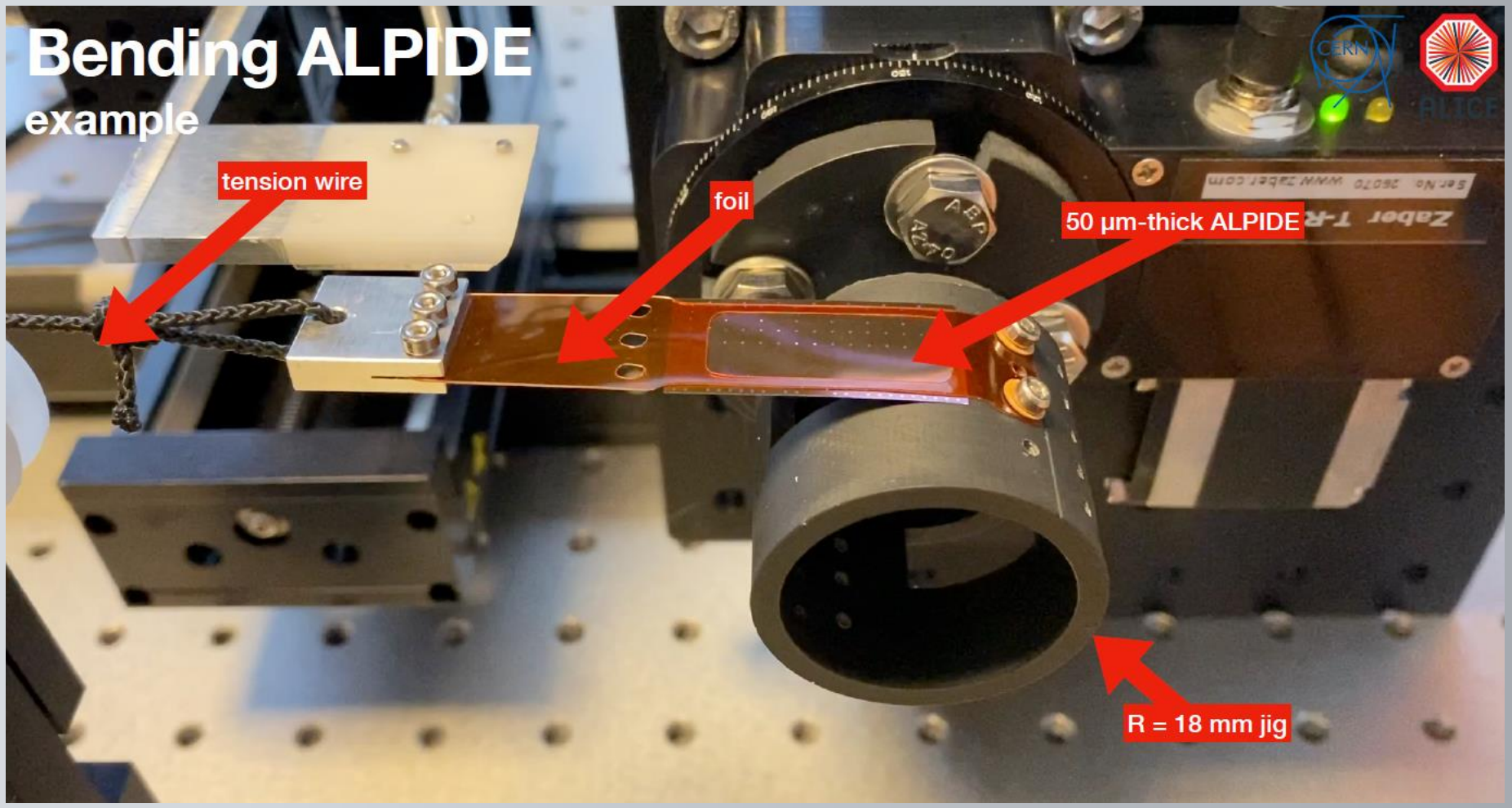
- Gap in the deep n-implant to increase the lateral electric field at the pixel borders
- Higher detection efficiency and improved timing performance at the corners

Bending MAPS

Make use of the flexible nature of thin silicon



Bending ALPIDE

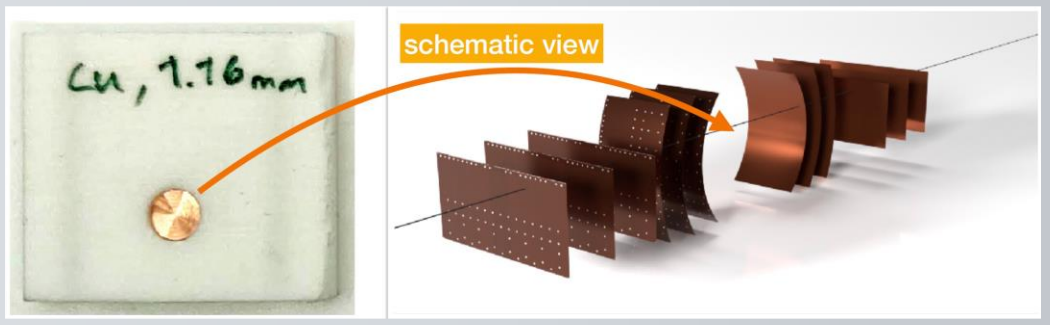


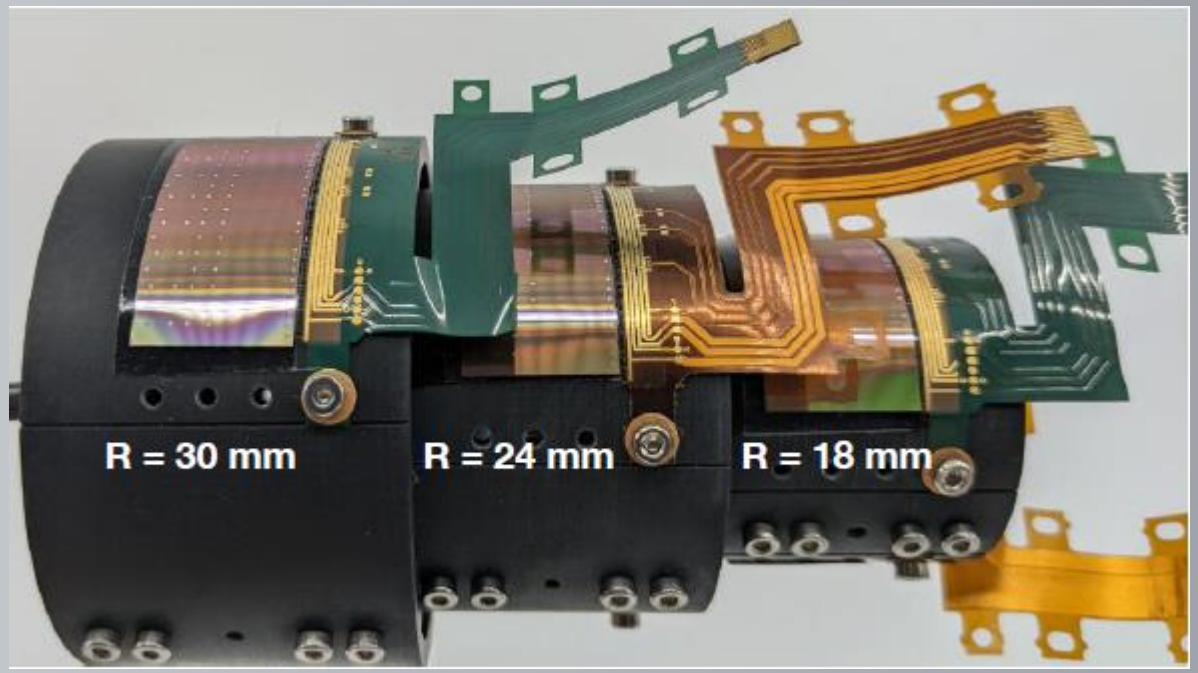
Bending MAPS

SPS, July 2021

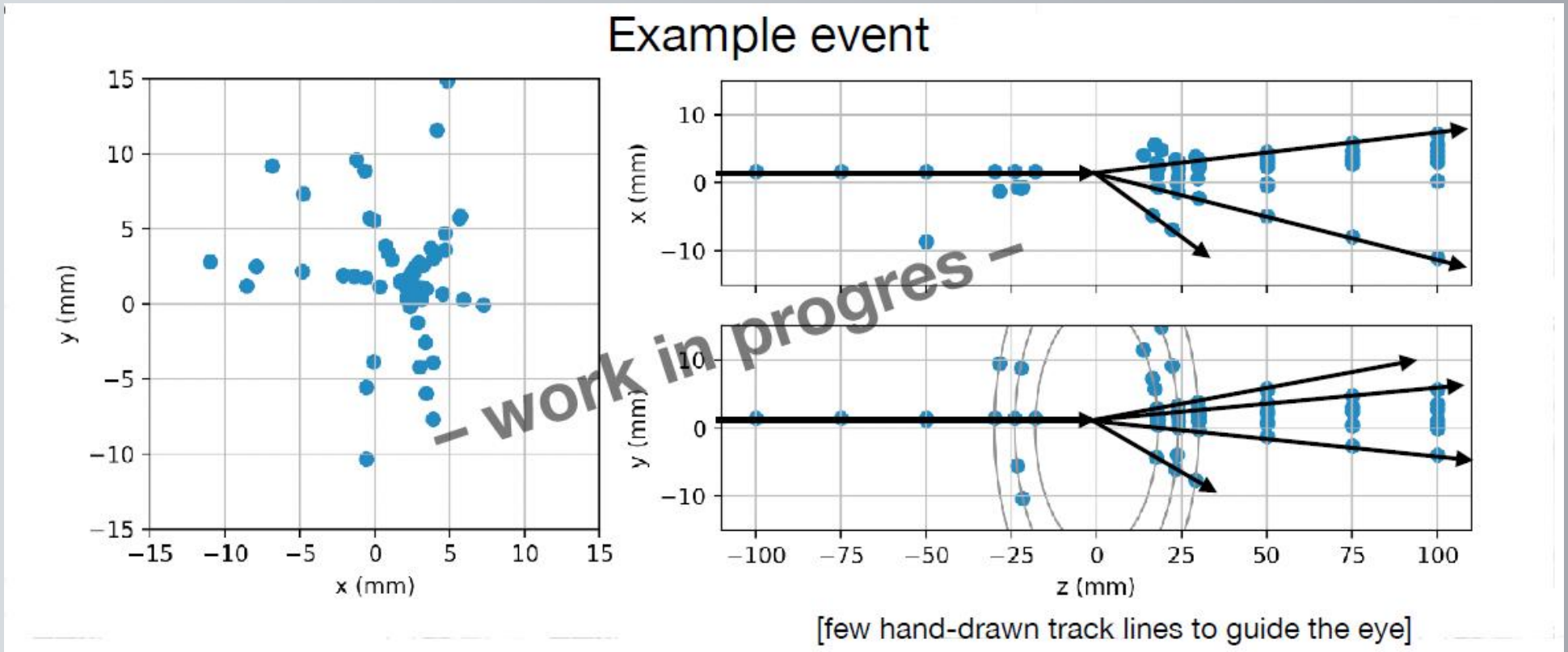
Full mock-up of the final ITS (“µITS3”)

- 6 ALPIDE chips bent to the target radii of ITS3 (R=18, 24, 30 mm)
- Fully bent along columns, including the periphery
- Test beam with Cu target in the center (proton/pion-Cu collisions)
- Track and vertex reconstruction



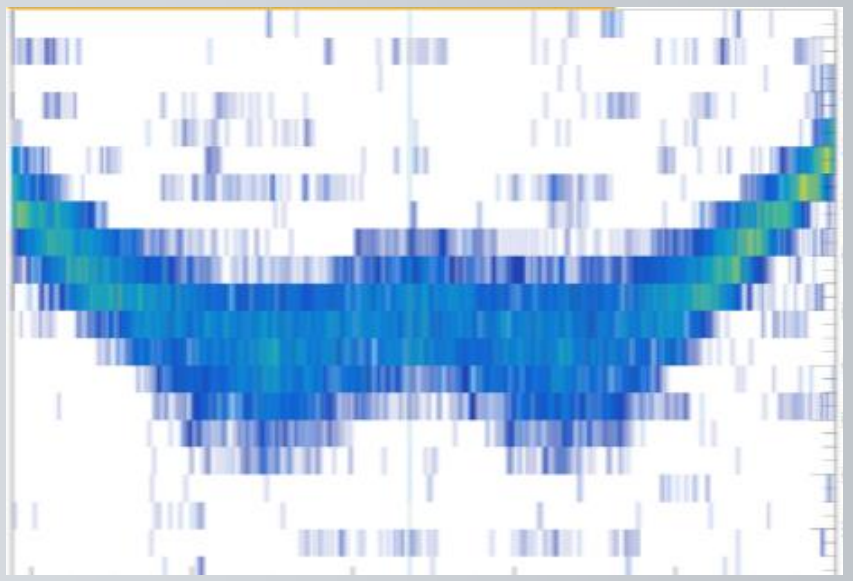


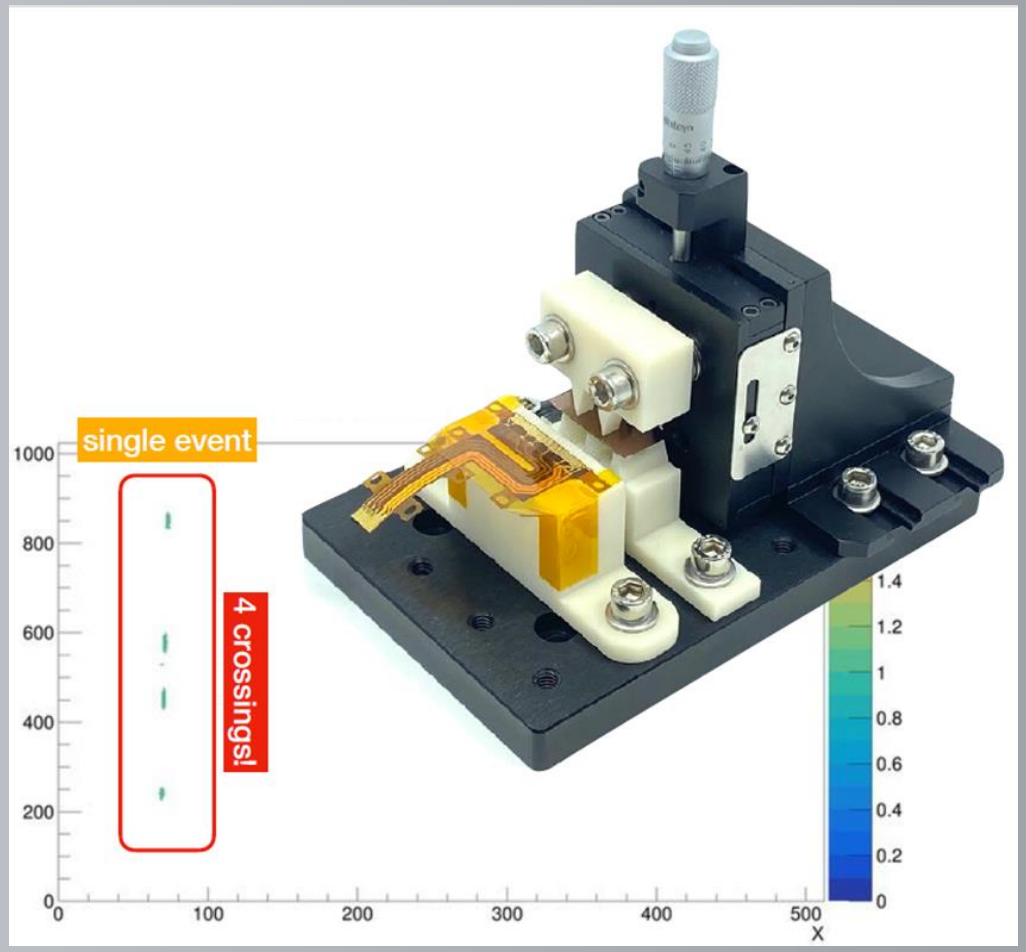
Beam test – ulTS3



Beam test – WON

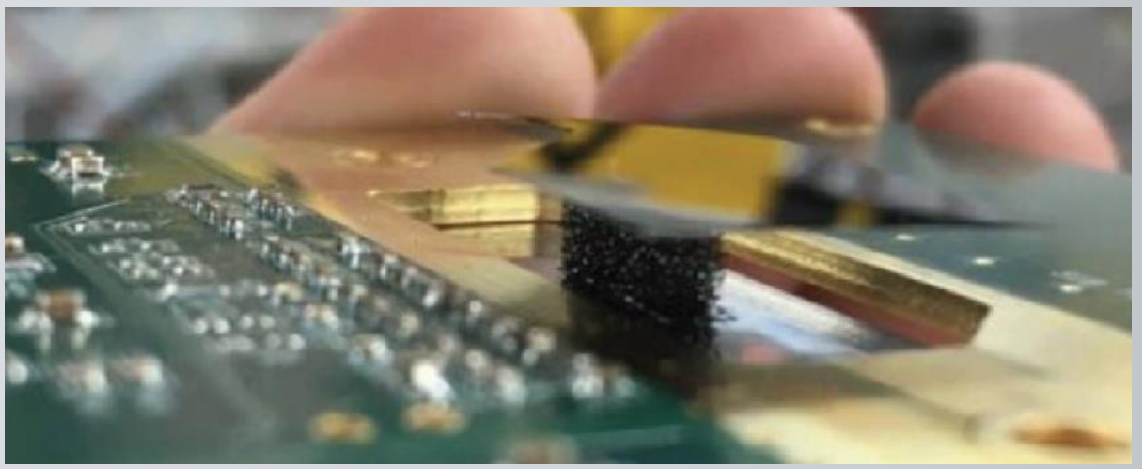
- ALPIDE bent into a W shape (bendig radii ≈ 2 cm)

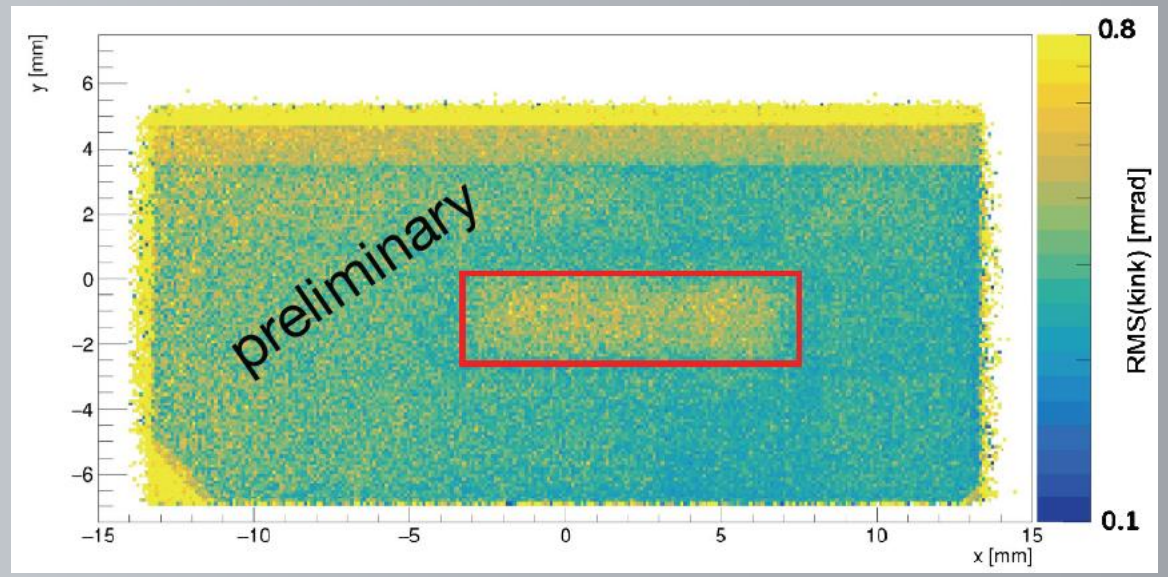




Beam test – Carbon foam

- Carbon foam brought to beam (DESY)
- Scattering angle due to carbon foam was studied
- Very small effect





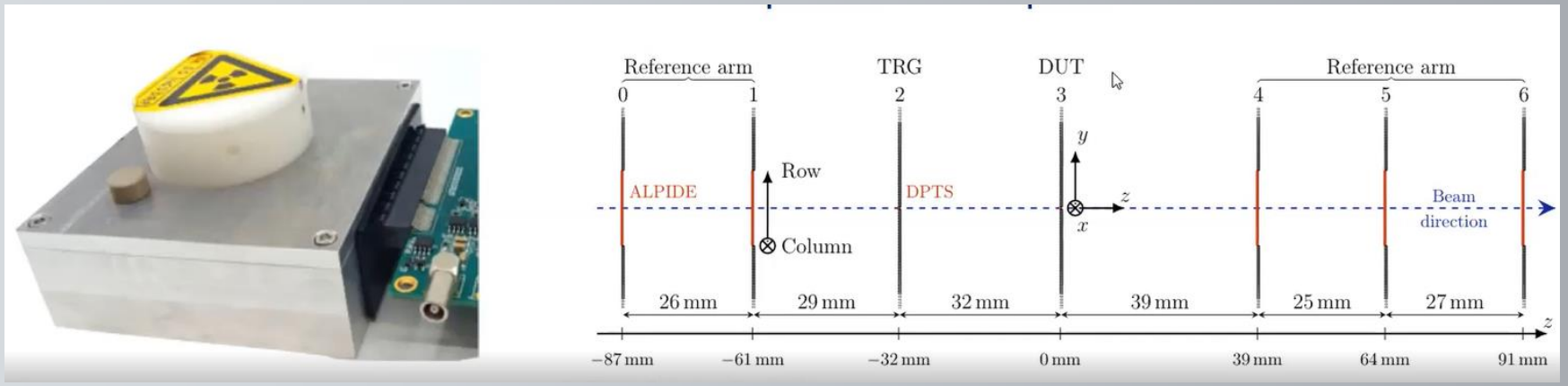
MRL1 chip characterization

Measurements in the LAB

1. Smoke tests
2. Pulse and noise measurements
3. Measurements with 5.9 KeV X-rays from 55Fe source
   - Tuning chip parameters
   - Signal calibration
   - Charge collection efficiency estimation

At the beam with MIPs (electrons and pions)

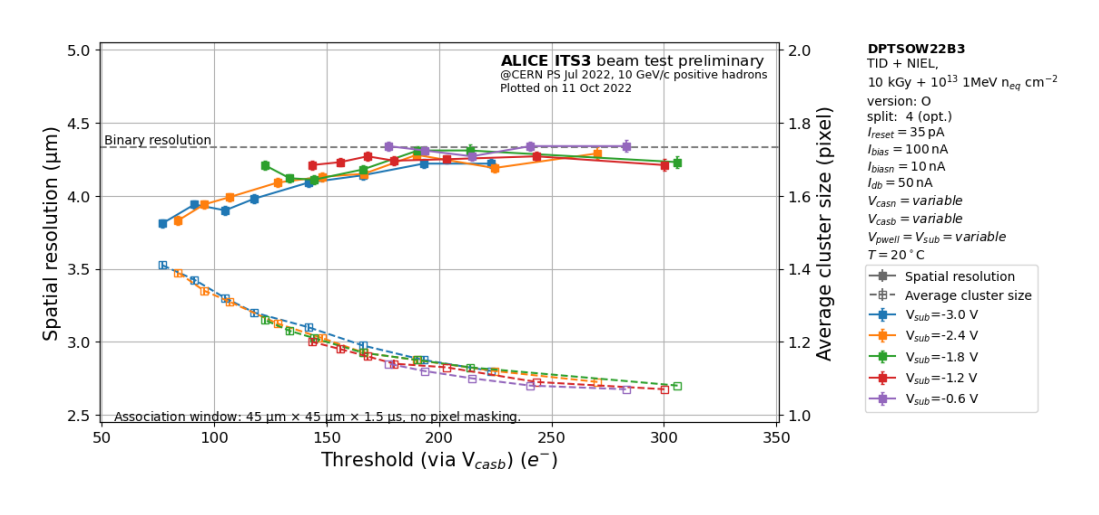
1. Tracks reconstructed by the telescope planes
2. Association of clusters in DUT with tracks
3. Efficiency/FHR vs discriminator threshold for digital chips
4. Signal, SNR for analogue chips
5. Spatial and temporal resolution

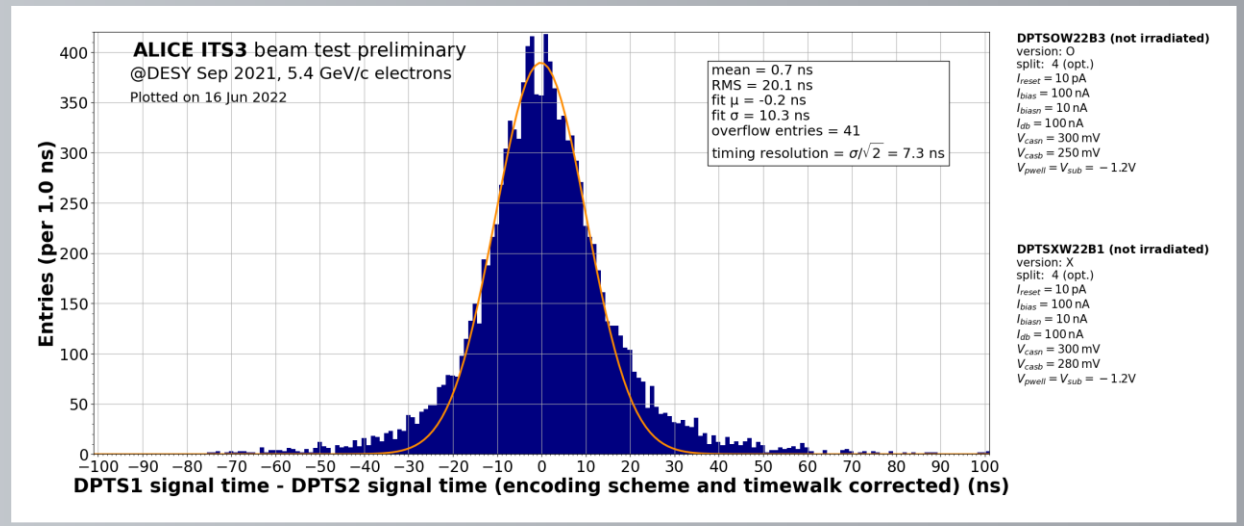


Development of the sensor

Main DPTS results:

- 99 % efficiency up to:
  - 10 Mrad + 10^{13} 1 MeV n eq /cm^2
  - 10^{15} 1 MeV n eq /cm^2
- Spatial resolution: about 4.3 µm
- Temporal resolution at default (low power) parameters: ~7 ns



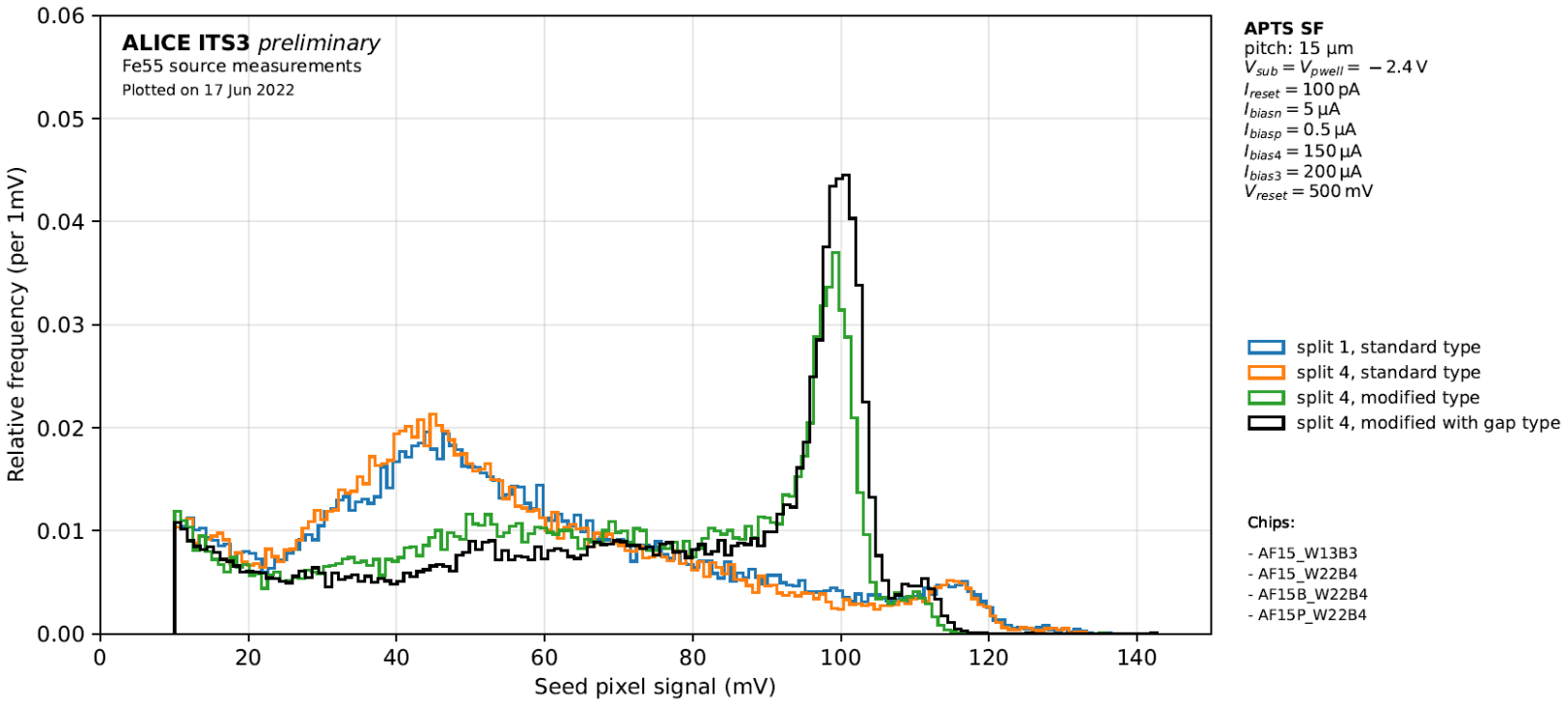


arXiv:2212.08621

Development of the sensor

APTS – Fe-55 lab tests

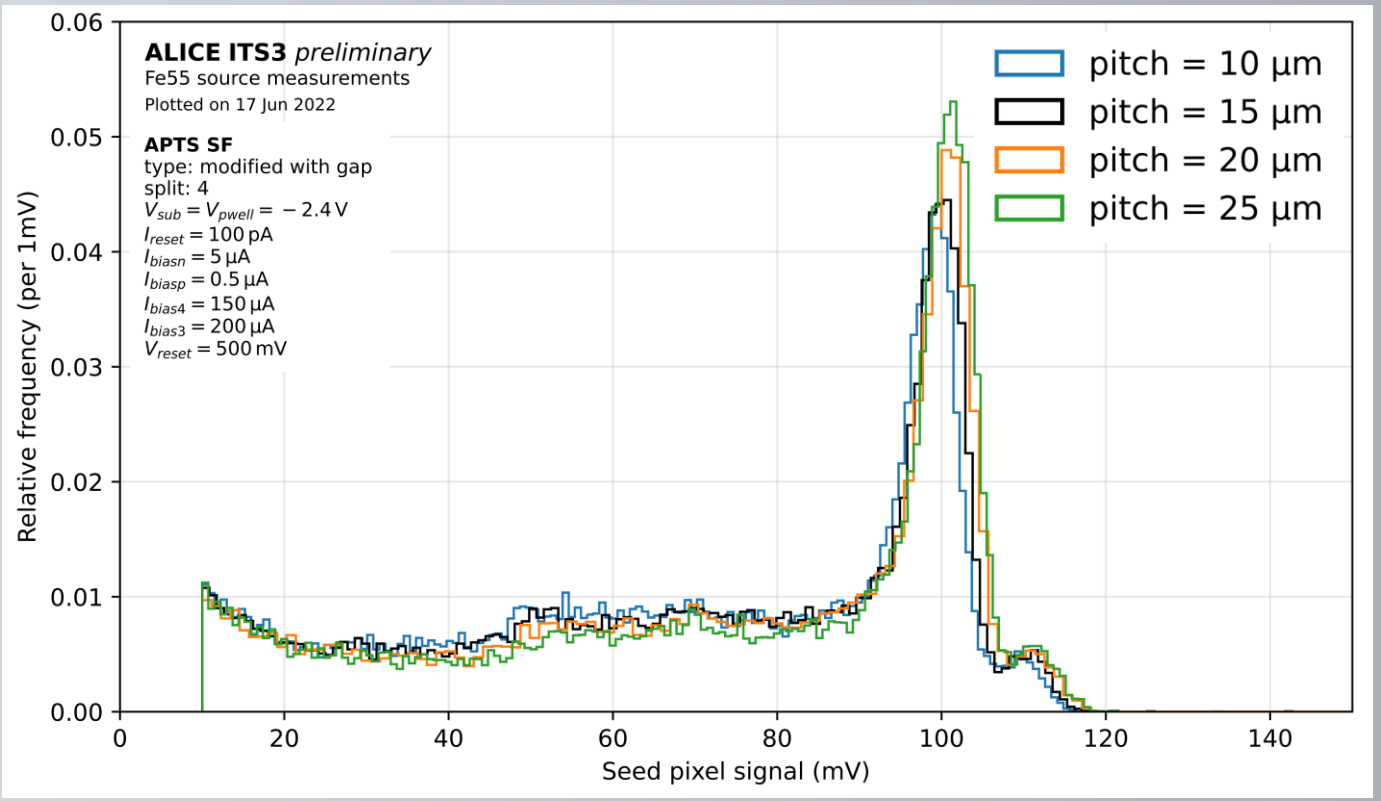
- In standard process seed pixel takes ~50% of charge
- In modified process most of the charge is collected in one pixel



Development of the sensor

APTS – Fe-55 lab tests

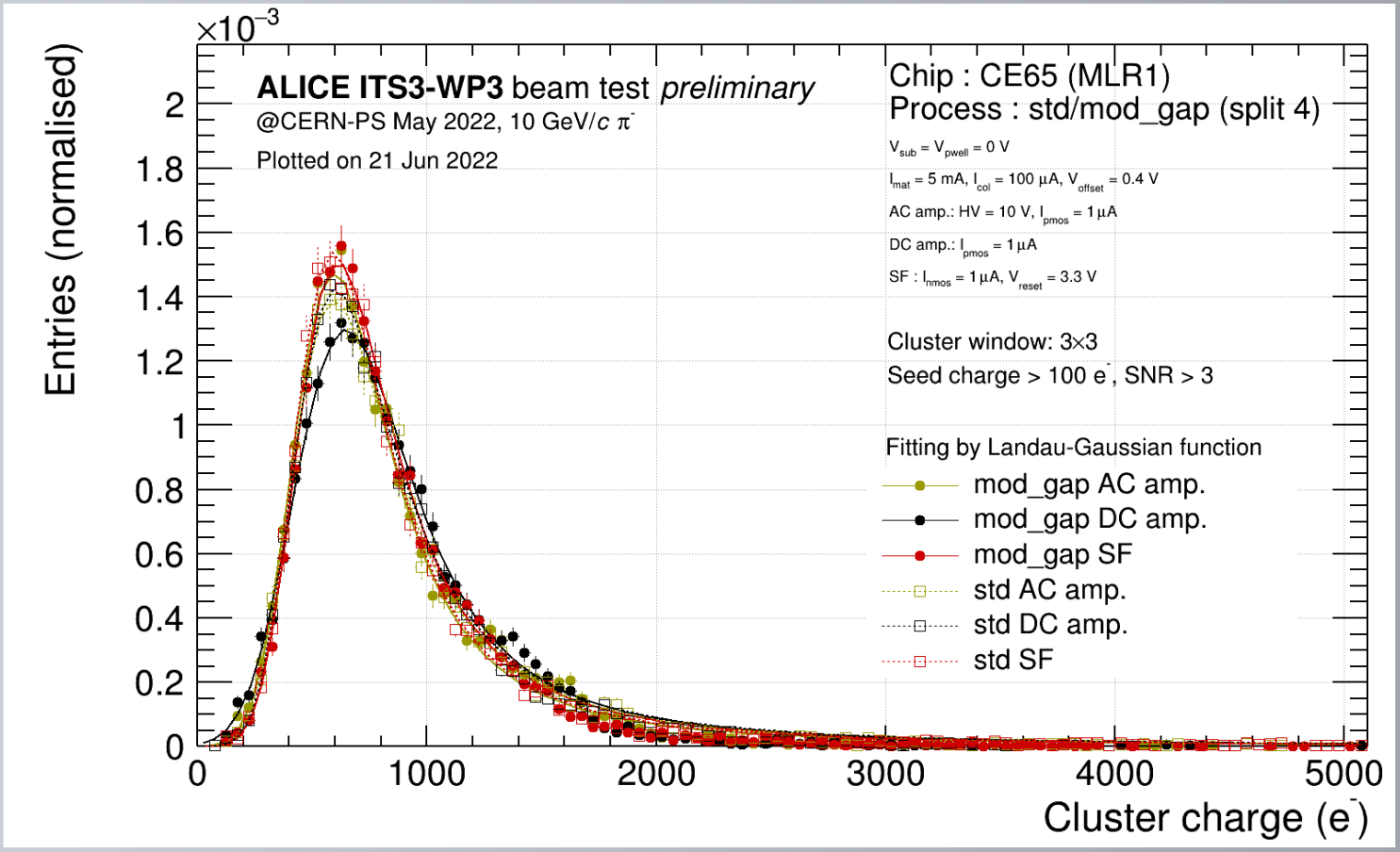
- Pixels of pitches of 10-25 µm show similar results → indicates that the charge collection is very efficient
- Allows to choose optimal pitch for the final sensor



Development of the sensor

CE65: Cluster charge doesn't depend on process modification and pixel architecture

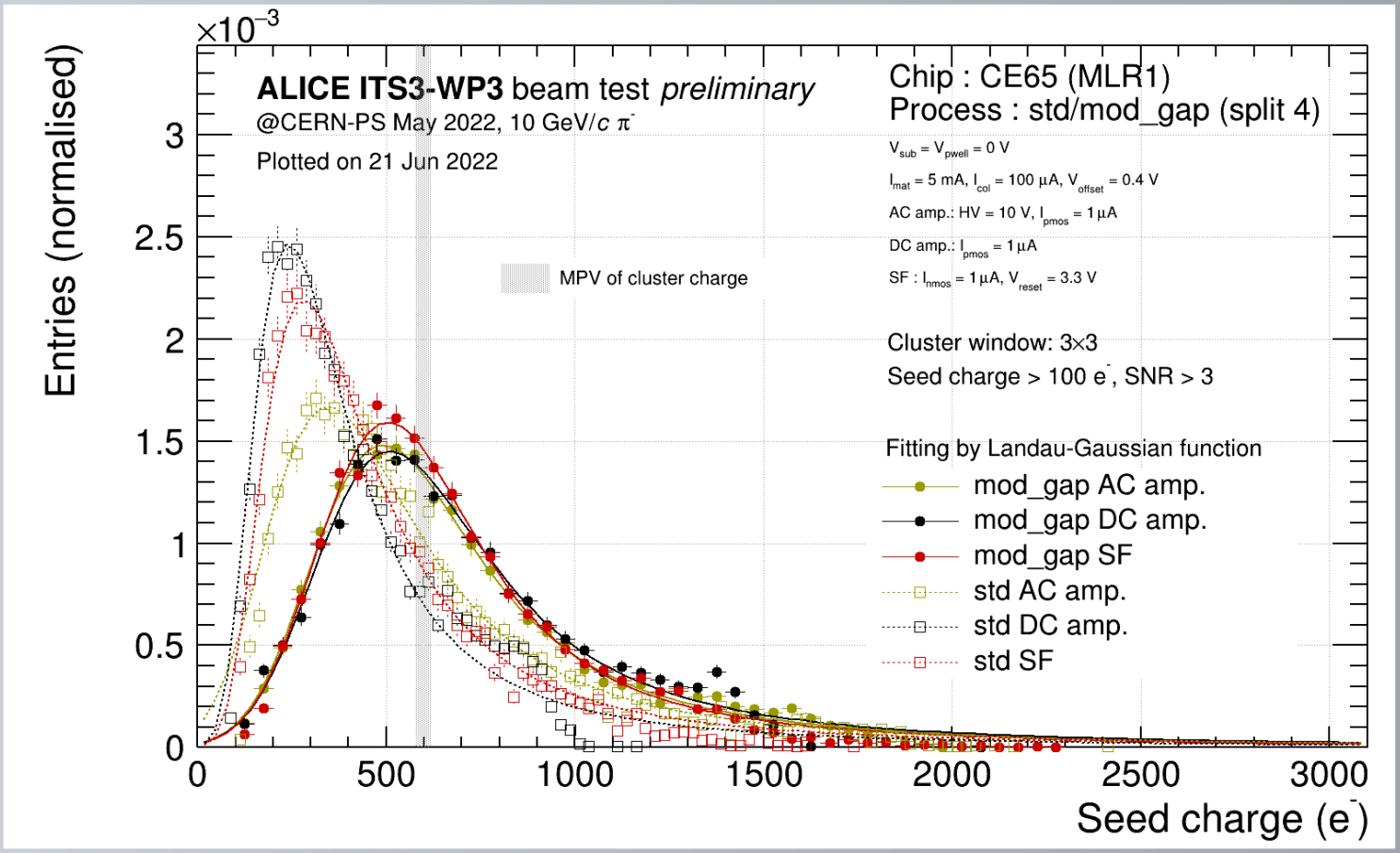
All submatrices in standard and modified processes collect the same total charge



Development of the sensor

CE65: Cluster charge doesn't depend on process modification and pixel architecture

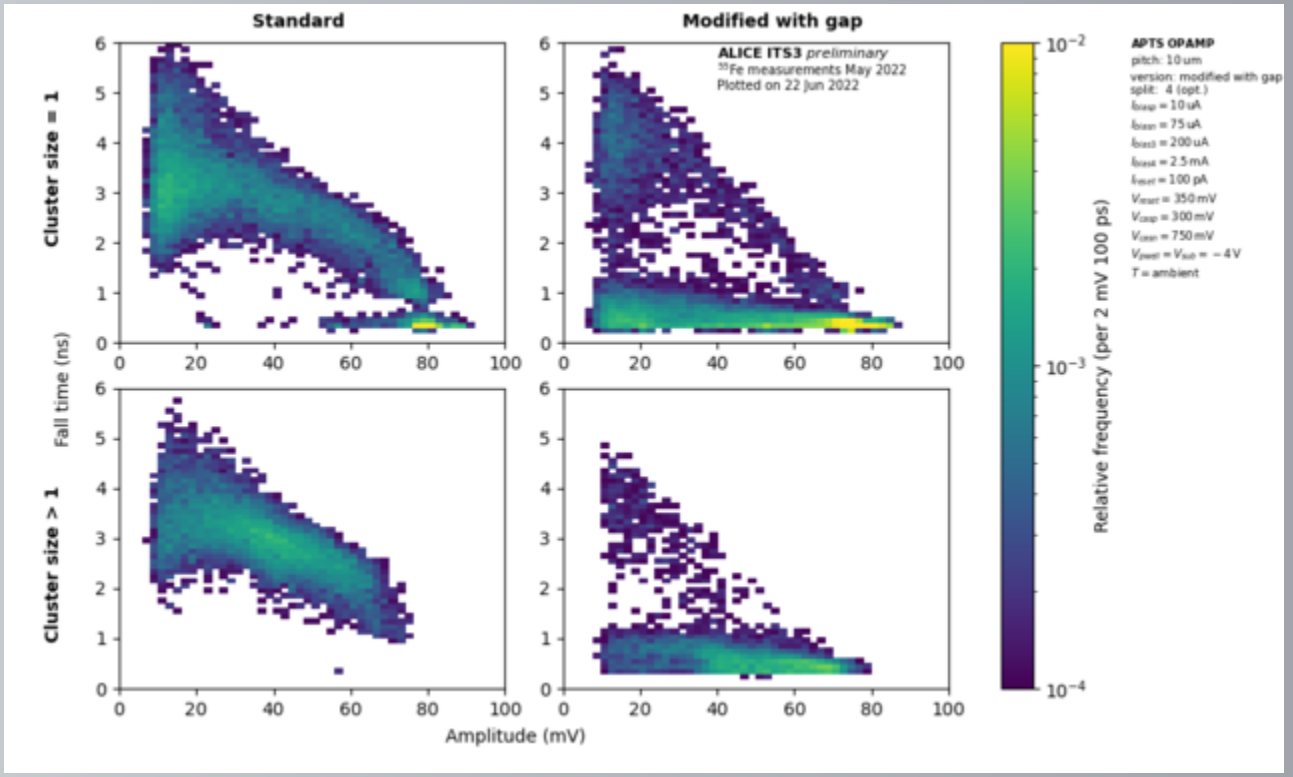
With modified process all the charge is mostly collected by a single pixel



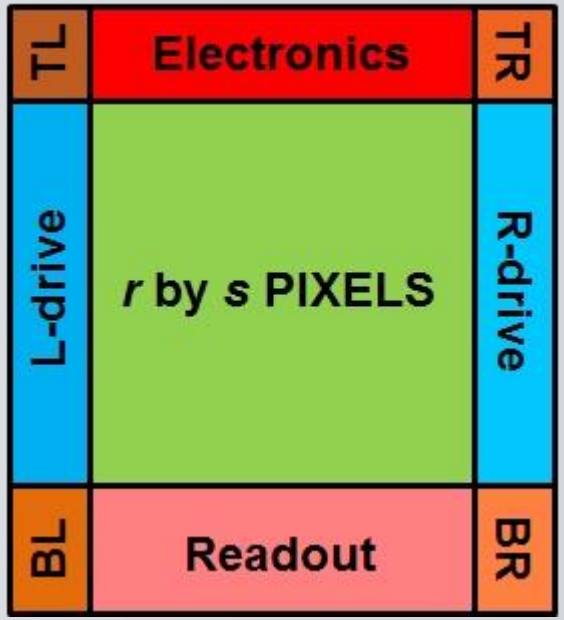
Development of the sensor

APTS OpAmp: 55Fe source measurements

- Charge collection time estimated via signal fall time
- In modified process the charge is collected faster
- Timing resolution measurements in progress with the beam



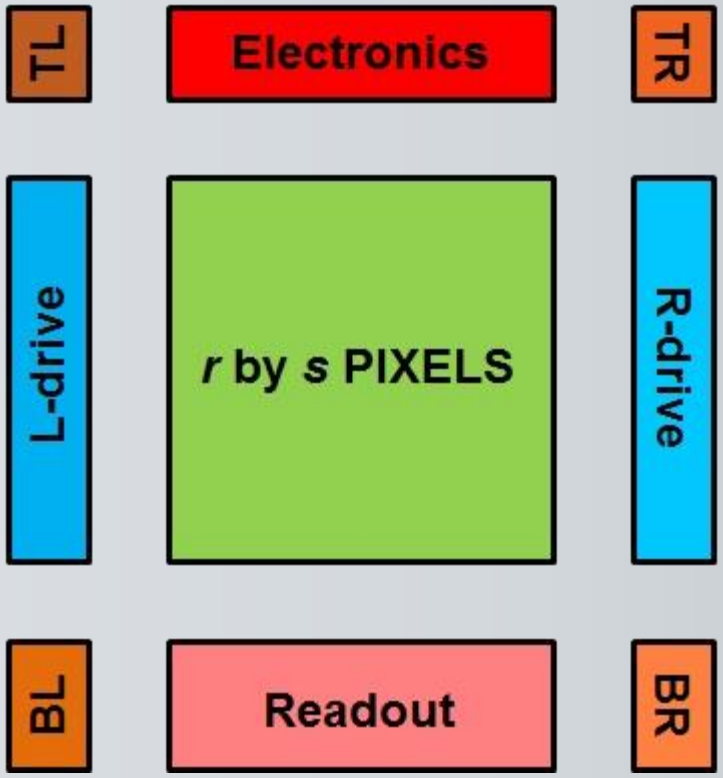
Stitching 1



In the normal design phase, all blocks (pixel matrix, electronics…) are nicely put together and the complete lay-out is sent to fabricate the masks.

The maximum useful area of a mask, defined by the field of view of the lithographic equipment, is about 25 mm x 25 mm.

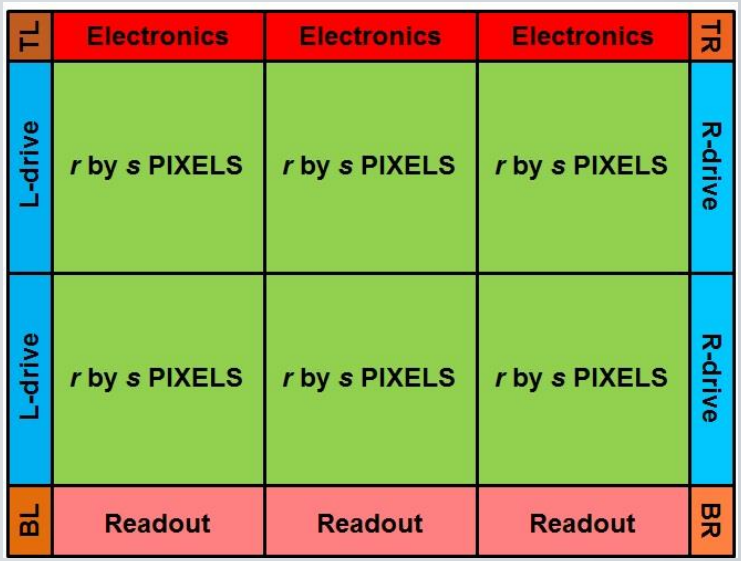
Stitching 2



Stitching is a technology that allows the designer to fabricate an image sensor that is larger than the field of view of the lithographic equipment.

The building blocks themselves are put on the reticle as individual pieces of the design.

Stitching 3

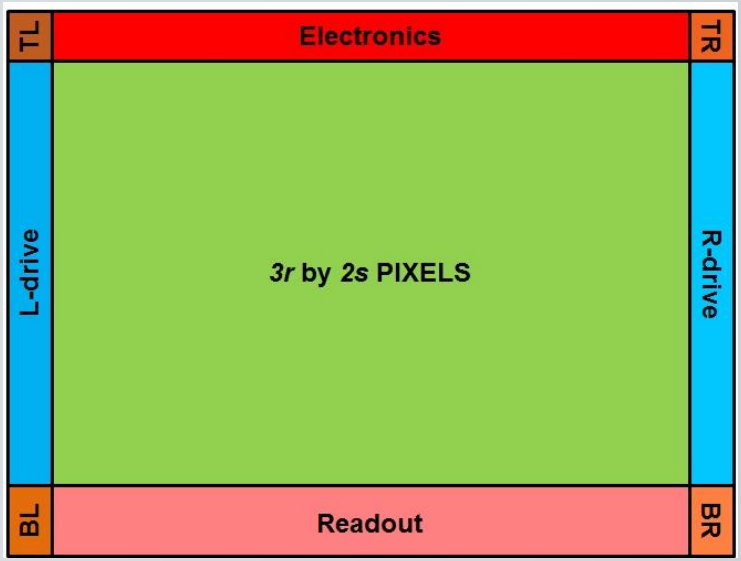


Stitching is a technology that allows the designer to fabricate an image sensor that is larger than the field of view of the lithographic equipment.

The building blocks themselves are put on the reticle as individual pieces of the design.

It is possible to “stitch” the various blocks together on the wafer during the lithographic process, making other configurations by means of multiple use of the various blocks.

Stitching 4



Stitching is a technology that allows the designer to fabricate an image sensor that is larger than the field of view of the lithographic equipment.

The building blocks themselves are put on the reticle as individual pieces of the design.

It is possible to “stitch” the various blocks together on the wafer during the lithographic process, making other configurations by means of multiple use of the various blocks.

If the design of the various blocks is carefully, the stitch lines will no longer be visible or noticeable, and the end result of the stitching technology is a large-size, monolithic image sensor.

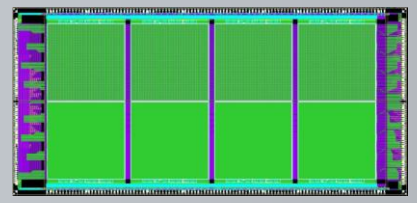
The size of the sensor will only be limited by the wafer size.

Towards the final sensor

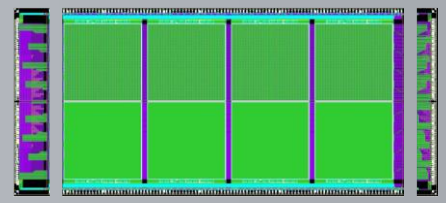
Next step: stitching

Engineering Run 1 (ER1) to establish stitching:

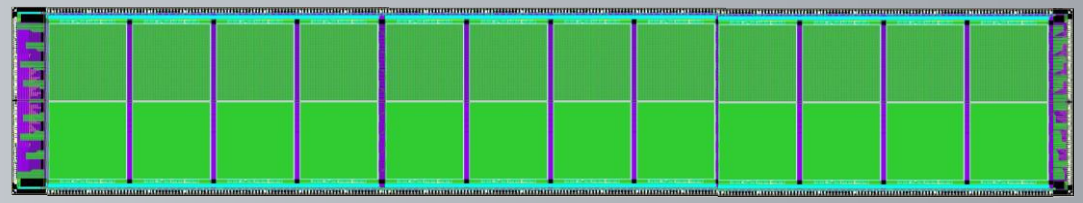
- Gain experience with design process
- Estimates on yield and parameter spread
- Production started



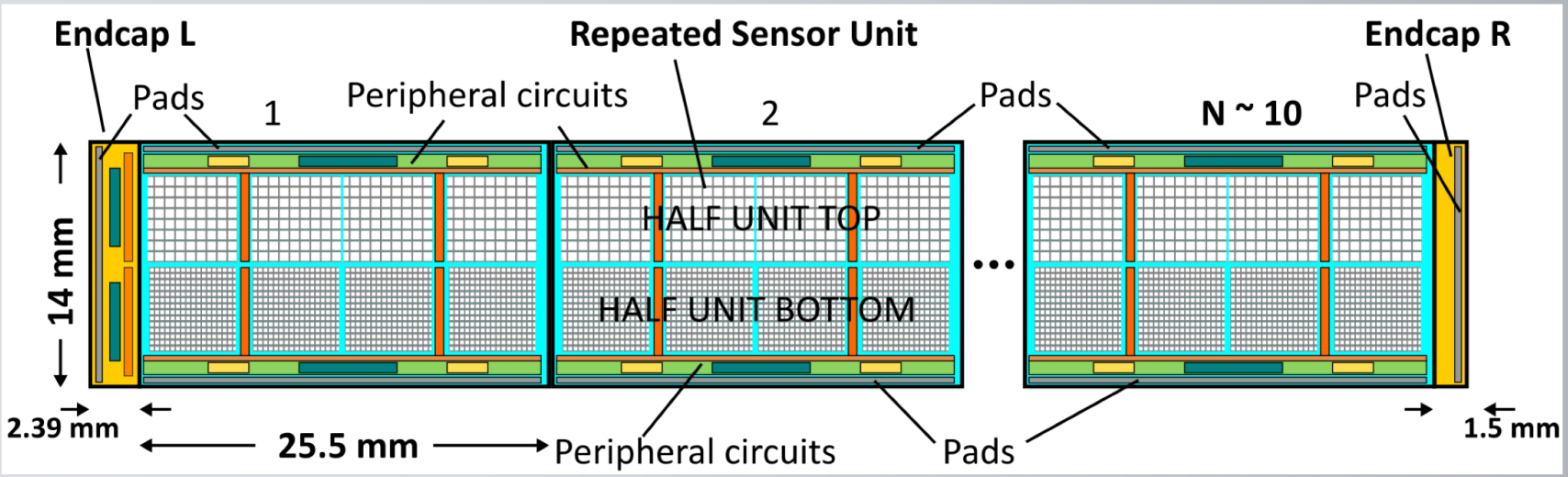
Reticle

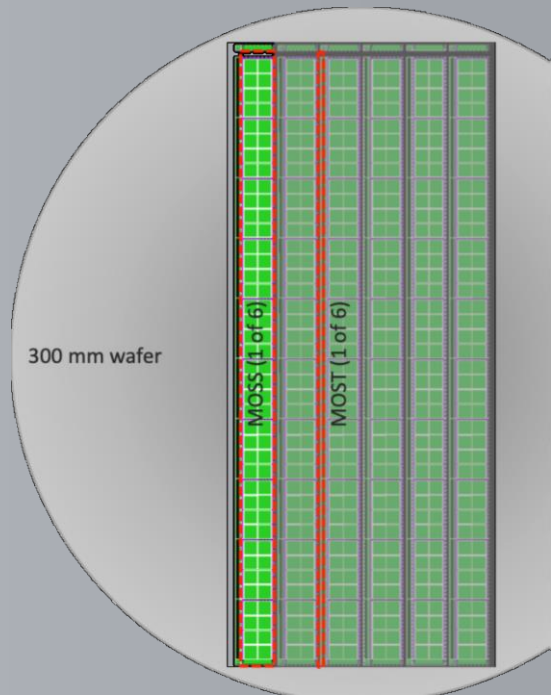


Splitted



Stitched object





Super-ALPIDE

- 9 x 2 array of ALPIDE chips
- A mock-up sensor to investigate integration and interconnection of large-scale, thinned and bent sensors
- To study the bending **AND** the interconnection of large pieces of processed chips